Dynamic Single Phase Logic with Self-timed Stages for Power Reduction in Pipeline Circuit Designs

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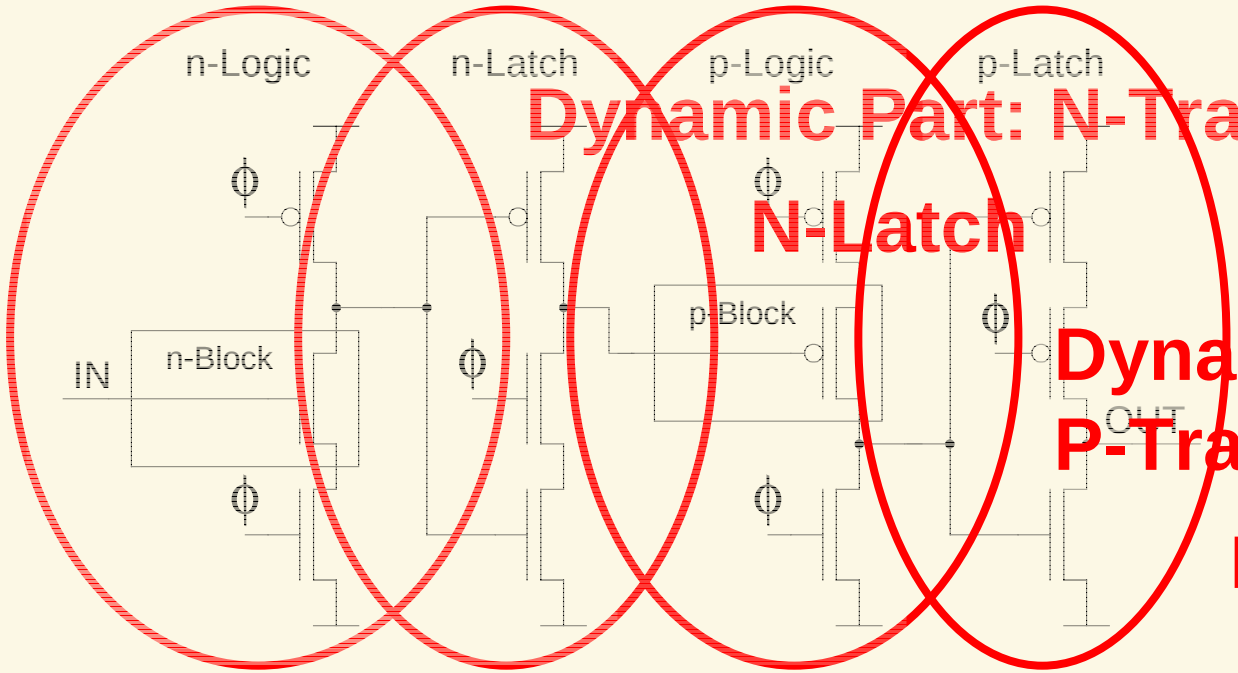
Outline

- Motivation
- True Single Phase Clock Logic
- Asynchronous structure
- Results
- Conclusions

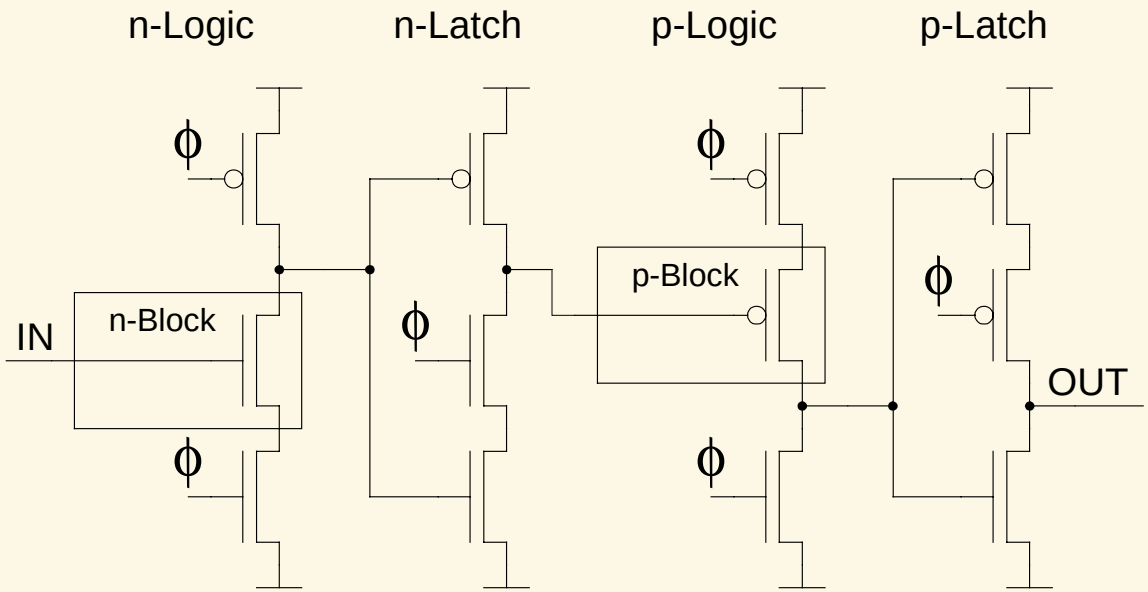
Motivation

- Fast circuits
  - Expensive calculations (e.g. cryptography)
  - → Dynamic logic styles !
- Low power
  - Wireless, battery-operated devices
  - → Asynchronous logic !
- Simple, automatic synthesis
  - Short turn around time
  - → Global single phase clock !

True Single Phase Clock - Logic



True Single Phase Clock - Logic

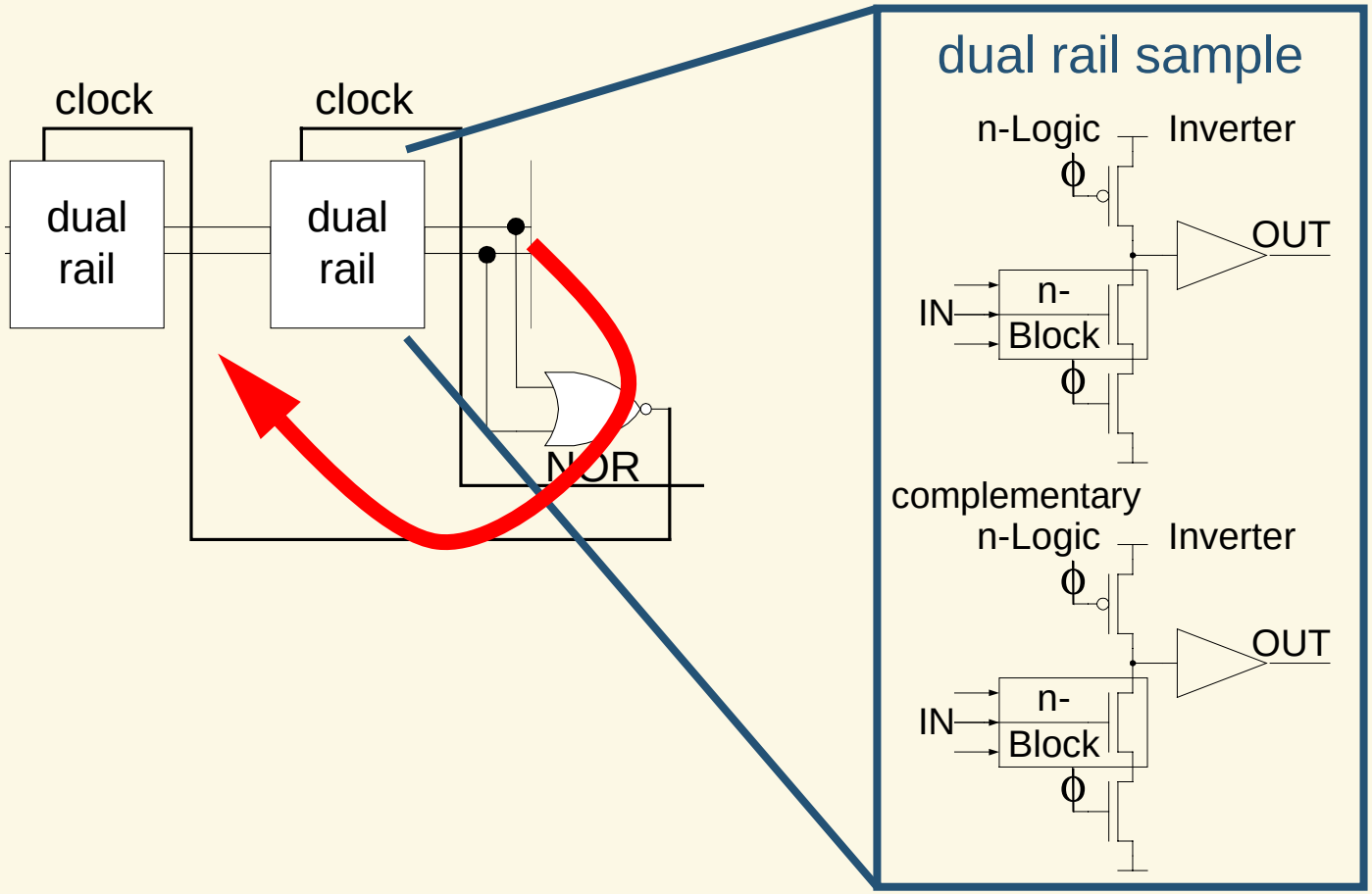


Analysis of TSPC

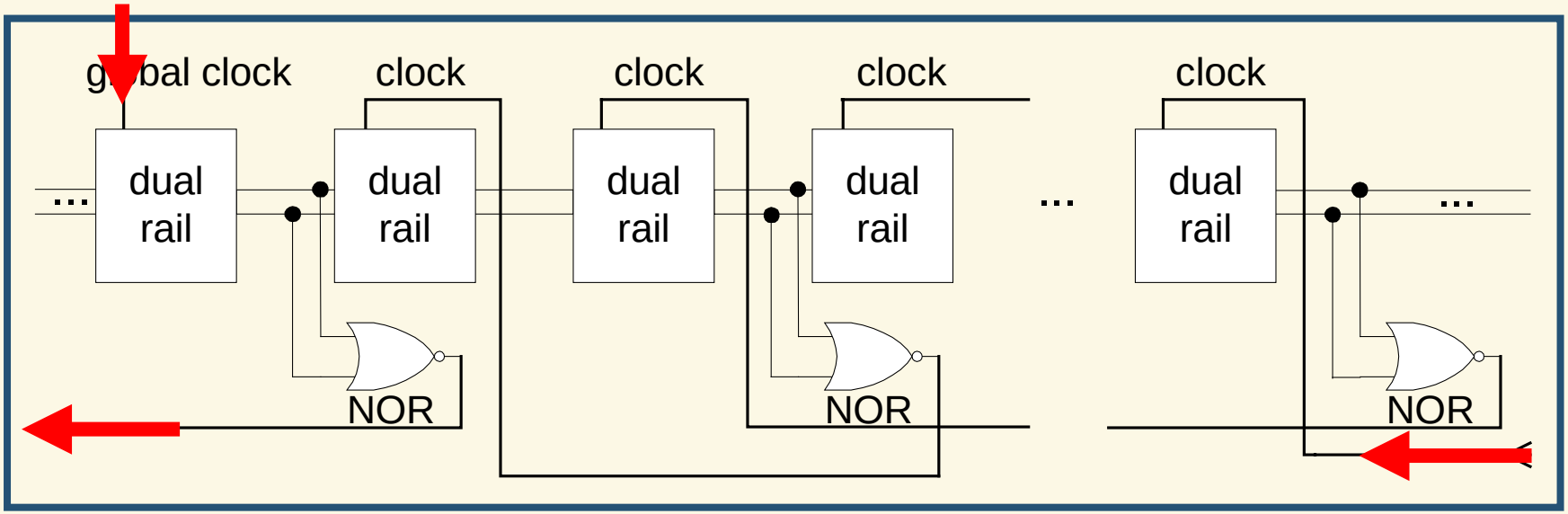
Disadvantages		Asynchronous Logic	
• Clock-load	→	Reduced	+
• Often dual rail	→	Used (must be dual rail)	~
• Often unused P-block	→	Dropped	+
• Clock-skew sensitive	→	Improved	+

Advantages			
• Register-function	→	Through self-timing	+/–
• Synthesis	→	Short chains in single clock scheme	?
• Speed: Throughput	→	Reduced	–
Latency	→	Improved	+

Asynchronous Chain (AC) – TSPC

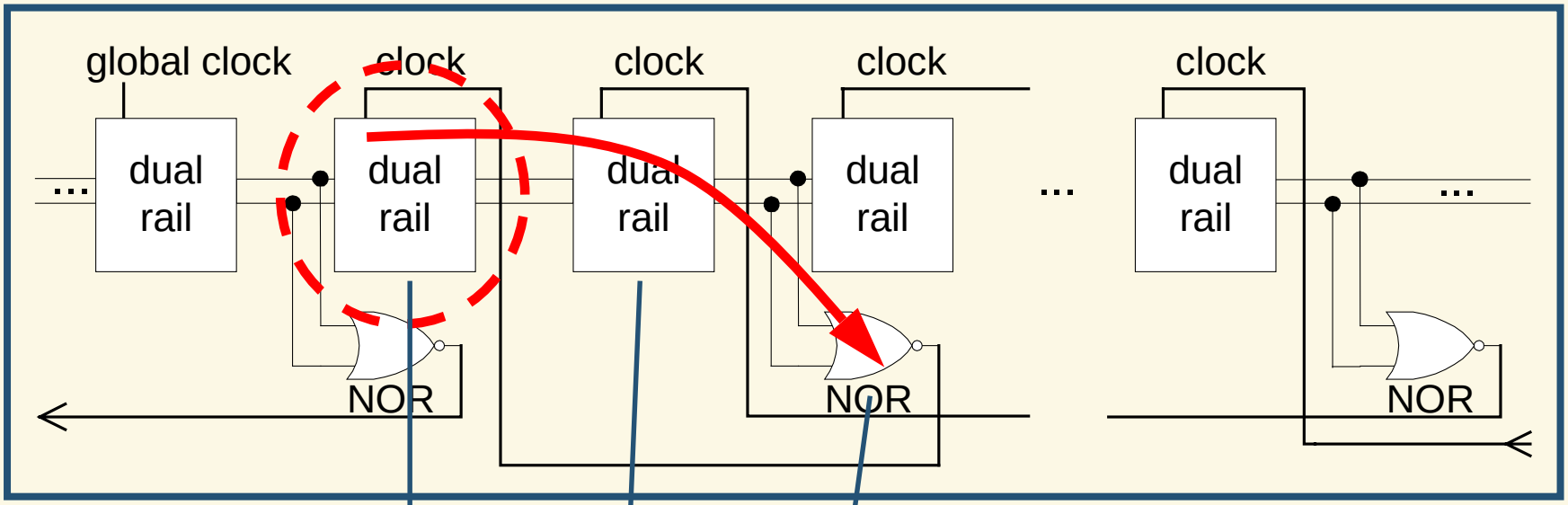


Asynchronous Chain (AC) – TSPC

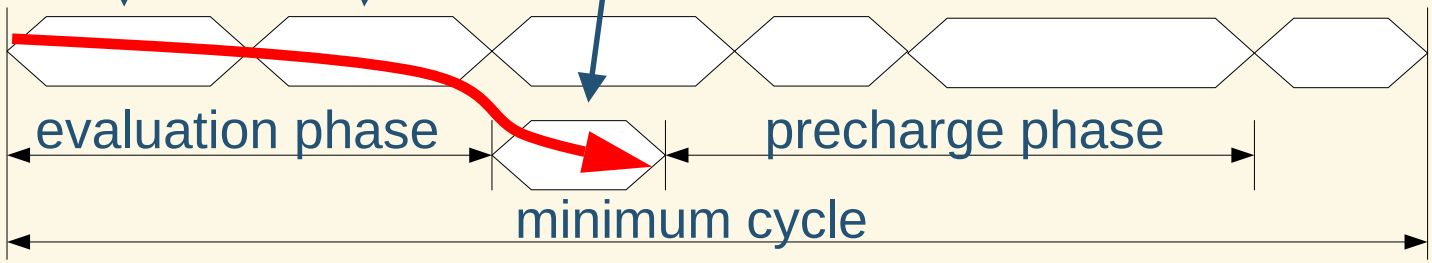


- Pass starts with global clock
- Run through the chain
- Last stage waits for self-timed signal of following chain – register function

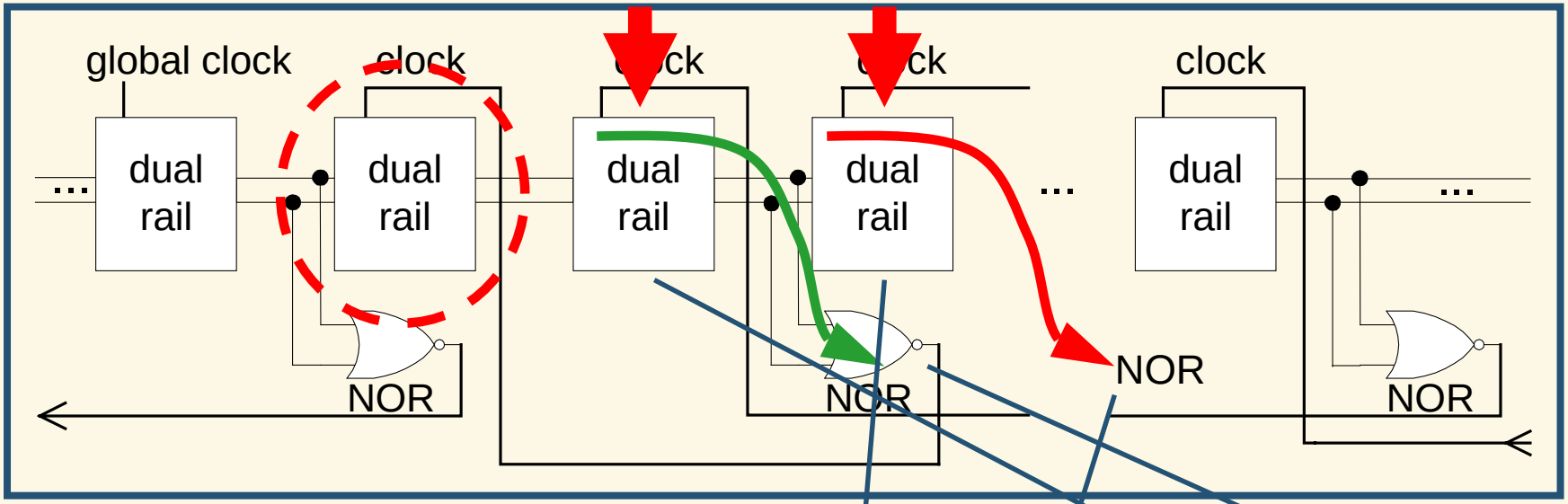
AC – TSPC – Timing



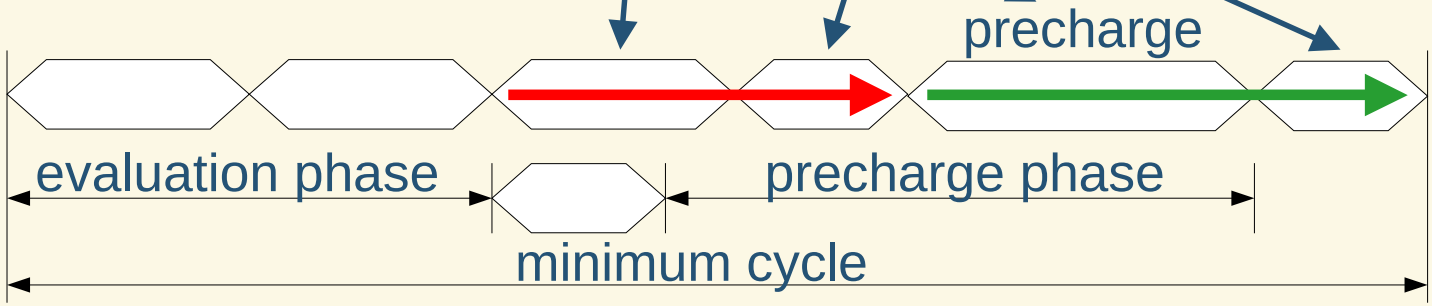
Evaluation:



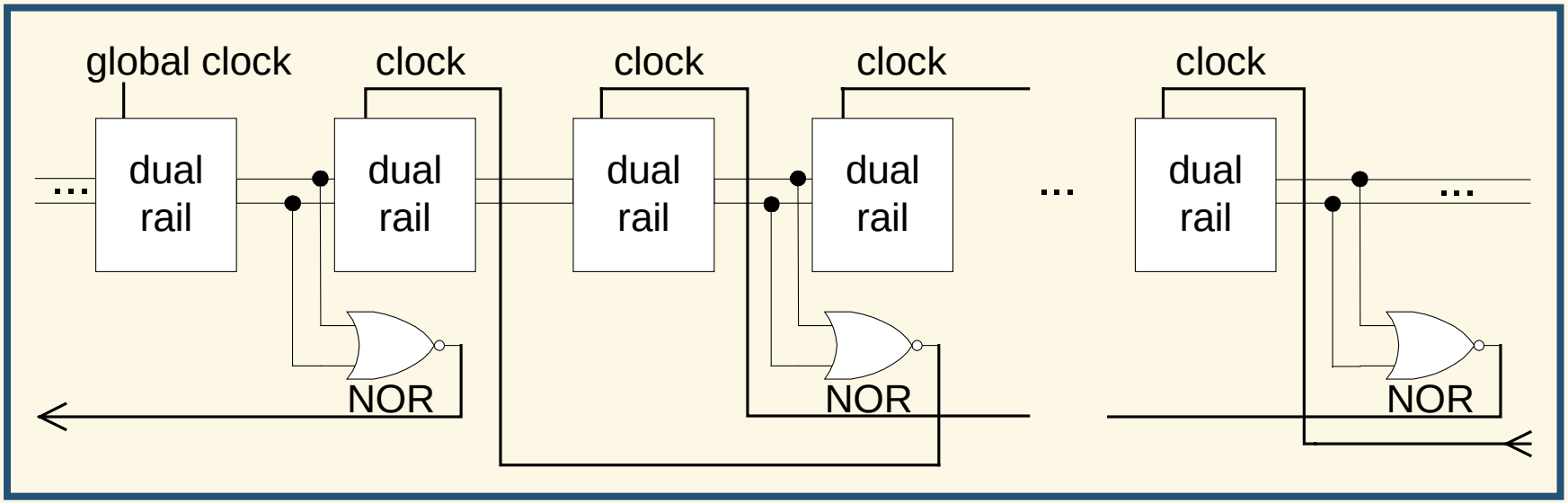
AC – TSPC – Timing



Precharge:



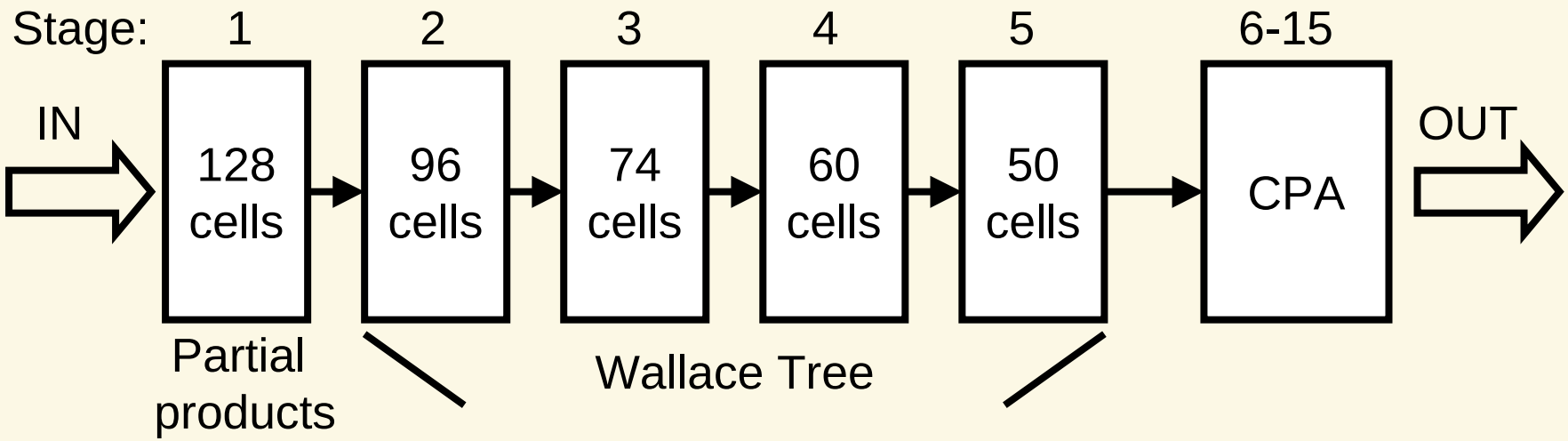
(AC – TSPC – Timing Parameters)



- Global clock longer than single cycle times
- Global clock equal evaluation time of critical path (no additional delay)
- Inclusion of self-timed gates with respect to parallel paths

Example – Wallace Tree Multiplier

- Example: 8x8 Bit Multiplier:



- TSPC: Pipeline of 15 stages – 15 cycles for multiplication
- AC-TSPC: five stages per cycle – 3 cycles for multiplication
- Identical dynamic n-parts

Results

Example: Wallace-Tree Multiplier; backannotated layout

	TSPC	AC-TSPC
Number of cycles for multiplication	1	0.2
Minimum clock cycle	1	2.5
Minimum latency	1	0.5
Power consumption for minimum clock cycle of AC-TSPC	1	0.5
Power-Delay-Product	1	0.25

Relative values for 0.6µm/3.3V (AMS)

Synthesis:

- Short chains → simple calculation scheme for asynchronous parts → externally synchronous-like behaviour
- Automatic synthesis possible, but more steps

Conclusion

- Improved power and latency with short asynchronous chains in a globally synchronous structure
- Reduced throughput
- Simpler clock-tree and robustness against clock skew
- Synthesis:
  - Splitting design in asynchronous parts, verifying parameters
  - Arrange synchronous blocks
- Implementation of various logic styles (but dual rail)