

# Networks: Complexity & Scalability

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**Abstract—Objectives of the dissertation are novel approaches to handle complexity, scalability, and derived problems in both prospective (inter)networks and in digital circuit design and architecture using a special flavor of networks—Networks-on-Chip. The thesis’ first part focuses on mechanisms for packet-switched IP networks aiming at scalability and security issues, the feasibility of new services, and the transition of conventional telecommunication services. The second part addresses complexity and scalability in digital circuit architecture and Systems-on-Chip. Research relates to Networks-on-Chip and globally asynchronous locally synchronous architectures as novel design paradigms. For evaluation, packet processing solutions of the first part have exemplarily been implemented on the developed infrastructures of the thesis’ second part.**

**Index Terms—(Inter)Networking, Scalability, Complexity, Network- & Interconnect Architectures**

### I. THESIS OUTLINE

Complexity and scalability are late-breaking topics regarding current and future networks as well as architecture and design of digital circuits and SoCs.

Networks are ubiquitous, growing, and increasingly complex. Especially, Ethernet-based, packet-switched IP networks like Internet access networks and the Internet itself gain much attention at the moment. This has (among others) the following reasons:

- The transition of classical telecommunication services into the Internet, e.g., telephony  $\hookrightarrow$  Voice-over-IP.
- Many new and inventive multimedia services are introduced these days making use of the global Internet and boosting an “always-on” mentality.

The increasing complexity leads to, e.g., exhausted address pools, scalability problems, and security issues. Two exemplary results of the research work are briefly outlined in Section I-A.

However, complexity and scalability play a role in digital circuit design as well. As integrated circuits and SoCs are getting more complex, conventional design flows and architectures cannot scale to the

same degree. This is commonly called the design-productivity-gap (DPG). The research work in this area addresses Networks-on-Chip (NoCs) and globally asynchronous locally synchronous (GALS) architectures, which are used as alternative design paradigms. Section I-B shortly reports selected aspects of this research strand.

Both part I-A and I-B merge in Section I-C. The compacted bibliography highlights selected papers.

#### A. Solutions for Access Networks & the Internet

**MAT:** Due to an increasing number of users, management of address tables and forwarding data bases (FDBs) within access nodes and core switches is getting more difficult. MAC address table explosions can occur. Furthermore, users are even able to manipulate MAC addresses resulting in duplicate MACs and other severe security problems, e.g., MAC Spoofing. The proposed solution is a special flavor of MAC Address Translation (MAT) [1], [2], [3]. User-side MACs are replaced (not encapsulated) with provider-side MACs and vice versa in a flexible way to reduce address table and FDB sizes and to prevent from security leakages.

**IPclip:** This solution refers to what we call Trust-By-Wire (TBW), which describes an inherent discrepancy between circuit- and packet-switched networks. TBW *is given* in classical, circuit-switched networks, e.g., PSTN or ISDN, but *is not given* in packet-switched IP networks. In circuit-switched networks, a phone number directly references to a fixed line ( $\rightarrow$  a location/address  $\rightarrow$  a person). But this direct relationship is not given for IP addresses in the Internet. IPs cannot be considered as equivalent to phone numbers, because an IP address does not uniquely reference a physical line. Furthermore, IPs do not provide location information in any case whereas phone numbers do have a well-defined origin. To reestablish the TBW in packet-switched IP networks, a mechanism called IPclip has been proposed [4]. The term *IPclip* is derived from the

optional CLIP feature of Integrated Services Digital Networks (ISDN), which transmits the caller's number to the callee. IPclip reuses selected, principle aspects of the ISDN CLIP by transmitting a flavor of trustable location information in packet-switched IP networks to facilitate enhanced and new services as in [4].

Research work in this section is done with support of and in cooperation with Nokia Siemens Networks.

### B. Networks-on-Chip & GALS

Due to an increasing DPG, new concepts are needed for the design and architecture of integrated digital systems. Aspects of the research work cover NoCs, GALS, and multi-core SoCs. Thereby, the motivation is not only to increase processing performance but also to handle complexity and billions of transistors, to partition large designs, and to enforce reuse of modular blocks. However, the application of NoCs requires rethinking the on-chip communication paradigm, which changes from synchronous signals to asynchronous messages. Existing long-time experiences from the operation and development of the Internet and of other large-scale distributed systems can be exploited in the area of on-chip networks—not least because of the fact, that NoC stacks derive from the OSI reference model as well.

In [5], principles of distributed (object) systems have been reused for NoC-based systems. Flexible building blocks for the development of NoC- and GALS-based systems have been developed [6]. Thereby, the research work especially addresses application-specific NoCs with small hardware footprint (the focus is on network packet processing as use case), which are to be used in field programmable gate arrays (FPGAs). The feasibility of NoC interconnects in FPGAs has been discussed in [7], [8].

### C. Integrating both Research Strands

The thesis' first part addresses issues and problems regarding complexity and scalability that do *exist in large-scale, packet-switched IP networks*. Solutions have been developed or are currently under development [2], [4]. Selected mechanism have been realized as a fully functional packet processing prototype [9] using a conventional, pipelined architecture [10].

The second part addresses complexity and scalability *in digital system design and SoCs*. The development and use of a special flavor of small-scale networks, Networks-on-Chip, as on-chip interconnection and communication infrastructure is integral part of this strand of the research work [6], [8].

To merge both topics, the same mechanisms from Section I-A have been realized in VHDL as modular

IP cores. They have exemplarily been applied to the developed NoC and GALS architectures to evaluate this approach [11]. This way, two functionally equal prototypes, which base on different design paradigms, can be compared against each other. One aspect that is going to be evaluated is to refine SUN's slogan "The network is the computer!" to "The network is the buffer!". This is part of current and future work.

## II. CONCLUSION

This brief outline described the main aspects and recent results of the author's research work. Major terms are *scalability* and *complexity* in different areas of networking, packet processing, and integrated SoCs. Thereby, networks covered by the research work range from large-scale networks like the Internet down to small-scale NoCs. Selected aspects of the IPDPS's scope are thus touched in this proposal, e.g., network scalability, communication protocols, and network & interconnect architectures.

Currently, the author is in his fourth PhD year and will finish in 2008.

Further information, full references, and pdf-papers can be obtained from the websites given below the affiliation.

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