Prof. Dr.-Ing. habil. Christian Haubelt

Institute of Applied Microelectronics and Computer Engineering
Department of Computer Science and Electrical Engineering
University of Rostock
Richard-Wagner Str. 31, 18119 Rostock, Germany
Phone: +49 381 498 - 7280, Fax: +49 381 498 - 118 7250
christian.haubelt@uni-rostock.de
http://www.imd.uni-rostock.de/index.php?id=christian_haubelt

Experience

06/2011- now	University of Rostock, Germany W3-Professor of Embedded Systems
10/2010-03/2011	University of Potsdam, Germany Substitute Professor of Computer Engineering
09/2008-10/2008:	UC Irvine, Center for Embedded Computer Systems, Irvine, CA, U.S.A. Visiting Researcher supported by Bavaria California Technology Center (BaCaTeC)
06/2005 – 05/2011	Institute Hardware-Software-Co-Design, Computer Science Department at the University of Erlangen-Nuremberg, Erlangen, Germany Habilitand (Researcher)
01/2004 – 05/2011	Head of the System-Level Design Automation (SDA) group at the Institute Hardware-Software-Co-Design, Computer Science Department at the University of Erlangen-Nuremberg, Erlangen, Germany
01/2003 - 05/2005	Institute Hardware-Software-C-Design, Computer Science Department at the University of Erlangen-Nuremberg, Erlangen, Germany Research Assistant
05/2001 - 12/2002	Computer Engineering Group; Electrical Engineering Department at the University of Paderborn, Paderborn, Germany Research Assistant

---

Education

07/2010	University of Erlangen-Nuremberg, Erlangen, Germany Habilitation (postdoctoral lecture qualification) in Computer Engineering Thesis Title “Design and Verification of Embedded Digital Hardware/Software Systems”
06/2005	University of Erlangen-Nuremberg, Erlangen, Germany Dr.-Ing. (Ph.D.) in Computer Science, *summa cum laude* Thesis Title: „Automatic Model-Based Design Space Exploration for Embedded Systems – A System Level Approach“.
04/2001	University of Paderborn, Paderborn, Germany Diplom-Ingenieur (Diploma degree) in Electrical Engineering
07/1992	Herder Gymnasium, Minden, Germany Abitur (university entrance diploma)

Professional Services

Memberships:

1. IEEE (Institute of Electrical and Electronics Engineers, since 2001, Senior Member since 2014)
2. GI (Gesellschaft für Informatik, since 2009 member of the steering committee for the working group on "General Methodologies and Support of Circuit and System Design Processes")
3. HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation, since 2012)
4. Wissenschaftsverbund IuK, (Wissenschaftsverbund "Entwicklung, Anwendung und Folgen moderner Informations- und Kommunikationstechnologien" der Universität Rostock, since 2012)

Editor:

1. Elsevier Journal of Systems Architecture, Subject Areas Editor “Multicore” und “Multiprocessor Systems” (2009 - 2014)

Reviewer:

Scientific organizations:

1. German Science Foundation (DFG)
2. Technology Foundation STW, The Netherlands
3. The German Israeli Foundation for Scientific Research and Development

Textbooks:

4. Springer-Verlag Heidelberg/Berlin

Journals:

5. IEEE Transactions on Computers
6. IEEE Transactions on Computer Aided Design
7. IEEE Transactions on Parallel and Distributed Systems
8. IEEE Transactions on Very Large Scale Integration Systems
9. IEEE Transactions on Signal Processing
10. IEEE Transactions on Evolutionary Computation
11. IEEE Transactions on Multimedia
12. IEEE Embedded Systems Letters
13. ACM Transactions on Design Automation of Electronic Systems
14. ACM Transactions on Embedded Computer Systems
15. Springer Journal on Design Automation for Embedded Systems
16. Springer Journal of Signal Processing Systems
17. Springer International Journal of Parallel Programming
18. Springer Computational Optimization and Applications
19. Sensors
20. EURASIP Journal on Embedded Systems
21. Elsevier Microprocessors and Microsystems
22. Elsevier Journal of Systems Architecture
23. Elsevier Simulation Modelling Practice and Theory

Conference Organization:

1. Design Automation and Test in Europe 2013-2016 (Topic Chair “System Specifications, Models and Methodologies”)
2. Conference on Hardware/Software Codesign and System Synthesis 2016 (Track Chair "System-level design")
3. Conference on Hardware/Software Codesign and System Synthesis 2015 (Track Chair "Embedded systems architecture" and Best Paper Award committee member)
4. Electronic System Level Synthesis Conference 2014 (Program Chair)
5. Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2013 (Workshop Organizer)

6. Forum on Design Languages 2012 (Special Session Organizer “Invasive Programming of Heterogeneous Multi-Core Systems”)
7. Design Automation and Test in Europe 2012 (Friday Workshop Organizer “Quo Vadis, Virtual Platforms? - Challenges and Solutions for Today and Tomorrow”)
8. Conference on Systems, Architectures, Modeling, and Simulation 2011 (Special Session Organizer “What’s next in ESL”, pp. 330)
9. Conference on Systems, Architectures, Modeling, and Simulation 2010 (Topic Chair “Design Automation”)
10. Compiler-Assisted System-On-Chip Assembly 2010 (Workshop Organizer)
11. Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2007 (Workshop Organizer)

Program Committee:

1. Design Automation and Test in Europe 2008 – 2016
2. Conference on Hardware/Software Codesign and System Synthesis 2007 - 2016
3. Conference on Systems, Architectures, Modeling, and Simulation 2010 – 2016
4. Forum on Design Languages 2006 – 2016
5. Workshop on Software and Compilers for Embedded Systems 2012 – 2014, 2016
6. International Workshop on Multi-Objective Many-Core Design 2014 – 2016
7. Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools 2016
8. Workshop on Integrating Dataflow, Embedded computing and Architecture 2016
9. Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2007 – 2016
10. Design Automation Conference 2015
11. Electronic System Level Synthesis Conference 2011 – 2015
12. Asia and South Pacific Design Automation Conference 2014
13. International Conference on Embedded and Ubiquitous Computing 2014
14. International Conference on Computer-Aided Design 2011 – 2013
15. Real-Time and Embedded Technology and Applications Symposium 2013
16. Reconfigurable Architectures Workshop 2012
17. Workshop on Cyber-Physical Systems 2011, 2012
18. Conference on Evolutionary Multi-Criterion Optimization 2007 – 2011
19. Congress on Evolutionary Computation 2005 - 2010
20. Workshop on Systems, Architectures, Modeling, and Simulation 2009
21. Conference on Computational Intelligence and Security 2007, 2008
22. Genetic and Evolutionary Computation Conference 2006

Publications

Books:

1. C. Haubelt and D. Timmermann. *Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen*. Rostock, Germany, 2013.
2. C. Haubelt and J. Teich. *Digitale Hardware/Software-Systeme: Spezifikation und Verifikation*. Springer-Verlag, Berlin Heidelberg, 2010.
3. J. Teich and C. Haubelt. *Digitale Hardware/Software-Systeme: Synthese und Optimierung*. 2. Auflage, Springer-Verlag, Berlin Heidelberg, 2007.
4. C. Haubelt and J. Teich. *Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen*. Shaker Verlag, Aachen, Germany, 2007.

5. C. Haubelt. *Automatic Model-Based Design Space Exploration for Embedded Systems - A System Level Approach*. Dissertation, University of Erlangen-Nuremberg, ISBN 3-89574-572-3, © Verlag Dr. Köster, Berlin, 2005.

Book Chapters:

1. J. Falk, C. Haubelt, C. Zebelein, and J. Teich. *Integrated Modeling Using Finite State Machines and Dataflow Graphs*. In Handbook of Signal Processing Systems, 2nd ed., pp. 975-1013, Springer, 2013.
2. M. Streubühr, J. Gladigau, C. Haubelt and J. Teich. *Efficient Approximately-Timed Performance Modeling for Architectural Exploration of MPSoCs*. In Advances in Design Methods from Modeling Languages for Embedded Systems and SoC's, pp. 59-72, Springer, 2010.
3. J. Falk, J. Keinert, C. Haubelt, J. Teich and C. Zebelein. *Integrated Modeling Using Finite State Machines and Dataflow Graphs*. In Handbook of Signal Processing Systems, pages 1041-1075, Springer, 2010.
4. C. Haubelt, D. Koch, F. Reimann, T. Streichert and J. Teich. ReCoNets – Design Methodology for Embedded Systems Consisting of Small Networks of Reconfigurable Nodes and Connections. In Dynamically Reconfigurable Systems - Architectures, Design Methods and Applications, pages 223-244. Springer, Heidelberg, 2010.
5. J. Gladigau, C. Haubelt and J. Teich. *Symbolic Scheduling of SystemC Dataflow Designs*. In M. Radetzki, editor, Languages for Embedded Systems and their Applications, volume 36 of Lecture Notes in Electrical Engineering, pages 183–199. Springer Netherlands, 2009.
6. T. Streichert, C. Haubelt, D. Koch and J. Teich. *Concepts for Self-Adaptive and Self-Healing Networked Embedded Systems*. Organic Computing, Rolf Würtz (Ed.), Springer Series Understanding Complex Systems, pp. 241-260, Springer, 2008.
7. B. Niemann, C. Haubelt, M. Uribe and J. Teich. *Formalizing TLM with Communicating State Machines*. In Advances in Design and Specification Languages for Embedded Systems, pp. 225-242, Springer, 2007.
8. C. Haubelt, S. Mostaghim, F. Slomka, J. Teich and A. Tyagi. *Hierachical Synthesis of Embedded Systems Using Evolutionary Algorithms*. In Evolutionary Algorithms in System Design by Drechsler, R. and Drechsler, N., in Genetic Algorithms and Evolutionary Computation (GENA), pp. 63-104, Kluwer Academic Publishers, Boston, Dordrecht, London, 2003.
9. C. Haubelt, J. Teich, K. Richter and R. Ernst. *Flexibility / Cost-Tradeoffs of Platform-Based Systems*. In Embedded Processor Design Challenges, E. Deprettere, J. Teich, and S. Vassiliadis, editors, Lecture Notes in Computer Science (LNCS), Vol. 2268, pp. 38-56, Springer, Berlin, Germany, March 2002.

Reviewed Journals:

1. L. Middendorf and C. Haubelt. *A Programmable Graphics Processor based on Partial Stream Rewriting*. In Computer Graphics Forum 32(7), pp. 325-334, 2013.
2. J. Falk, C. Zebelein, C. Haubelt, and J. Teich. *A Rule-Based Quasi-Static Scheduling Approach for Static Islands in Dynamic Dataflow Graphs*. ACM Transactions on Embedded Computing Systems 12(3), pp. 74:1 – 74:31, 2013.
3. J. Gladigau, C. Haubelt, and J. Teich. *Model-Based Virtual Prototype Acceleration*. In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 31(10), pp. 1572 – 1585, 2012.
4. R. Dorsch, R. K. Errickson, M. M. Helms, G. Crew, T. A. Gregg, W. Haileselassie, L. W. Helmer, A. Kohler, K. M. Pandey, S. Roscher, E. S. Rotter, C. Haubelt. *IBM Parallel Sysplex design for the IBM z196 system*. IBM Journal of Research and Development 56(1): 9, 2012.
5. J. Gladigau, A. Gerstlauer, C. Haubelt, M. Streubühr, and J. Teich. *Automatic System-Level Synthesis: From Formal Application Models to Generic Bus-Based MPSoCs.* In Transactions on HiPEAC 5(4), pp. 1-22, 2011.
6. J. Falk, C. Zebelein, J. Keinert, C. Haubelt, J. Teich and S. S. Bhattacharyya. *Analysis of SystemC Actor Networks for Efficient Synthesis*. In ACM Transactions on Embedded Computing Systems, 10(2):94–127, 2010.
7. A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski and J. Teich. *Electronic System-Level Synthesis Methodologies*. In IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 28(10), pp. 1517-1530, 2009.

8. J. Keinert, M. Streubühr, T. Schlichter, J. Falk, J. Gladigau, C. Haubelt, J. Teich and M. Meredith. *SYSTEMCODESIGNER - An Automatic ESL Synthesis Approach by Design Space Exploration and Behavioral Synthesis for Streaming Applications*. In ACM Transactions on Design Automation of Electronic Systems, 14(1), pp. 1-23, 2009.
9. T. Streichert, M. Glaß, C. Haubelt and J. Teich. *Design Space Exploration of Reliable Networked Embedded Systems*. In Journal on Systems Architecture (JSA). Volume 53(10): 751-763, 2007.
10. F. Dittmann, F. Rammig, M. Streubühr, C. Haubelt, A. Schallenberg and W. Nebel. *Exploration, Partitioning and Simulation of Reconfigurable Systems*. it - Information Technology, http://it-information-technology.de , Oldenbourg Wissenschaftsverlag, vol. 49(3):149-156, 2007.
11. T. Streichert, C. Strengert, D. Koch, C. Haubelt and J. Teich. *Communication Aware Optimization of the Task Binding in Hardware/Software Reconfigurable Networks*. Journal on Integrated Circuits and Systems, Volume 2, Number 1, pp. 29-36, March 2007.
12. C. Haubelt, J. Falk, J. Keinert, T. Schlichter, M. Streubühr, A. Deyhle, A. Hadert and J. Teich. *A SystemC-based Design Methodology for Digital Signal Processing Systems*. In EURASIP Journal on Embedded Systems, Special Issue on Embedded Digital Signal Processing Systems, Volume 2007 (2007), Article ID 47580, 22 pages, March 2007.
13. T. Streichert, D. Koch, C. Haubelt and J. Teich. *Modeling and Design of Fault-Tolerant and Self-Adaptive Reconfigurable Networked Embedded Systems*. EURASIP Journal on Embedded Systems, Volume 2006 (2006), Article ID 42168, 15 pages, Hindawi Publishing Corporation.
14. C. Haubelt, T. Schlichter and J. Teich. *Improving Automatic Design Space Exploration by Integrating Symbolic Techniques into Multi-Objective Evolutionary Algorithms*. In International Journal of Computational Intelligence Research (IJCIR), Special Issue on Multiobjective Optimization and Applications, Volume 2, Issue 3. pp. 239-254, 2006.

Patents:

1. A. Biewer, D. Thoss, J. Gladigau, and C. Haubelt. *Control Device for a Motor Vehicle*. WIPO Patent WO 2015/082109 A1, Jun. 11, 2015.
2. A. Biewer, D. Thoss, J. Gladigau, and C. Haubelt. *Steuergerät für ein Kraftfahrzeug*. Offenlegungsschrift DE 10 2013 224 702 A1, Jun. 3, 2015
3. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. United States Patent 8,554,972 B2, Oct. 8, 2013.
4. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. United States Patent 8,018,249 B2, Sep. 13, 2011.
5. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. Patent Application Publication US 2011/0055449 A1, Mar. 3, 2011.
6. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. Patent Application Publication US 2010/0283505 A1, Nov. 11, 2010.
7. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. Patent Application EP 2188894 A1, May 26, 2010.
8. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. Patent Application EP 2188735 A1, May 26, 2010.
9. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. WIPO Patent Application WO/2009/033630 A1, Mar. 19, 2009.
10. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. WIPO Patent Application WO/2009/033631 A1, Mar. 19, 2009.
11. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Logic System and Method for Designing a Logic Chip*. Patent Application PCT/EP2008/007342, Sep. 8, 2008.
12. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Logic Chip, Method and Computer Program for Providing a Configuration Information for a Configurable Logic Chip*. Patent Application PCT/EP2008/007343, Sep. 8, 2008.
13. D. Koch, T. Streichert, C. Haubelt and J. Teich. *Efficient Reconfigurable On-Chip Buses*. European Patent Application EP07017975, Sep. 13, 2007.

Reviewed Conference Papers:

1. N. Büscher, L. Middendorf, C. Haubelt, R. Dorsch, and F. Wegelin. *Improving Repeatability and Reproducibility of Mobile Tests for Inertial Measurement Units*. Symposium on Engineering Interactive Computing Systems (EICS'16), Brussels, Belgium, June, 2016. (to appear)
2. F. Grützmacher, B. Beichler, C. Haubelt, B. Theelen. *Dataflow-based Modeling and Performance Analysis for Online Gesture Recognition*. In Proceedings of the International Workshop on modeling, analysis and control of complex Cyber-Physical Systems (CPSData'16), Vienna, Austria, April, 2016. (to appear)
3. S. Stieber, R. Dorsch, and C. Haubelt. *Accurate Sample Time Reconstruction for Sensor Data Synchronization*. In Proceedings of the International Conference on Architecture of Computing Systems (ARCS), pp. 185-196, Nuremberg, Germany, April, 2016.
4. F. Grützmacher, J.-P. Wolff, and C. Haubelt. *Sensor-Based Online Hand Gesture Recognition on Multi-Core DSPs*. In Proceedings of the Symposium on Signal Processing on Graphics Processing Units and Multicores, pp. 898-902, Orlando, Florida, December, 2015.
5. L. Middendorf, R. Dorsch, R. Bichler, C. Strohrmann, and C. Haubelt. *A Mobile Camera-Based Evaluation Method of Inertial Measurement Units on Smartphones*. In the Proceedings of the International Conference on Sensor Systems and Software (S-CUBE'15), Rome, Italy, October 26–27, 2015. Best Paper Award (to appear)
6. L. Middendorf and C. Haubelt. *Dynamic Task Mapping of Graphics Processing Applications on Many-Core Architectures through Stream Rewriting*. In Proceedings of the IEEE Symposium on Embedded Systems for Real-time Multimedia (ESTIMEdia'15), pp. 7-8, Amsterdam, The Netherlands, October 8-9, 2015.
7. J. Falk, T. Schwarzer, M. Glaß, J. Teich, C. Zebelein, and C. Haubelt. *Quasi-Static Scheduling of Data Flow Graphs in the Presence of Limited Channel Capacities*. In Proceedings of the IEEE Symposium on Embedded Systems for Real-time Multimedia (ESTIMEdia'15), pp. 29-38, Amsterdam, The Netherlands, October 8-9, 2015.
8. B. Beichler, T. Schulz, C. Haubelt, and F. Golatowski. *A Parametric Dataflow Model for the Speed and Distance Monitoring in Novel Train Control Systems*. In Proceedings of the Fifth Workshop on Design, Modeling and Evaluation of Cyber Physical Systems (CyPhy'15), pp. 56-66, Amsterdam, The Netherlands, October 2015.
9. B. Andres, A. Biewer, J. Romero, C. Haubelt, and T. Schaub. *Improving Coordinated SMT-based System Synthesis by Utilizing Domain-specific Heuristics*. In Proceedings of the International Conference on Logic Programming and Nonmonotonic Reasoning, pp. 55-68, Lexington, KY, USA, September 27-30, 2015.
10. J. Schützel, S. Stieber, C. Haubelt, and L. Uhrmacher. *Targeted On-Line Data Extraction with SystemXtract*. In Proceedings of International Conference on Simulation Tools and Techniques (SIMUtools'15), pp. 228-237, Athens, Greece, August, 2015.
11. F. Grützmacher, J.-P. Wolff, and C. Haubelt. *Exploiting Thread-Level Parallelism in Template-Based Gesture Recognition with Dynamic Time Warping*. In Proceedings of the International Workshop on Sensor-based Activity Recognition and Interaction (iWoAR'15), pp. 6:1 – 6:6, Rostock, Germany, June, 2015.
12. T. Schwarzer, J. Falk, M. Glaß, J. Teich, C. Zebelein, and C. Haubelt. *Throughput-optimizing Compilation of Dataflow Applications for Multi-Cores using Quasi-Static Scheduling*. In Proceedings of the International Workshop on Software and Compilers for Embedded Systems (SCOPES'15), pp. 68 – 75, St. Goar, Germany, June, 2015.
13. A. Biewer, B. Andres, J. Gladigau, T. Schaub, and C. Haubelt. *A Symbolic System Synthesis Approach for Hard Real-Time Systems Based on Coordinated SMT-Solving*. In Proceedings of Design, Automation and Test in Europe (DATE'15), pp. 357-362, Grenoble, France, March, 2015.
14. A. Biewer, P. Munk, J. Gladigau, and C. Haubelt. *On the Influence of Hardware Design Options on Schedule Synthesis in Time-Triggered Real-Time Systems*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pp. 105-114, Chemnitz, Germany, March, 2015.
15. A. Nitsch, B. Beichler, F. Golatowski, and C. Haubelt. *Model-based Systems Engeneering with Matlab/Simulink in the Railway Sector*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pp. 125-134, Chemnitz, Germany, March, 2015.

16. L. Middendorf and C. Haubelt. *Scheduling of Recursive and Dynamic Data-Flow Graphs using Stream Rewriting*. In Proceedings of the International Symposium on Computer Architecture and High Performance Computing (SBAC-PADW), pp. 102-107, Paris, France, 2014.
17. B. Beichler, A. Nitsch, F. Golatowski, and C. Haubelt. *Ein abstraktes SystemC-Modell zur Analyse und Leistungsabschätzung des europäischen Zugsicherungssystems ETCS*. In Proceedings of the GI Workshop Technologien zur Analyse und Steuerung komplexer cyber-physischer Systeme (CPSData'14), Stuttgart, Deutschland, pp. 1191-1201, 2014.
18. L. Middendorf and C. Haubelt. *System Level Synthesis of Many-Core Architectures using Parallel Stream Rewriting*. In Proceedings of the Electronic System Level Synthesis Conference (ESLsyn'14), San Francisco, USA, pp. 1-6, 2014.
19. A. Biewer, J. Gladigau, and C. Haubelt. *A Novel Model for System-Level Decision Making with Combined ASP and SMT Solving*. In Proceedings of Design, Automation and Test in Europe (DATE'14), Dresden, Germany, pp. 1-4, March, 2014.
20. C. Zebelein, C. Haubelt, J. Falk, T. Schwarzer, and J. Teich. *Model-Based Actor Multiplexing with Application to Complex Communication Protocols*. In Proceedings of Design, Automation and Test in Europe (DATE'14), Dresden, Germany, pp. 1-4, March, 2014.
21. S. Stieber, J.-P. Wolff, R. Dorsch, and C. Haubelt. *Hybride Prototypisierung eines Sensorsubsystems*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Böblingen, Germany, pp. 209-212, March, 2014.
22. A. Biewer, J. Gladigau, and C. Haubelt. *Towards Tight Interaction of ASP and SMT Solving for System-Level Decision Making*. In Proceedings of the International Conference on Architecture of Computing Systems (ARCS), Lübeck, Germany, February, pp. 1-7, 2014.
23. L. Middendorf and C. Haubelt. *A Novel Graphics Processor Architecture Based on Partial Stream Rewriting*. In Proceedings of the Conference on Design and Architectures for Signal and Image Processing (DASIP 2013), Cagliari, Italy, pp. 38-45, 2013.
24. C. Zebelein, C. Haubelt, J. Falk, T. Schwarzer, and J. Teich. *Representing Mapping and Scheduling Decisions within Dataflow Graphs.* In Forum on specification and Design Languages Paris, France, pp. 1-8, 2013.
25. B. Andres, M. Gebser, M. Glaß, C. Haubelt, F. Reimann, and T. Schaub. *Symbolic System Synthesis Using Answer Set Programming*. In Proceedings of the International Conference on Logic Programming and Nonmonotonic Reasoning, pp. 79-91, Corunna, Spain, 2013.
26. L. Middendorf, C. Zebelein, and C. Haubelt. *Dynamic Task Mapping onto Multi-Core Architectures through Stream Rewriting*. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, Samos, Greece, pp. 196-204, 2013.
27. R. Kiesel, M. Streubühr, C. Haubelt, O. Löhlein, and J. Teich. *Efficient Multi-Platform Performance Evaluation of Pedestrian Detection at the Electronic System Level*. In Proceedings of Automotive meets Electronics (AmE 2013), pp. 98-103, 2013.
28. B. Andres, T. Schaub, M. Gebser, C. Haubelt, F. Reimann, and M. Glaß. *A Combined Mapping and Routing Algorithm for 3D NoCs Based on ASP.* In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Rostock, Germany, pp. 35-46, 2013.
29. C. Zebelein, C. Haubelt, J. Falk, and J. Teich. *Model-Based Representation of Schedules for Dataflow Graphs.* In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Rostock, Germany, pp. 105-115, 2013.
30. R. Kiesel, M. Streubühr, A. Terzis, C. Haubelt, and J. Teich. *Virtual Prototyping for Efficient Multi-Core ECU Development of Driver Assistance Systems*. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, Samos, Greece, pp. 33-40, July, 2012.
31. L. Middendorf, C. Bobda, and C. Haubelt. Hardware Synthesis of Recursive Functions through Partial Stream Rewriting. In Proceedings of the 49th Design Automation Conference (DAC 2012), San Francisco, USA, pp. 1207-1215, June, 2012.
32. C. Zebelein, J. Falk, C. Haubelt, and J. Teich. *A Model-Based Inter-Process Resource Sharing Approach for High-Level Synthesis of Dataflow Graphs*. In Proceedings of the Electronic System Level Synthesis Conference (ESLsyn), San Francisco, USA, pp. 17-22, June, 2012.
33. Y. Xu, B. Li, R. Hasholzner, B. Rohfleisch, C. Haubelt, and J. Teich. *Variation-Aware Leakage Power Model Extraction for System-Level Hierarchical Power Analysis*. In

Proceedings of Design, Automation and Test in Europe (DATE'12), Dresden, Germany, pp. 346-351, March, 2012.

34. Christian Zebelein, Joachim Falk, Christian Haubelt, and Jürgen Teich. Exploiting Model-Knowledge in High-Level Synthesis. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Kaiserslautern, Germany, pp. 181-191, 2012.
35. Y. Xu, R. Rosales, B. Wang, M. Streubühr, R. Hasholzner, C. Haubelt, and J. Teich. *A Very Fast and Quasi-Accurate Power-State-Based System-Level Power Modeling Methodology*. Proceedings of the International Conference on Architecture of Computing Systems (ARCS), Munich, Germany, pp. 37-49, February 2012.
36. M. Streubühr, R. Rosales, R. Hasholzner, C. Haubelt, and J. Teich. *ESL Power and Performance Estimation for Heterogeneous MPSoCs Using SystemC*. In Forum on specification and Design Languages, Oldenburg, Germany, pp. 202-209, 2011.
37. R. Kiesel, M. Streubühr, C. Haubelt, O. Löhlein and J. Teich. *Calibration and Validation of Software Performance Models for Pedestrian Detection Systems*. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, Samos, Greece, pp. 182-189, 2011.
38. L. Middendorf, C. Haubelt, and C. Bobda, *Optimizing The Costs of Communication Infrastructure In Message-Based Multicore*, Proceedings of Engineering of Reconfigurable Systems and Algorithms (ERSA '11), Las Vegas, USA, pp. 359-360, 2011.
39. F. Reimann, M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich. *Symbolic System Synthesis in the Presence of Stringent Real-Time Constraints*. In Proceedings of the 48th Design Automation Conference (DAC 2011), San Diego, USA, pp. 393-398, 2011.
40. P. Mahr, S. Christgau, C. Haubelt, and C. Bobda: *Integrated Temporal Planning, Module Selection and Placement of Tasks for Dynamic Networks-on-Chip*. Proceedings of the 25th IEEE International Symposium on Parallel and Distributed Processing (IPDPS'11), Anchorage, USA, pp. 258-263, 2011
41. P. Kutzer, J. Gladigau, C. Haubelt and J. Teich. *Automatic Generation of System-Level Virtual Prototypes from Streaming Application Models*. Proceedings of the 22nd IEEE International Symposium on Rapid System Prototyping, Karlsruhe, Germany, pp. 128-134, 2011.
42. J. Falk, C. Zebelein, C. Haubelt and J. Teich. *A Rule-Based Static Dataflow Clustering Algorithm for Efficient Embedded Software Synthesis*. Proceedings of Design, Automation and Test in Europe (DATE'11), IEEE Computer Society, Grenoble, France, pp. 521-526, 2011.
43. M. Glaß, M. Lukasiewycz, F. Reimann, C. Haubelt and J. Teich. *Symbolic System Level Reliability Analysis*. In Proceedings of the International Conference on Computer-Aided Design (ICCAD). San Jose, USA. pp. 185-189, 2010.
44. F. Reimann, M. Glaß, C. Haubelt, M. Eberl and J. Teich. *Improving Platform-Based System Synthesis by Satisfiability Modulo Theories Solving*. In Proceedings of the 8th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS). Scottsdale, USA, pp. 135-144, 2010.
45. J. Gladigau, A. Gerstlauer, M. Streubühr, C. Haubelt and J. Teich. *A System-Level Synthesis Approach from Formal Application Models to Generic Bus-Based MPSoCs*. In proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), Samos, Greece, pp. 118-125, 2010.
46. M. Glaß, M. Lukasiewycz, C. Haubelt and J. Teich. *Towards Scalable System-Level Reliability Analysis*. In Proceedings of the Design Automation Conference (DAC 2010), Anaheim, CA, U.S.A., pages 234-239, 2010.
47. F. Reimann, A. Kern, C. Haubelt, T. Streichert and J. Teich. *Echtzeitanalyse Ethernet-basierter E/E-Architekturen im Automobil*. In Proceedings of Automotive meets Electronics (AmE 2010), pages 9-14, 2010.
48. C. Zebelein, J. Falk, C. Haubelt, J. Teich and R. Dorsch. *Efficient High-Level Modeling in the Networking Domain*. In Proceedings of Design, Automation and Test in Europe (DATE'10), Dresden, Germany, pp. 1189-1194, 2010.
49. J. Falk, C. Zebelein, C. Haubelt, J. Teich and R. Dorsch. *Integrating Hardware/Firmware Verification Efforts Using SystemC High-Level Models*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pp. 137-146, 2010.
50. R. Kiesel, O. Löhlein, A. Terzis, M. Streubühr, C. Haubelt and J. Teich. *Actor-oriented Modeling of Driver Assistance Systems for Efficient Multi-Core ECU Implementation*. In

Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, pp. 117-126, 2010.

51. M. Glaß, M. Lukasiewycz, C. Haubelt and J. Teich. Lifetime Reliability Optimization for Embedded Systems: A System-Level Approach. In Proceedings of the International Workshop on Reliability Aware System Design and Test (RASDAT '10), pp. 17-22, Bangalore, India, 2010.
52. M. Streubühr, J. Gladigau, C. Haubelt and J. Teich. *Efficient Approximately-Timed Performance Modeling for Architectural Exploration of MPSoCs*. In Proceedings of Forum on specification & Design Languages, Sophia Antipolis, France, Sep. 22-24, 2009.
53. J. Keinert, C. Haubelt and J. Teich. *Data Flow Based System Level Design and Analysis of Concurrent Image Processing Applications*. Proceedings of DATE'09 Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Nice, April 2009, pp. 215-216.
54. J. Keinert, H. Dutta, F. Hannig, C. Haubelt and J. Teich. *Model-Based Synthesis and Optimization of Static Multi-Rate Image Processing Algorithms*. Proceedings of Design, Automation and Test in Europe (DATE 2009), IEEE Computer Society, Nice, France, April 20-24, pp. 135-140, 2009.
55. M. Glaß, M. Lukasiewycz, C. Haubelt and J. Teich. *Incorporating Graceful Degradation into Embedded System Design*. Proceedings of Design, Automation and Test in Europe (DATE 2009), pp. 320-323, IEEE Computer Society, Nice, France, April 20-24, 2009.
56. M. Lukasiewycz, M. Streubühr, M. Glaß, C. Haubelt and J. Teich. *Combined System Synthesis and Communication Architecture Exploration for MPSoCs*. Proceedings of Design, Automation and Test in Europe (DATE 2009), pp. 472-477, IEEE Computer Society, Nice, France, April 20-24, 2009.
57. J. Gladigau, C. Haubelt, M. Streubühr, J. Teich, A. Schneider, J. Knäblein and M. Lindig. *Testfallgenerierung für SystemC-Designs mit abstrakten Modellbeschreibungen*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Seite 157-166, Berlin, Germany, March 2-4, 2009.
58. F. Reimann, M. Glaß, M. Lukasiewycz, J. Keinert, C. Haubelt and J. Teich. *Symbolic Voter Placement for Dependability-Aware System Synthesis*. In Proceedings of the 6th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 237-242, Atlanta, GA USA, October 19-24 2008.
59. J. Falk, J. Keinert, C. Haubelt, J. Teich and S. Bhattacharyya. *A Generalized Static Data Flow Clustering Algorithm for MPSoC Scheduling of Multimedia Applications*. In Proc. of the 8th ACM & IEEE international conference on Embedded software (EMSOFT'2008), pp. 189-198, Atlanta, Georgia, USA, October 20-22, 2008.
60. J. Keinert, C. Haubelt and J. Teich. *Automatic Synthesis of Design Alternatives for Fast Stream-Based Out-of-Order Communication*. Proceedings of the 2008 IFIP/IEEE WG 10.5 International Conference on Very Large Scale Integration, (VLSI-SoC 2008) pp. 265-270, Rhodes Island, Greece, October 13-15, 2008.
61. J. Gladigau, C. Haubelt and J. Teich. *Symbolic Quasi-Static Scheduling of Actor-Oriented SystemC Models*. Proceedings of Forum on specification & Design Languages 2008 (FDL08), pages 1-6, Stuttgart, Germany, Sep. 23-25, 2008.
62. M. Glaß, M. Lukasiewycz, F. Reimann, C. Haubelt and J. Teich. *Symbolic Reliability Analysis of Self-healing Networked Embedded Systems*. In Proceedings of the 27th International Conference on Computer Safety, Reliability and Security (SAFECOMP 2008), pp. 139-152, Newcastle upon Tyne, UK, September 22-25, 2008.
63. M. Glaß, M. Lukasiewycz, R. Wanka, C. Haubelt and J. Teich. *Multi-Objective Routing and Topology Optimization in Networked Embedded Systems*. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS 2008), pp. 74-81, Samos, Greece, July 21-24, 2008.
64. C. Haubelt, M. Meredith, T. Schlichter and J. Keinert. *SystemCoDesigner: Automatic Design Space Exploration and Rapid Prototyping from Behavioral Models*. In Proceedings of 2008 ACM/EDAC/IEEE Design Automation Conference (DAC 2008), pp. 580-585, Anaheim, CA, USA, June 8-13, 2008.
65. M. Lukasiewycz, M. Glaß, C. Haubelt, J. Teich, R. Regler and B. Lang. *Concurrent Topology and Routing Optimization in Automotive Network Integration*. In Proceedings of the 2008 ACM/EDAC/IEEE Design Automation Conference (DAC 2008), pp. 626-629, Anaheim, CA, U.S.A., June 08-13, 2008.
66. C. Zebelein, J. Falk, C. Haubelt and J. Teich. *Classification of General Data Flow Actors into Known Models of Computation*. In Proc. of the Sixth ACM/IEEE International Conference on

Formal Methods and Models for Codesign (MEMOCODE 2008), pp. 119-128, Anaheim, CA, USA, June 5-7, 2008.

67. M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich. *A Feasibility-preserving Local Search Operator for Constrained Discrete Optimization Problems*. In Proceedings of the 2008 IEEE Congress on Evolutionary Computation (CEC 2008), pp. 1968-1975, Hong Kong, China, June 01-06, 2008.
68. D. Koch, C. Haubelt and J. Teich. *Efficient Reconfigurable On-Chip Buses for FPGAs*. Proceedings 16th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2008), pp. 287-290, Palo Alto, California, April 14-15, 2008.
69. M. Glaß, M. Lukasiewycz, F. Reimann, C. Haubelt and J. Teich. *Symbolic Reliability Analysis and Optimization of ECU Networks*. Proceedings of Design, Automation and Test in Europe (DATE 2008), IEEE Computer Society, pp. 158-163, Munich, Germany, March 10-14, 2008.
70. M. Streubühr, M. Jäntsch, C. Haubelt, J. Teich and A. Schneider. *Semi-Automatic Generation of mixed Hardware-Software Prototypes from Simulink Models*. 11. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Freiburg, Germany, pp. 139-148, March 03-05, 2008.
71. J. Gladigau, F. Blendinger, C. Haubelt and J. Teich. *Symbolische Modellprüfung Aktor-orientierter High-level SystemC-Modelle mit Intervalldiagrammen*. 11. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Freiburg, Germany, pp. 109-118, March 03-05, 2008.
72. J. Keinert, C. Haubelt and J. Teich. *Synthesis of Multi-Dimensional High-Speed FIFOs for Out-of-Order Communication*. Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008), pp. 130-143, Dresden, Germany, February 25-28, 2008.
73. R. Brendle, T. Streichert, D. Koch, C. Haubelt and J. Teich. *Dynamic Reconfiguration of FlexRay Schedules for Response Time Reduction in Asynchronous Fault-Tolerant Networks*. Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008), pp. 117-129, Dresden, Germany, February 25-28, 2008.
74. T. Streichert, M. Glaß, R. Wanka, C. Haubelt and J. Teich. *Topology-Aware Replica Placement in Fault-Tolerant Embedded Networks*. Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008), pp. 23-37, Dresden, Germany, February 25-28, 2008.
75. M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich. *Efficient Symbolic Multi–Objective Design Space Exploration*. In Proceedings of the 13th Asia and South Pacific Design Automation Conference (ASP-DAC 2008), pp. 691-696, Seoul, Korea.
76. J. Keinert, J. Falk, C. Haubelt and J. Teich. *Actor-Oriented Modeling and Simulation of Sliding Window Image Processing Algorithms*. Proceedings of the 2007 IEEE/ACM/IFIP Workshop of Embedded Systems for Real-Time Multimedia (ESTIMEDIA 2007), pp. 113-118, Salzburg, Oct. 4-5, 2007.
77. M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich. *SAT-Decoding in Evolutionary Algorithms for Discrete Constrained Optimization Problems*. In Proceedings of the 2007 IEEE Congress on Evolutionary Computation (CEC 2007), Singapore, Singapore, pp. 935-942, September 25-28, 2007.
78. J. Gladigau, C. Haubelt, B. Niemann and J. Teich. *Mapping Actor-Oriented Models to TLM Architectures*. In Proceedings FDL'07, Forum on specification and Design Languages 2007, Barcelona, Spain, September 18-20, 2007.
79. J. Keinert, C. Haubelt and J. Teich. *Simulative Buffer Analysis of Local Image Processing Algorithms Described by Windowed Synchronous Data Flow*. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, Acoustics, Speech, and Signal Processing (IC-SAMOS VII), Samos (Greece) July 16-19, 2007.
80. B. Niemann and C. Haubelt. *Towards a Unified Execution Model for Transactions in TLM*. In Proceedings of Fifth ACM & IEEE International Conference on Formal Methods and Models for Co-Design (MEMOCODE'07), pp. 103-112, Nice, France, May 30 - June 01, 2007.
81. M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich. *Solving Multiobjective Pseudo-Boolean Problems*. In Proceedings of Tenth International Conference on Theory and Applications of Satisfiability Testing (SAT 2007), Lisbon, Portugal, pp. 56-69, May 28-31, 2007.
82. D. Koch, C. Haubelt, T. Streichert and J. Teich. *Modeling and Synthesis of Hardware-Software Morphing*. In Proceedings of the International Symposium on Circuits and Systems (ISCAS 2007), pp. 2746-2749, New Orleans, LA, U.S.A., May 2007.

83. M. Glaß, M. Lukasiewycz, T. Streichert, C. Haubelt and J. Teich. *Reliability-Aware System Synthesis*. In Proceedings of Design, Automation and Test in Europe (DATE 2007), IEEE Computer Society, Nice, France, pp. 409-414, April 16-20, 2007.
84. M. Glaß, M. Lukasiewycz, T. Streichert, C. Haubelt and J. Teich. *Synthese zuverlässiger und flexibler Systeme*. In Proceedings of Zuverlässigkeit und Entwurf (ZuD 2007), Munich, Germany, pp. 141-148, March 26-28, 2007.
85. M. Lukasiewycz, M. Glaß, C. Haubelt and J. Teich. *Symbolic Archive Representation for a Fast Nondominance Test*. In Proceedings of the Fourth International Conference on Evolutionary Multi-Criterion Optimization (EMO 2007), Sendai, Japan, pp. 111-125, March 5-8, 2007.
86. M. Streubühr, C. Riedel, C. Haubelt and J. Teich. *System Level Modeling and Performance Simulation for Dynamic Reconfigurable Computing Systems in SystemC*. 10. Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen", Erlangen, Germany, pp. 59-68, March 05-07, 2007.
87. D. Koch, C. Haubelt and J. Teich. *Efficient Hardware Checkpointing -- Concepts, Overhead Analysis, and Implementation*. In Proceedings of the 15th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2007), Monterey, CA, pp. 188-196, February 18-20, 2007.
88. G. Bunin, A. Schneider, C. Haubelt, J. Langer and U. Heinkel. *Automatic Test Case Generation with NuSMV*. In Proceedings of the Informatik 2006 - Workshop Modellbasiertes Testen. Dresden, Germany, pp. 262 - 263, October 02-10, 2006.
89. B. Niemann and C. Haubelt. *Formalizing TLM with Communicating State Machines*. In Proceedings Forum on Specification and Design Languages (FDL'06), pp. 285-292, Darmstadt, September 19-22, 2006.
90. J. Falk, C. Haubelt and J. Teich. *Efficient Representation and Simulation of Model-Based Designs in SystemC*. In Proceedings FDL'06, Forum on Design Languages 2006, Darmstadt, Germany, September 19-22, pp. 129 - 134, 2006.
91. T. Streichert, C. Strengert, C. Haubelt and J. Teich. *Dynamic Task Binding for Hardware/Software Reconfigurable Networks*. In Proceedings of SBCCI 2006, pages 38-43, Ouro Preto, Brasil, August 28th - September 1st, 2006.
92. T. Streichert, C. Haubelt and J. Teich. *Multi-Objective Topology Optimization for Networked Embedded Systems*. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS 2006), pp. 93--98, Samos (Greece), July 17-20, 2006.
93. J. Keinert, C. Haubelt and J. Teich. *Modeling and Analysis of Windowed Synchronous Algorithms*. In Proceedings of the 31st International Conference on Acoustics, Speech, and Signal Processing (ICASSP2006), Toulouse (France) May 14-19, 2006.
94. D. Koch, T. Streichert, S. Dittrich, C. Strengert, C. Haubelt and J. Teich. *An Operating System Infrastructure for Fault-Tolerant Reconfigurable Networks*. In Proceedings of the 19th International Conference on Architecture of Computing Systems (ARCS 2006), Frankfurt/Main, Germany, pp. 202-216, March 13-16, 2006.
95. M. Streubühr, J. Falk, C. Haubelt, J. Teich, R. Dorsch and T. Schlipf. *Task-Accurate Performance Modeling in SystemC for Real-Time Multi-Processor Architectures*. In Proceedings of Design, Automation and Test in Europe (DATE 2006), IEEE Computer Society, Munich, Germany, pp. 480-481, March 6-10, 2006.
96. T. Schlichter, M. Lukasiewycz, C. Haubelt and J. Teich. *Improving System Level Design Space Exploration by Incorporating SAT-Solvers into Multi-Objective Evolutionary Algorithms*. In Proceedings of IEEE Computer Society Annual Symposium on VLSI. Karlsruhe, Germany, pp. 309-314, March 2-3, 2006.
97. B. Niemann and C. Haubelt. *Assertion-Based Verification of Transaction Level Models*. In Proceedings of the 9th ITG/GMM/GI Workshop, Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Dresden, Germany, pp. 232-236, February 20-22, 2006.
98. C. Haubelt, M. Jersak, K. Richter, K. Strehl, D. Ziegenbein, R. Ernst, J. Teich and L. Thiele. *SPI-Workbench - Modellierung, Analyse und Optimierung eingebetteter Systeme*. In Proceedings of INFORMATIK 2005 - Informatik LIVE. by Armin B. Cremers, Rainer Manthey, Peter Martini, and Volker Steinhage (Eds.). In Lecture Notes in Informatics. VOL. P-68, No. 2, Bonn, Germany, pp. 693-697, September 19-22, 2005. © Gesellschaft für Informatik, Bonn, Germany, 2005.
99. S. Helwig, C. Haubelt and J. Teich. *Modeling and Analysis of Indirect Communication in Particle Swarm Optimization*. In Proceedings of the 2005 IEEE Congress on Evolutionary Computation, volume 2, pages 1246-1253, Edinburgh, UK, September 2nd-5th, 2005.

100. T. Schlichter, C. Haubelt, F. Hannig and J. Teich. *Using Symbolic Feasibility Tests during Design Space Exploration of Heterogeneous Multi-Processor Systems*. In Proceedings of Application-specific Systems, Architectures and Processors (ASAP). Samos, Greece, pp. 9-14, July 23-25, 2005.
101. T. Schlichter, C. Haubelt and J. Teich. *Improving EA-based Design Space Exploration by Utilizing Symbolic Feasibility Tests*. In Proceedings of Genetic and Evolutionary Computation Conference (GECCO). Washington, DC, pp. 1945-1952, June 25-29, 2005.
102. J. Falk, C. Haubelt and J. Teich. *Representing Models of Computation in SystemC*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen. GI/ITG/GMM-Workshop 2005, Munich, Germany, April 06-07, 2005.
103. T. Dinkel, C. Haubelt, U. Heinkel, T. Schlichter and J. Teich. *Automatische Verifikation von ADeVA-Spezifikationen*. In Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen. GI/ITG/GMM-Workshop 2005, Munich, Germany, April 06-07, 2005.
104. C. Haubelt, J. Gamenik and J. Teich. *Initial Population Construction for Convergence Improvement of MOEAs*. In Evolutionary Multi-Criterion Optimization, Carlos A. Coello Coello, Arturo Hernández Aguirre, and Eckart Zitzler (eds.), Lecture Notes in Computer Science, Vol. 3410, pp. 191-205, Springer, Berlin, Heidelberg, New York, 2005.
105. C. Haubelt. *Automated Model-Based Design Space Exploration of Embedded Systems*. PhD Forum at the Design, Automation and Test in Europe (DATE'05), March 7-11, Munich, Germany, 2005.
106. T. Streichert, C. Haubelt and J. Teich. *Distributed HW/SW-Partitioning for Embedded Reconfigurable Systems*. In Proceedings of DATE 2005, Munich, Germany, pp. 894-895, March 7-11, 2005.
107. T. Streichert, C. Haubelt and J. Teich. *Verteilte HW/SW-Partitionierung für fehlertolerante rekonfigurierbare Netzwerke*. In Proceedings of 17. ITG/GI/GMM Workshop für Testmethoden und Zuverlässigkeit und Fehlertoleranz von Schaltungen und Systemen. Innsbruck, Austria, pp. 50-54, February 27 - March 1, 2005.
108. C. Haubelt, S. Otto, C. Grabbe and J. Teich. *A System-Level Approach to Hardware Reconfigurable Systems*. In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05). Shanghai, China, pp. 298-301, January 18-21, 2005.
109. T. Streichert, C. Haubelt and J. Teich. *Online Hardware/Software Partitioning in Networked Embedded Systems*. In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05). Shanghai, China, pp. 982-985, January 18-21, 2005.
110. C. Haubelt. *Design Space Exploration for Distributed Hardware Reconfigurable Systems*. In Field-Programmable Logic and Applications by Jürgen Becker, Marco Platzner, and Serge Vernalde (Eds.). In Lecture Notes in Computer Science, Vol. 3203, p. 1171, Springer, Berlin, Heidelberg, 2004.
111. C. Haubelt, D. Koch and J. Teich. *Basic OS Support for Distributed Reconfigurable Hardware*. In Proceedings of the International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'04), Samos, Greece, July 19-21, published as Springer Lecture Notes in Computer Science (LNCS), volume 3133, pages 30-38, 2004.
112. C. Haubelt and J. Teich. *Accelerating Design Space Exploration*. In Proceedings of 5th International Conference on ASIC (ASICON 2003), pp. 79-84, Beijing, China, October 21-24, 2003.
113. C. Haubelt, D. Koch and J. Teich. *ReCoNets: Modeling and Implementation of Fault Tolerant Distributed Reconfigurable Hardware*. In Proceedings of the 16th Symposium on Integrated Circuits and Systems Design (SBCCI2003), pp. 343-348, São Paulo, Brazil, September 8-11, 2003.
114. R. Feldmann, C. Haubelt, B. Monien and J. Teich. *Fault Tolerance Analysis of Distributed Reconfigurable Systems Using SAT-Based Techniques*. In Proceedings of 13th International Conference on Field Programmable Logic and Applications, pp. 478-487, Lisbon, Portugal, September 1-3, 2003.
115. C. Haubelt, D. Koch and J. Teich. *Basic OS Support for Distributed Reconfigurable Hardware*. In Proceedings of the Third International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'03), pp. 18-22, Samos, Greece, July 21-23, 2003, ISBN 90-807957-1-2.
116. C. Haubelt, S. Mostaghim, J. Teich and A. Tyagi. *Solving Hierarchical Optimization Problems Using MOEAs*. In Evolutionary Multi-Criterion Optimization, Carlos M. Fonseca, Peter J. Fleming, Eckart Zitzler, Kalyanmoy Deb, and Lothar Thiele (eds.), Lecture Notes in Computer Science, Vol. 2632, pp. 162-176, Springer, Berlin, Heidelberg, New York, 2003.

117. C. Haubelt, J. Teich, R. Feldmann and B. Monien. *SAT-Based Techniques in System Synthesis*. In Proceedings of Design, Automation and Test in Europe (DATE 2003), Norbert Wehn and Diederik Verkest, IEEE Computer Society, Munich, Germany, pp. 1168-1169, March 3-7, 2003.
118. C. Haubelt and J. Teich. *Accelerating Design Space Exploration Using Pareto-Front Arithmetics*. In Proceedings ASP-DAC 2003, Asia and South Pacific Design Automation Conference, pp. 525-531, Kitakyushu, Japan, January 21-24, 2003.
119. C. Haubelt, J. Teich, K. Richter and R. Ernst. *System Design for Flexibility*. In Proc. DATE 2002, Design, Automation and Test in Europe, IEEE Computer Society Press, pp. 854-861, Paris, France, March 4-8, 2002.
120. C. Haubelt, J. Teich, K. Richter and R. Ernst. *Modellierung Rekonfigurierbarer Systemarchitekturen*. GI / ITG / GMM Workshop - Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Tuebingen, Germany, Shaker Verlag, pp. 163-171, February 25-27, 2002.

Non-Reviewed Journals:

1. C. Haubelt, J. Teich and R. Dorsch. *Entdecke die Möglichkeiten*. In Design&Elektronik (8):22-27, 2008, WEKA.

Non-Reviewed Conference Papers:

1. M. Geilen, J. Falk, C. Haubelt, T. Basten, B. Theelen, S. Stuijk. *Performance Analysis of Weakly-Consistent Scenario-Aware Dataflow Graphs*. In Proceeding of the Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, U.S.A.,pp. 393-397, 2014.
2. C. Haubelt, F. Ludwig, L. Middendorf, and C. Zebelein. *Using Stream Rewriting for Mapping and Scheduling Data Flow Graphs onto Many-Core Architectures*. In Proceeding of the Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, U.S.A., pp. 1431-1435, 2013.
3. P. Kutzer, M. Streubühr, C. Haubelt, J. Teich and A. von Schwerin. *Actor-oriented Modeling of Industrial Ethernet in the Automation Domain Using SystemC*. Proceedings of the Embedded World Conference, Nuremberg, Germany, 2011.
4. M. Streubühr, M. Jäntsch, C. Haubelt and J. Teich. *From Model-based Design to Virtual Prototypes for Automotive Applications*. In Proceedings of the Embedded World Conference, Nuremberg, Germany, March 03-05, 2009.
5. A. Schneider, G. Bunin, C. Haubelt and U. Heinkel. *Automatic Test Generation with Model Checking Techniques*. In Software Quality in Service-Oriented Architectures Proceedings of the Conference on Quality Engineering in Software Technology (CONQUEST2006). Berlin, Germany, pp. 307 - 318, September 27-29, 2006.
6. T. Dinkel, C. Haubelt, U. Heinkel, J. Knäblein, T. Schlichter, S. Schock and J. Teich. *Comparison of Techniques for the Automatic Verification of ADeVA Specifications*. In Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2005). Dresden, Germany, April 13-14, 2005.
7. C. Haubelt and J. Teich. *Modeling and Analysis of Distributed Reconfigurable Hardware*. In Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2004), pp. 106-111, Dresden, Germany, April 19-20, 2004.
8. M. Jersak, K. Richter, D. Ziegenbein, R. Ernst, C. Haubelt, F. Slomka and J. Teich. *SPI-Workbench für die Analyse eingebetteter Systeme*. Workshop: Modelle, Werkzeuge und Infrastrukturen zur Unterstützung von Entwicklungsprozessen, Aachen, Germany, March 20-22, 2002.

Invited Talks:

1. F. Grützmacher, B. Beichler, B. Theelen, and C. Haubelt. *Performance Estimation of Template-based Gesture Recognition on Multi- Core Architectures Using Scenario-Aware Dataflow Graphs*. At Integrating Dataflow, Embedded computing and Architecture (IDEA'2016) Workshop. April 11, Vienna, Austria, 2016.
2. C. Haubelt: *Gesture Detection On-Loading for the Next Generation Sensor Subsystems*. At TISU: Transfer to Industry and Start-Ups, January 19, Prague, Czech Republic, 2016.
3. C. Haubelt. *A Novel Task Mapping Approach Based on Stream Rewriting*. Invited Talk at KTH Stockholm, December 5, Stockholm, Sweden, 2014.

4. A. Nitsch, B. Beichler, F. Golatowski, and C. Haubelt. *Towards a Model-based Design for ETCS Speed and Distance Monitoring*. At Internationale Fachmesse für Verkehrstechnik - Innovative Komponenten, Fahrzeuge, Systeme (InnoTrans 2014), September 24, Berlin, Germany, 2014.
5. C. Haubelt. *A Novel Task Mapping Approach Based on Stream Rewriting*. Invited Talk at Eindhoven Technical University, October 24, Eindhoven, The Netherlands, 2013.
6. R. Kiesel, O. Löhlein, M. Streubühr, J. Teich, and C. Haubelt. *SystemC-based Actor-oriented Modeling of an Automotive Pedestrian Detection System*. At 24. European SystemC User's Group Meeting, September 13, Oldenburg, Germany 2011.
7. C. Haubelt. *Synthesis and Optimization of Heterogeneous Multi-Core Systems*. Invited Talk at Eindhoven Technical University, December 9, Eindhoven, The Netherlands, 2010.
8. C. Haubelt. Accelerated *Design Space Exploration for Heterogeneous MPSoCs Using Symbolic Techniques.* At ARTIST Design Map2MPSoC 2010 Workshop, June 29, St. Goar, Germany, 2010.
9. C. Haubelt. *ESL Synthesis Across Hardware/Software Boundaries*. Invited Talk at the Workshop on Compiler-Assisted System-On-Chip Assembly (CASA'09), Embedded Systems Week 2009, October 10, Grenoble, France, 2009.
10. C. Haubelt. *SystemCoDesigner: An ESL Synthesis Methodology*. DATE´09 Friday Workshop: The Future of ESL Synthesis, Nice, France, 2009. Invited Talk.
11. M. Streubühr, C. Haubelt and J. Teich. *System Level Performance Simulation for Heterogenous Multi-Processor Architectures*. 1st Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), in conjunction with the 4th HiPEAC Conference, Paphos, Cyprus, January 25, 2009.
12. C. Haubelt. *An Actor-Oriented Design Methodology Using SystemC*. Invited talk at IBM Future Technology Forum, Böblingen, Germany, December 12, 2008.
13. C. Haubelt. *SystemCoDesigner - Map2MPSoC 2008*. Invited talk at ARTIST Design Map2MPSoC 2008 Workshop, Düsseldorf, Germany, November 28, 2008.
14. C. Haubelt. *SystemCoDesigner - A Methodology for an Early Assessment of Design Options*. Invited talk at the Fraunhofer Institut für Integrierte Schaltungen (FhG-IIS), Erlangen, Germany, November 25, 2008.
15. C. Haubelt, J. Falk, C. Zebelein, J. Keinert, J. Teich and S. Bhattacharyya. S*ystemCoDesigner - An ESL Design Methodology Based on the FunState MoC*. Talk at 2nd Artist Workshop on Models of Computation and Communication, Eindhoven, The Netherlands, July 3, 2008.
16. C. Haubelt. *SystemCoDesigner: Automatic Design Space Exploration and Rapid Prototyping from Behavioral Models*. Talk at Center of Embedded Computer Systems, Irvine, CA, USA, June 13, 2008.
17. C. Haubelt. *SystemCoDesigner - A Methodology for an Early Assessment of Design Options*. Invited Talk at the 1. ILP-Summit Embedded Systems Institute, Nuremberg, Germany, February 27, 2008.
18. C. Haubelt. *Substantiating Early Design Decisions by Automatic Design Space Exploration*. Invited Talk at TU Chemnitz. December 12, Chemnitz, Germany, 2007.
19. J. Falk, J. Gladigau, C. Haubelt, J. Keinert, T. Schlichter, M. Streubühr and J. Teich. *Substantiating Early Design Decisions by Automatic Design Space Exploration*. Talk at 16. European SystemC Users Group Meeting, September 18, Barcelona, Spain, 2007.
20. J. Falk, J. Gladigau, C. Haubelt and J. Teich. *SysteMoC - Verification and Refinement of Actor-Based Models of Computation*. Talk, ARTIST2 Workshop on MoCC - Models of Computation and Communication, November 16-17, Zurich, Switzerland, 2006.
21. C. Haubelt. *SystemCoDesigner - Eine Entwurfsmethodik für SystemC-Beschreibungen*. Invited Talk, Siemens Medical Solutions, July 17, Erlangen, Germany, 2006.
22. C. Haubelt. *SystemCoDesigner - Eine Entwurfsmethodik für SystemC-Beschreibungen*. Invited talk, Institute of Computer and Communication Network Engineering, TU Braunschweig, April 28, Braunschweig, Germany, 2006.
23. C. Haubelt. *SystemCoDesigner - Eine Entwurfsmethodik für SystemC-Beschreibungen*. Invited Talk, Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und Systeme OFFIS, April 24, Oldenburg, Germany, 2006.
24. J. Teich, C. Haubelt, D. Koch and T. Streichert. *Concepts for Self-Adaptive Automotive Control Architectures*. DATE'06 Friday Workshop Future Trends in Automotive Electronics and Tool Integration, Conference Design Automation and Test in Europe, March 10, 2006, Munich, Germany.
25. C. Haubelt. *Eine modellbasierte Entwurfsmethodik für SystemC*. Invited talk, Professur Schaltkreis- und Systementwurf, TU Chemnitz, February 1, Chemnitz, Germany, 2006.

26. C. Haubelt. *SystemCoDesigner: Entwurfsraumexploration für SystemC-Beschreibungen*. Invited Talk, Fraunhofer Institut für Integrierte Schaltungen (FhG-IIS), December 12, Erlangen, Germany, 2005.
27. C. Haubelt. *A System-Level Approach to Automated Model-Based Design Space Exploration*. Invited Talk at the Computer Engineering and Networks Laboratory (TIK), ETH Zurich, March 31, Zurich, Switzerland, 2005.
28. C. Haubelt. *Introduction to Hardware-Software-Co-Design*. Invited Talk, Fraunhofer Institut für Integrierte Schaltungen (FhG-IIS), May 03, Erlangen, Germany, 2004.
29. C. Haubelt. *Hierarchische Mehrzieloptimierung Eingebetteter Systeme*. Invited Talk, Oldenburger Forschungs- und Entwicklungsinstitut für Informatik-Werkzeuge und Systeme OFFIS, September 16, Oldenburg, Germany, 2003.

Tutorials:

1. C. Haubelt. *Entwurf und virtuelles Prototyping*. Kompaktkurs "Eingebettete Systeme", May 7th, Rostock, Germany, 2014.
2. C. Haubelt. *Integrated Finite State Machine and Dataflow Modeling*. Lecture at the Summer School on Models for Embedded Signal Processing Systems, September 2nd, Leiden, The Netherlands, 2010.
3. C. Haubelt. *Designing Heterogeneous MPSoCs*. DAC'10 Friday Tutorial "SystemC for Holistic System Design with Digital Hardware, Analog Hardware, and Software". June 18th, Anaheim, CA, U.S.A., 2010.
4. C. Haubelt. *Designing Multi-Processor Systems-on-Chip*. Embedded Tutorial at the 22nd International SoC Conference. September 10th, Belfast, Northern Ireland, UK, 2009.
5. J. Teich and C. Haubelt. *Principles: Analysis, Optimization and Exploration*. DATE´09 Monday Tutorial: System-Level Modeling, Analysis and Synthesis of Embedded Multi-Core Designs, Nice, France, 2009. Invited Talk.
6. C. Haubelt. *Practice: ESL Case Studies (Motion-JPEG Example)*. DATE´09 Monday Tutorial: System-Level Modeling, Analysis and Synthesis of Embedded Multi-Core Designs, Nice, France, 2009. Invited Talk.
7. C. Haubelt and B. Niemann. *Formalizing and Verifying SystemC TLMs*. Talk at FDL Industrial Workshop on Verification of Complex Systems, September 19, Barcelona, Spain, 2007.
8. C. Haubelt. *Hardware-Software-Partitioning with SystemC*. In Master Course Modern Design Techniques with SystemC at the Design, Automation and Test in Europe (DATE'04), February 20, Paris, France, 2004.