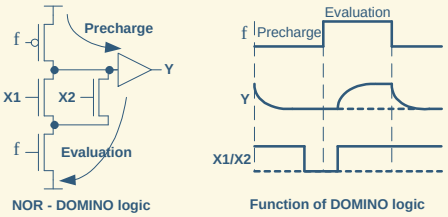
Dynamic Single-rail Self-timed Logic Structures for Power Efficient Synchronous Pipelined Designs

Frank Grassert, Dirk Timmermann

Single-Rail DOMINO Logic

Why? **Fast!**



Single-Rail

e.g. DOMINO

+ Lower power consumption
+ About half area than dual-rail
+ Smaller output load (fast)
+ Less clock transistors

– Only non-inverting logic functions
– Completion detection for self-timed structures

Idea: Combination of single-rail logic with self-timed structures

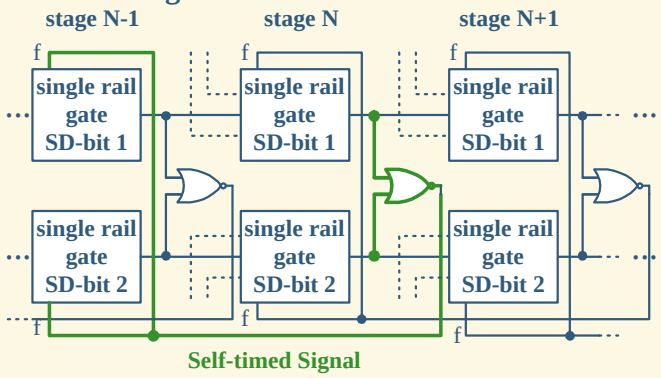
Redundant Numbers for Self-timed Structures:

Digit	Representation	Self-timed-Signal
-1	10	Evaluate
0	01	Evaluate
1	11	Evaluate
free	00	Precharge

Table 1: Signed-Digit representation

- Simplifies completion detection
- Ensures the change of at least one bit

Single-Rail Self-timed Structures



Results:

+ Power, area and delay reduction
+ Reduced clock load
– Only small timing differences between parallel paths allowed
– Intensive timing calculations necessary

	Stat. CMOS	DOMINO	CD-Domino	Single-rail Self-timed
Delay (D)	1	0,6	0,4	0,5
Area	1	1,6	1,5	1
Power (P)	1	2,6	2,3	1,8
P*D	1	1,6	0,9	**0,9**

Table 2: Comparison of rough relative values for different logic styles.

Sechen, Clock-Delayed Domino for Dynamic Circuit Design. Trans. on VLSI 2000; Grassert, Single-Rail Self-timed Logic Circuits in Synchronous Designs. MWSCAS 2002.

Lower Power-Delay-Product!

UNIVERSITY OF ROSTOCK

Institute of Applied Microelectronics and Computer Science