Advance VLSI Design (Module 24151) Phase 3

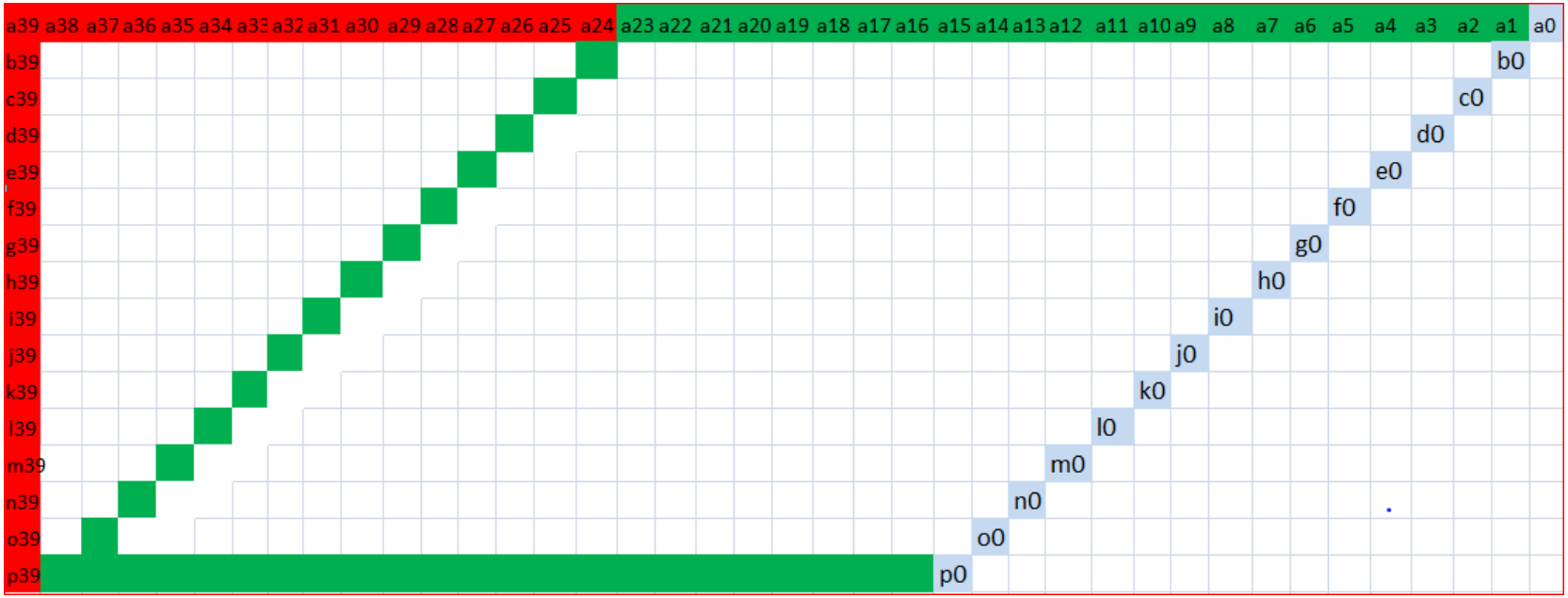
Hooma Amjad

Aim of Phase 3 Task

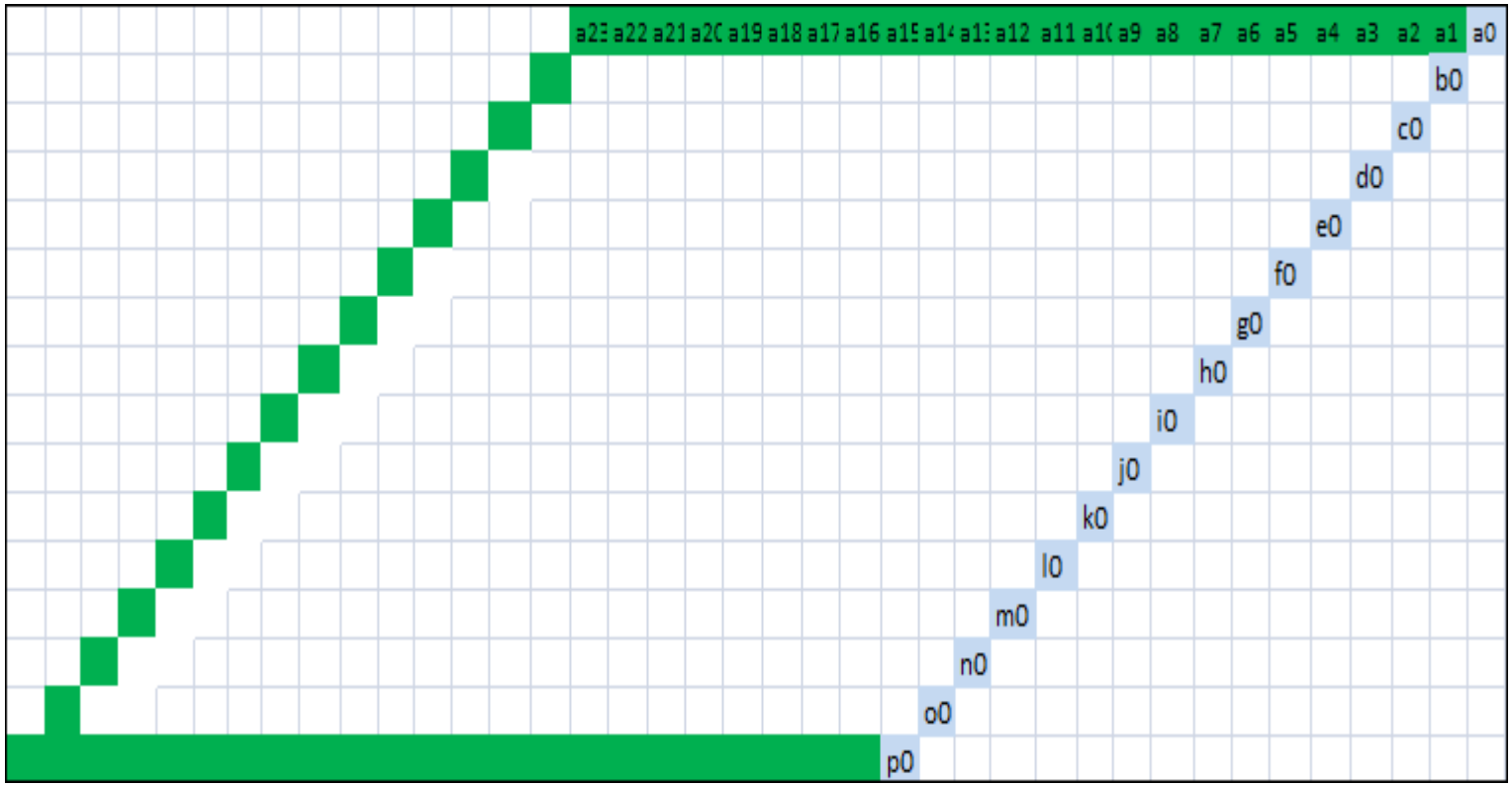
Final FPGA Design

Design and Architecture

Signed Wallace Tree Multiplier



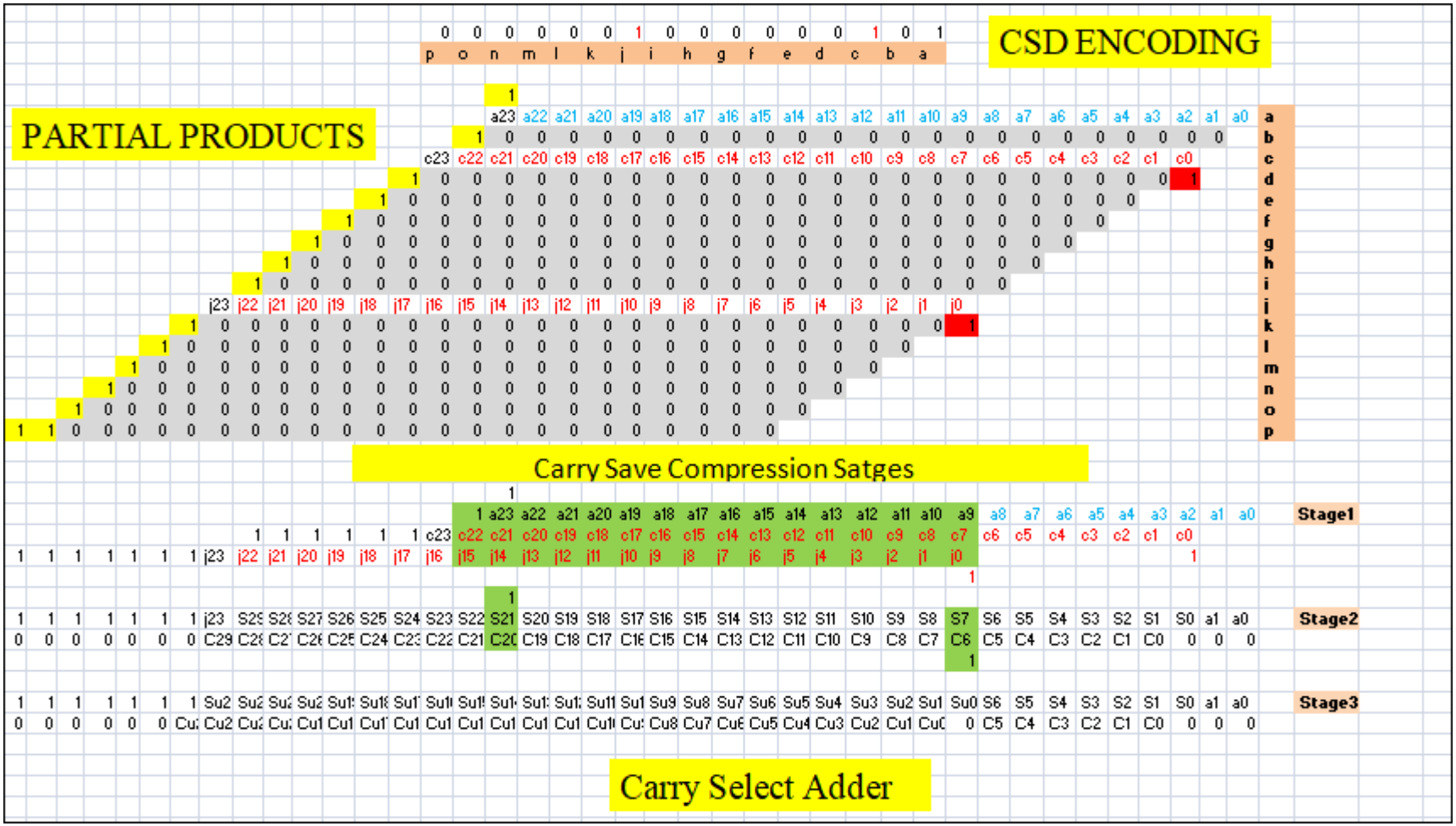
Improved Wallace Tree Multiplier

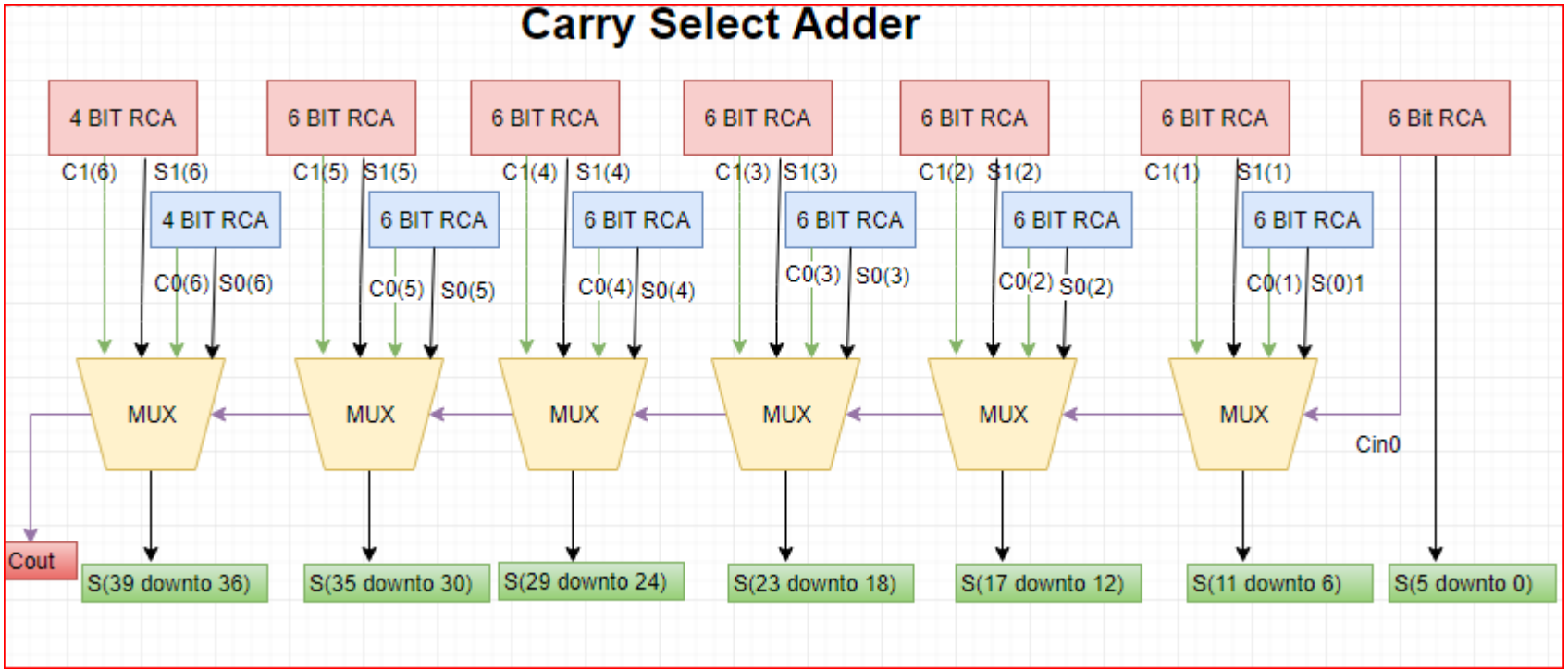


CSD Encoded Wallace Tree Multiplier

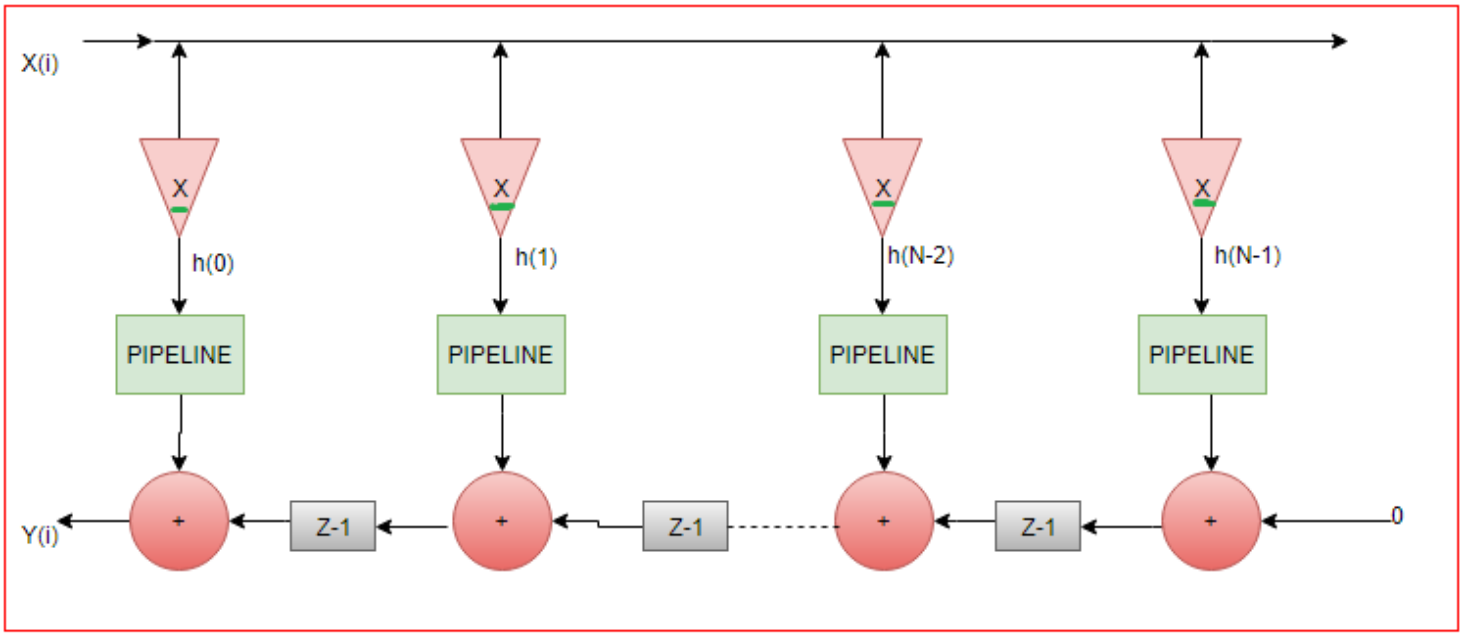
Reduced Partial Products.

Multiplier Internal Structure

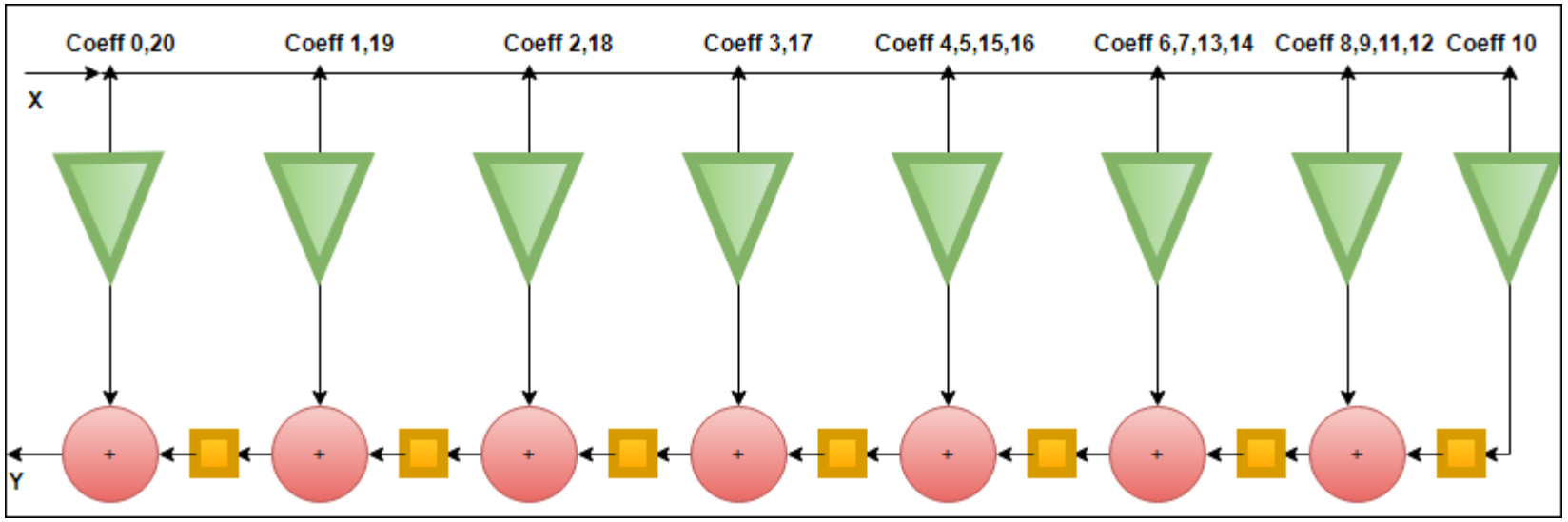



Carry Select Adder
4 BIT RCA
6 BIT RCA
6 BIT RCA
6 BIT RCA
6 BIT RCA
6 BIT RCA
6 Bit RCA
C1(6)
S1(6)
C1(5)
S1(5)
C1(4)
S1(4)
C1(3)
S1(3)
C1(2)
S1(2)
C1(1)
S1(1)
4 BIT RCA
6 BIT RCA
6 BIT RCA
6 BIT RCA
6 BIT RCA
6 BIT RCA
C0(6)
S0(6)
C0(5)
S0(5)
C0(4)
S0(4)
C0(3)
S0(3)
C0(2)
S0(2)
C0(1)
S(0)1
MUX
MUX
MUX
MUX
MUX
MUX
Cin0
Cout
S(39 downto 36)
S(35 downto 30)
S(29 downto 24)
S(23 downto 18)
S(17 downto 12)
S(11 downto 6)
S(5 downto 0)

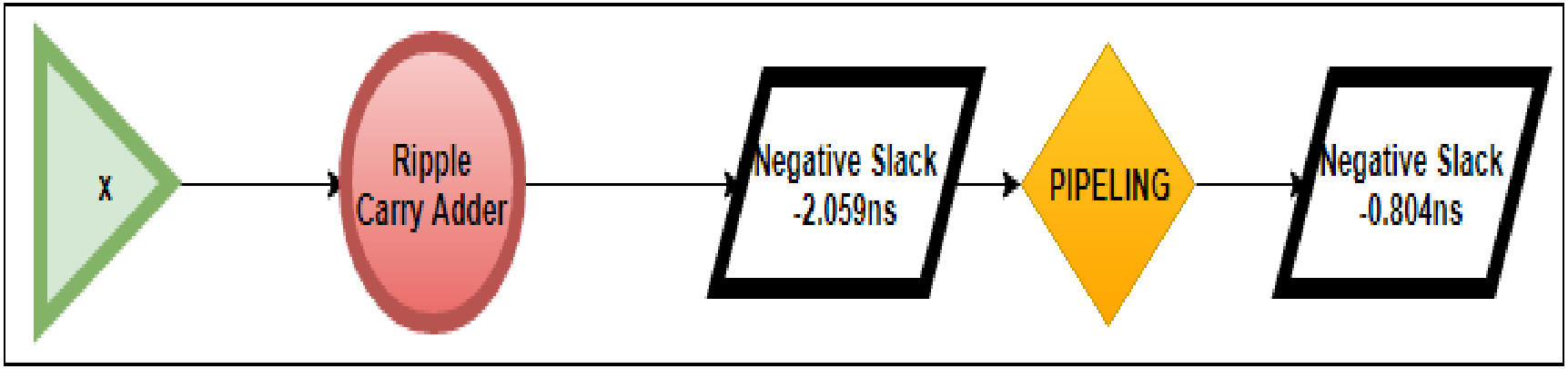
Pipelined Direct form II
Phase 2



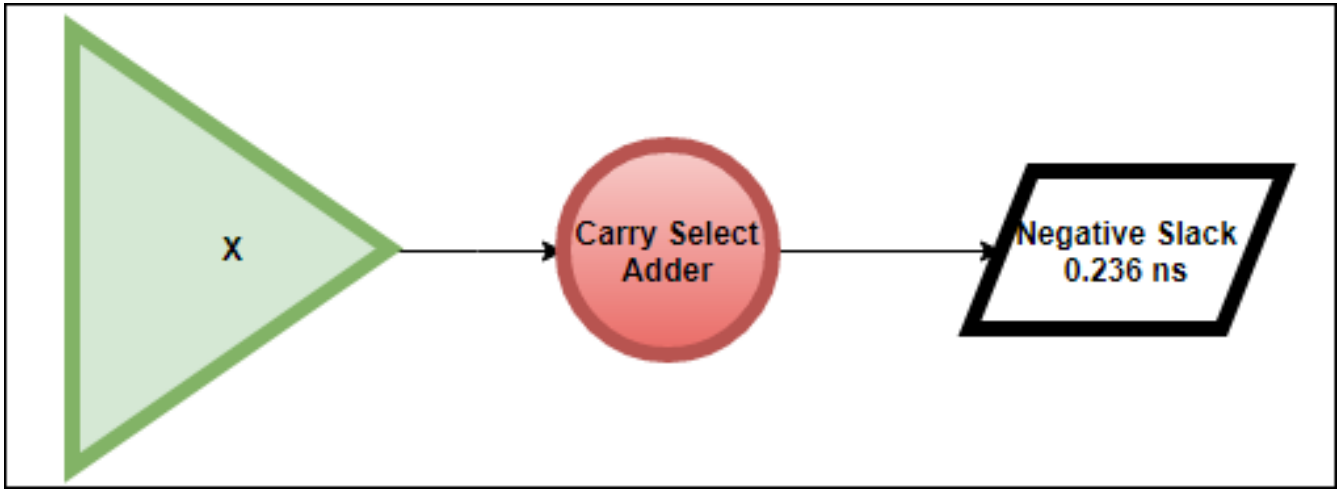
Term Sharing



Issues


x
Ripple Carry Adder
Negative Slack -2.059ns
PIPELING
Negative Slack -0.804ns

Solution

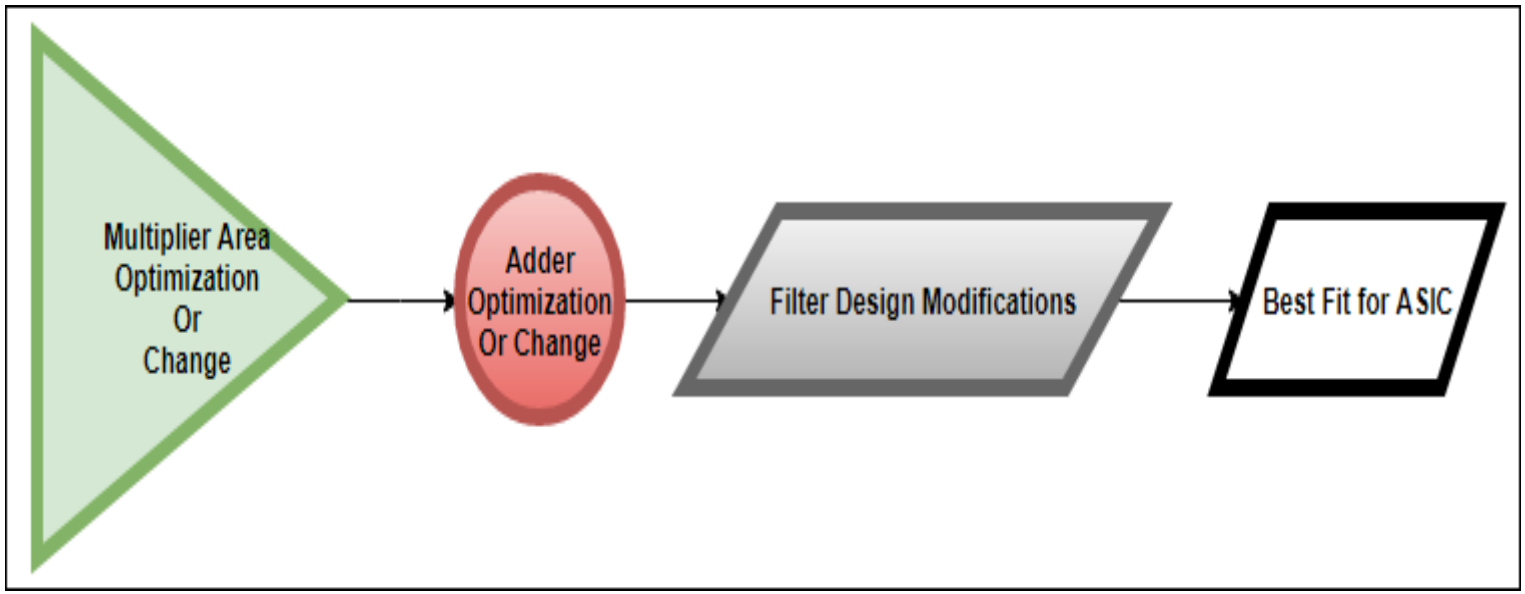


Design Values Comparison

Phase 2	
Frequency	100MHz
Area	**LUT: 4134 / FF: 2148**
# Pipeline Satges	**2**

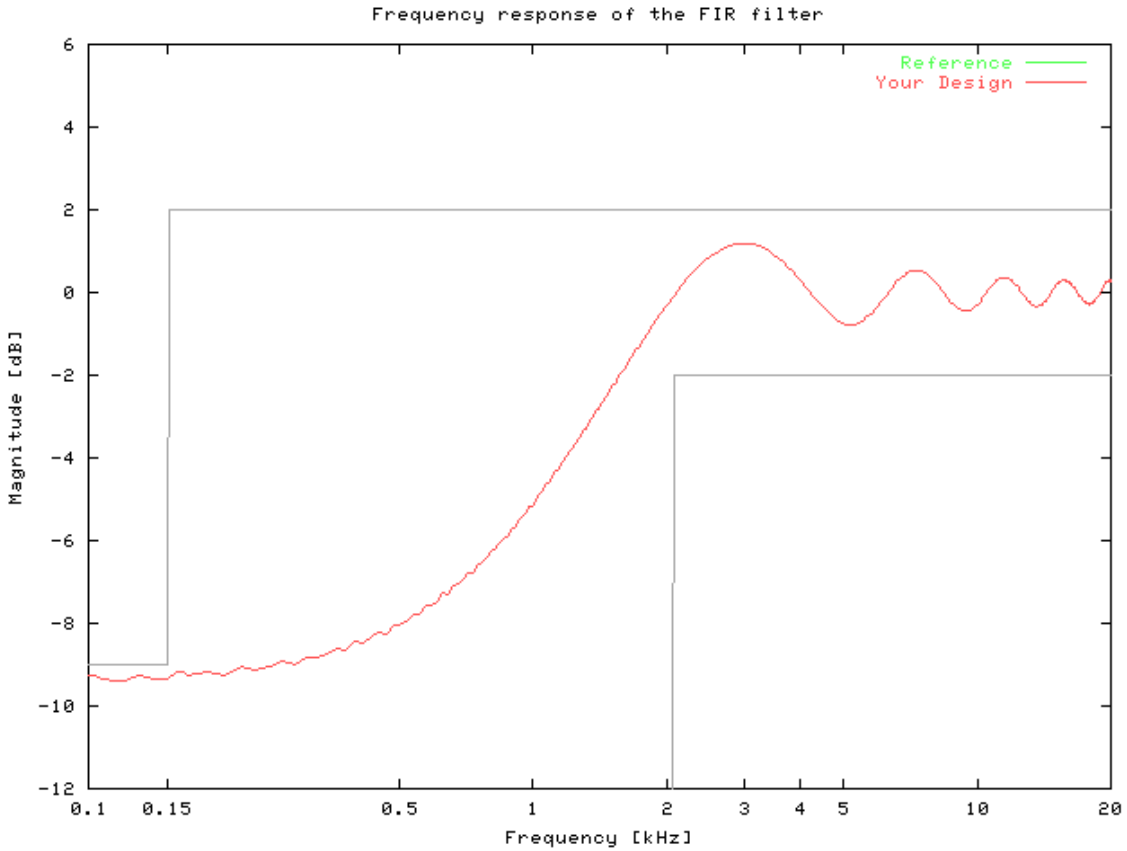
Phase 3	
Frequency	100MHz
Area	**LUT: 2413 / FF:835**
# Pipeline Satges	**0**

Further Improvements



Result

- Worst Negative Slack : 0.236 ns



THANK YOU

QUESTIONS?