Universität Rostock Traditio et Innovatio

Institut für Angewandte Mikroelektronik und Datentechnik

# Advanced VLSI (Project)

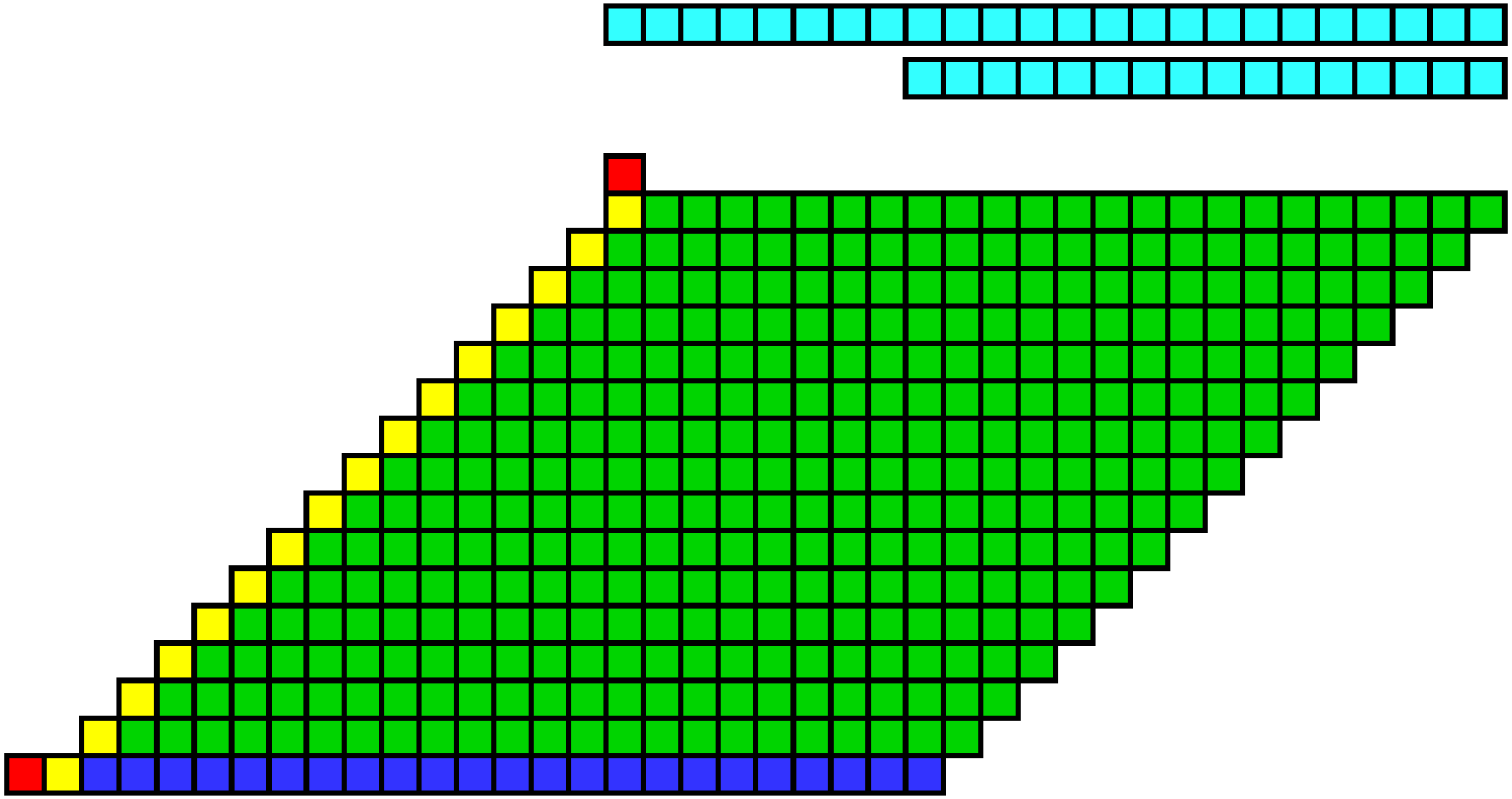
## Module (24513)

*Obaid Ullah Shah*

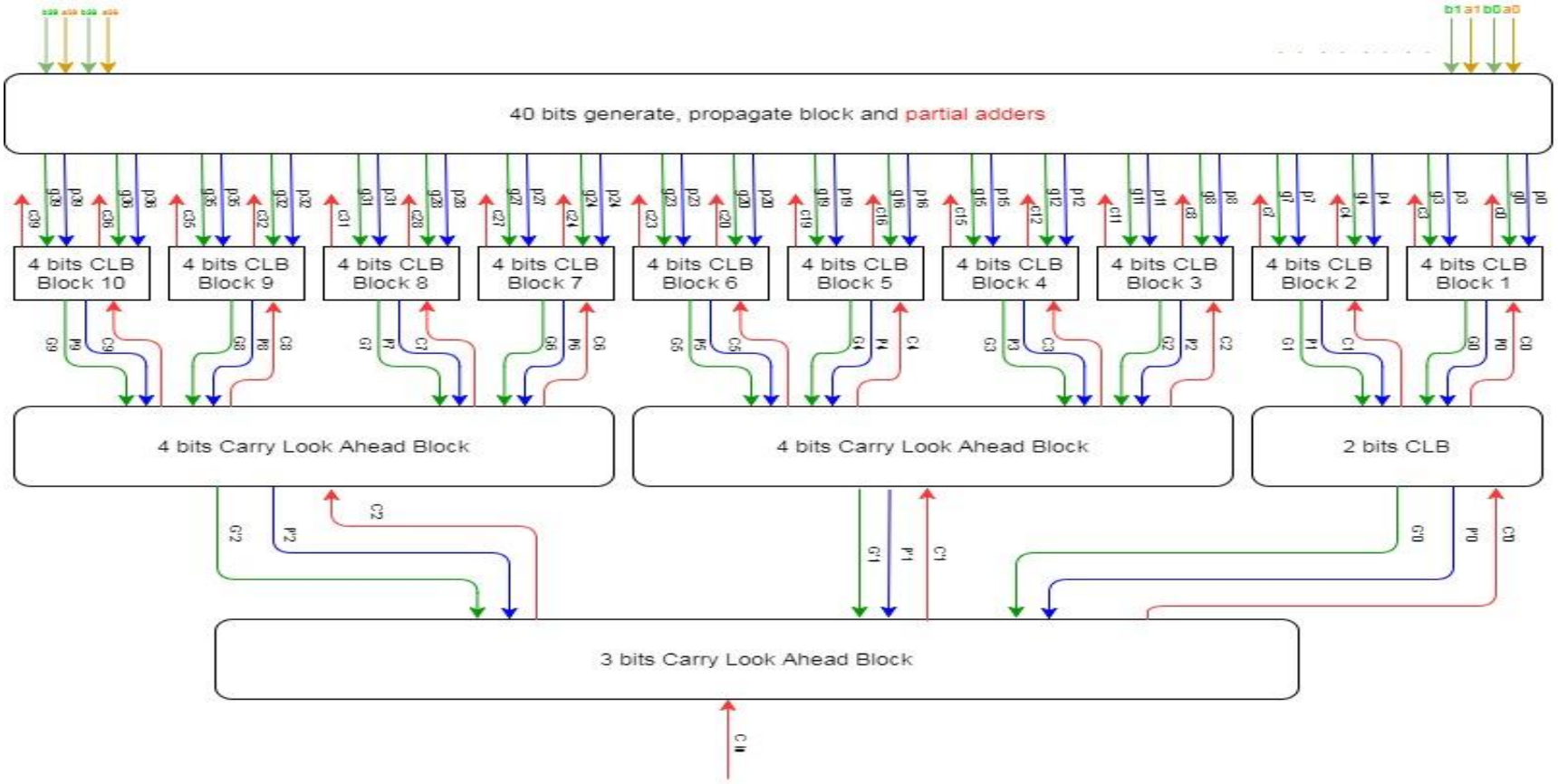
# TASK – 3 :

## Optimization and Testing of FIR Filter Design on a ZedBoard Evaluation Platform

# Logic used in Multiplier

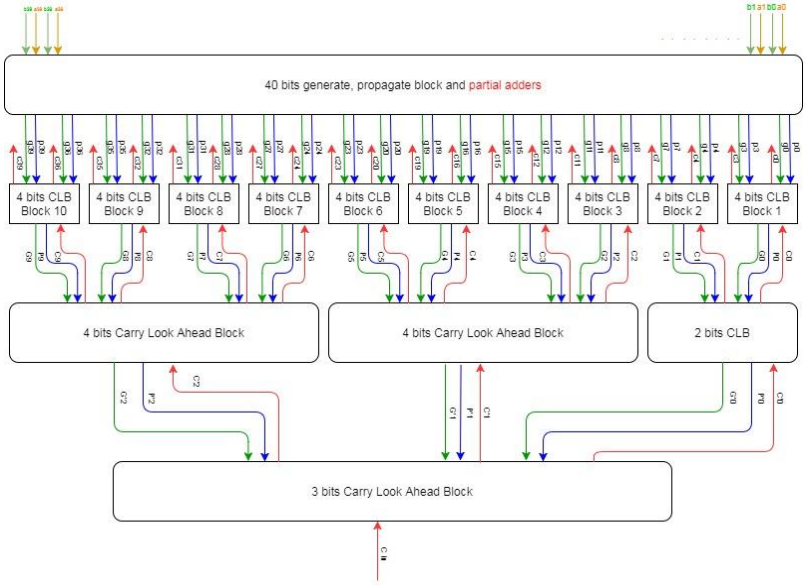


# Fixed Size CLA with Partial Adders

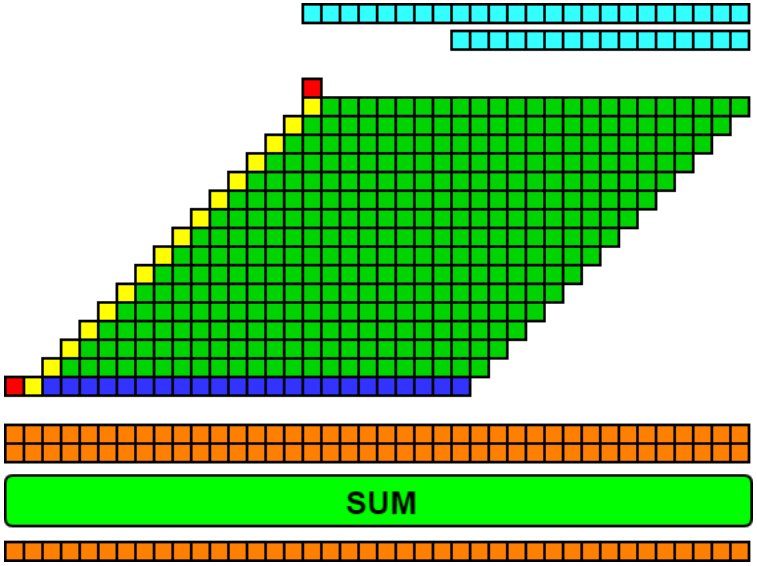


# FIR Filter Design 1

## Fixed Group CLA

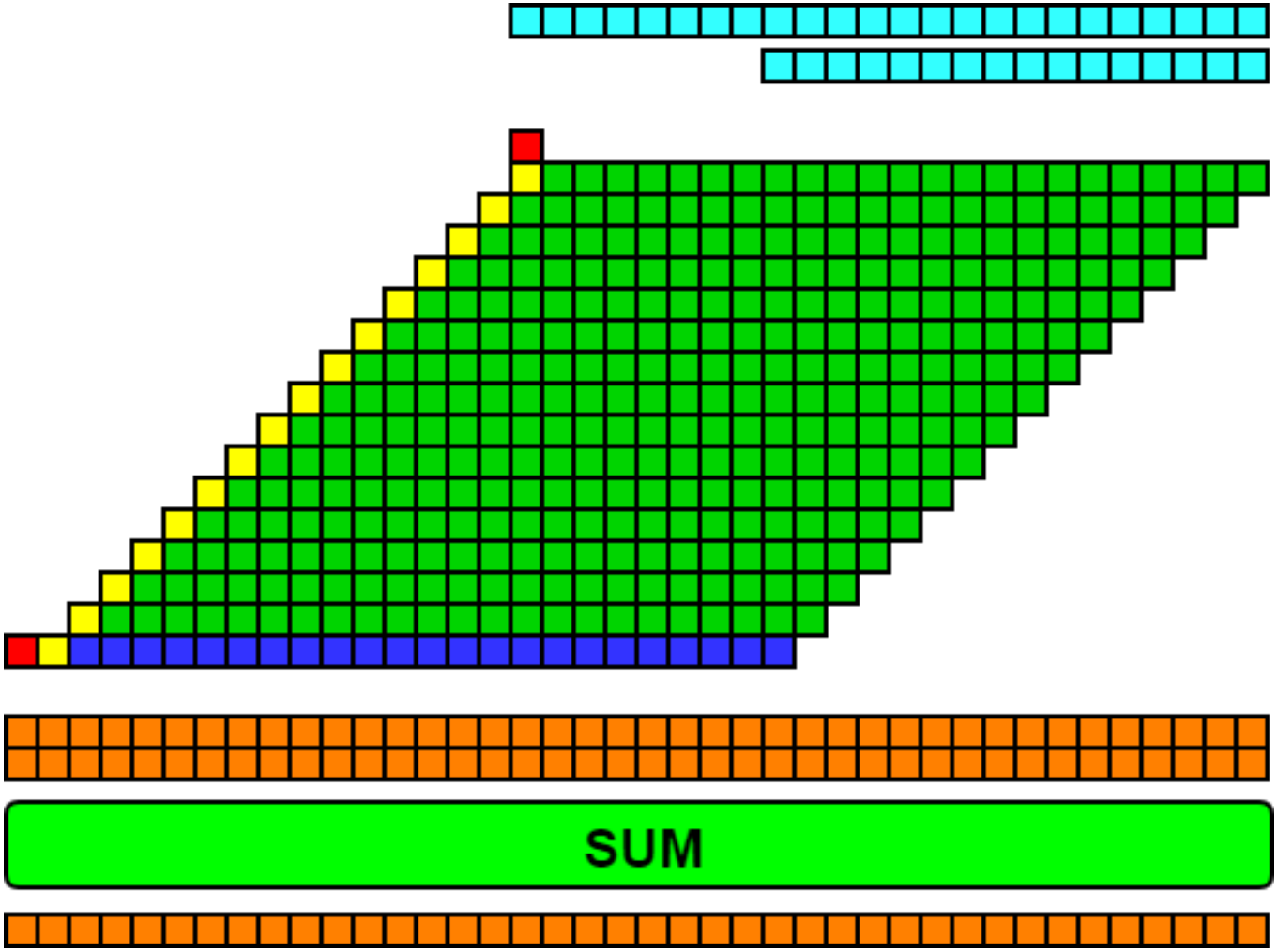



## Multiplier with 2 pipelining

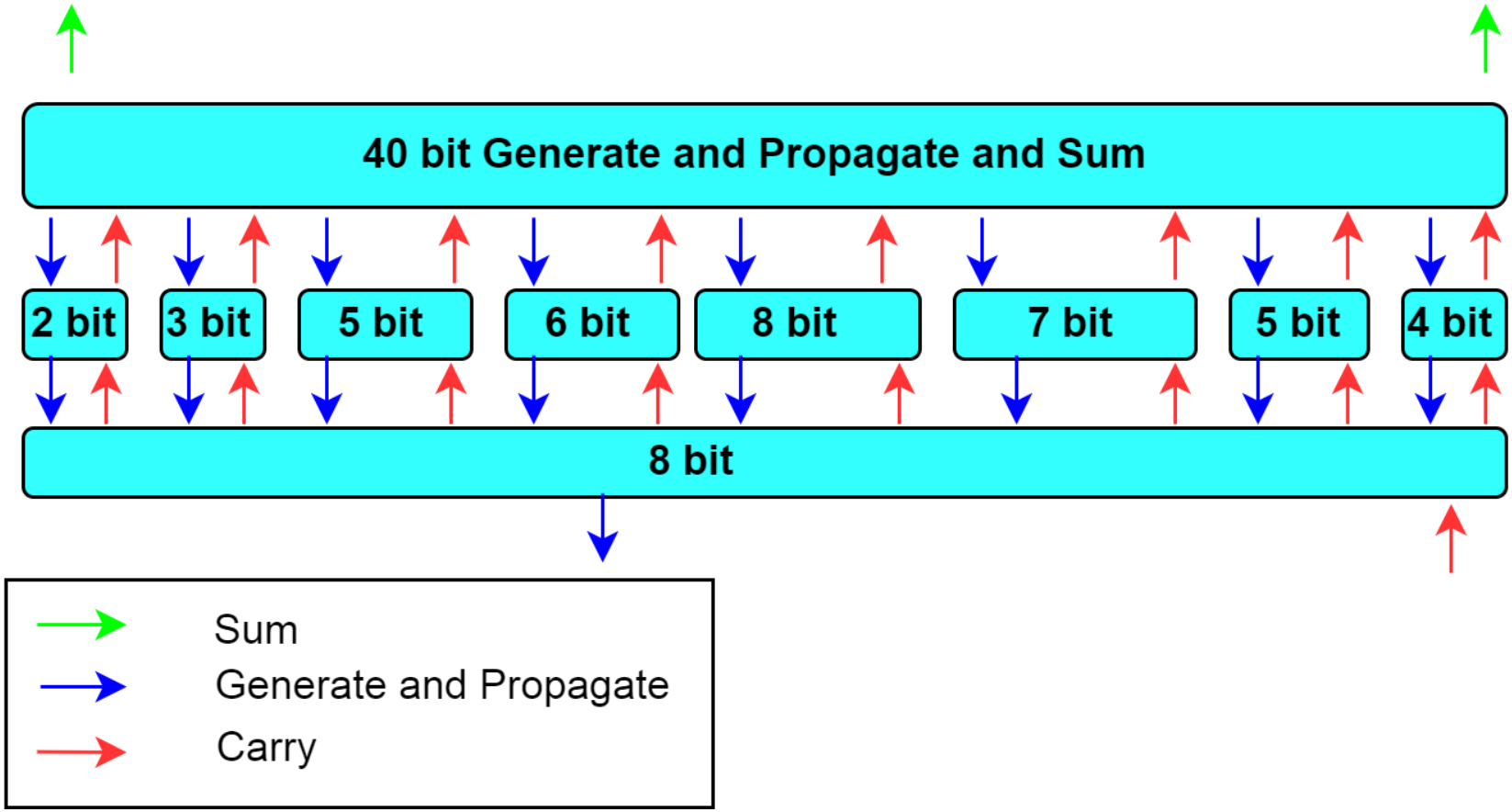



| WNS | LUT | FF |
|---|---|---|
| 2.143 | 3505 | 1529 |

# Final Multiplier with two pipelining



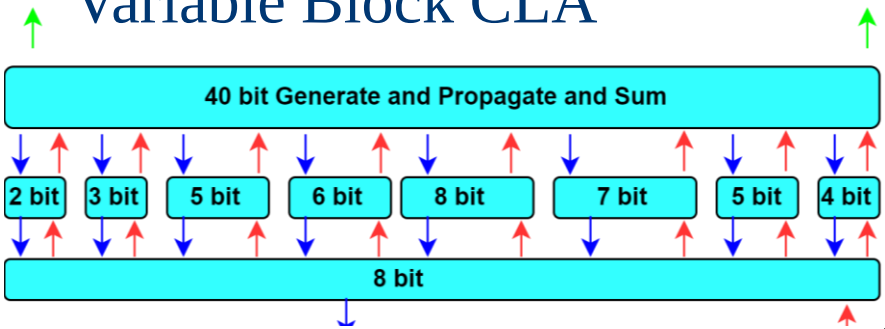
# CLA with variable CLB size

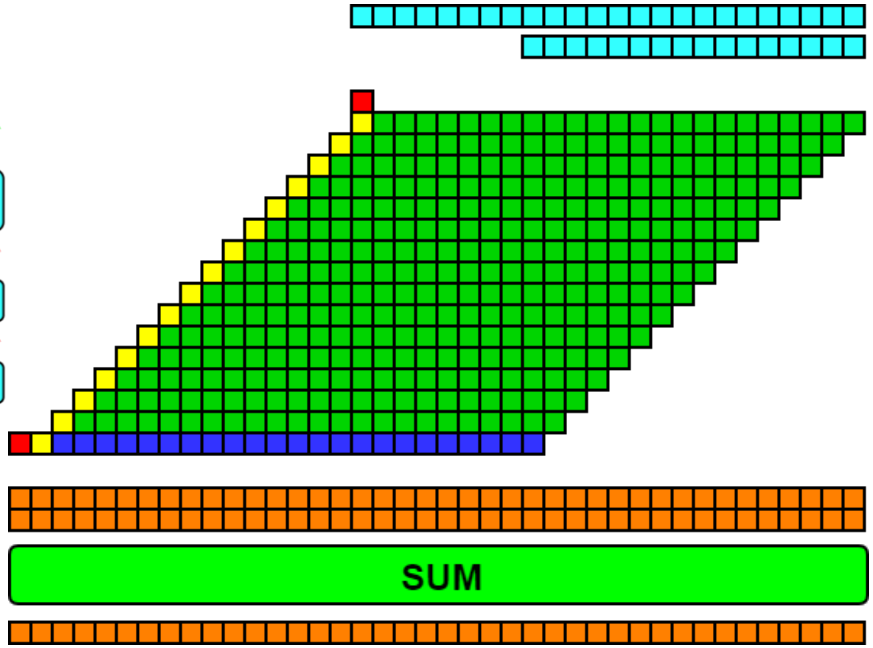


# FIR Filter Design 2

## Multiplier with 2 pipelining

## Variable Block CLA



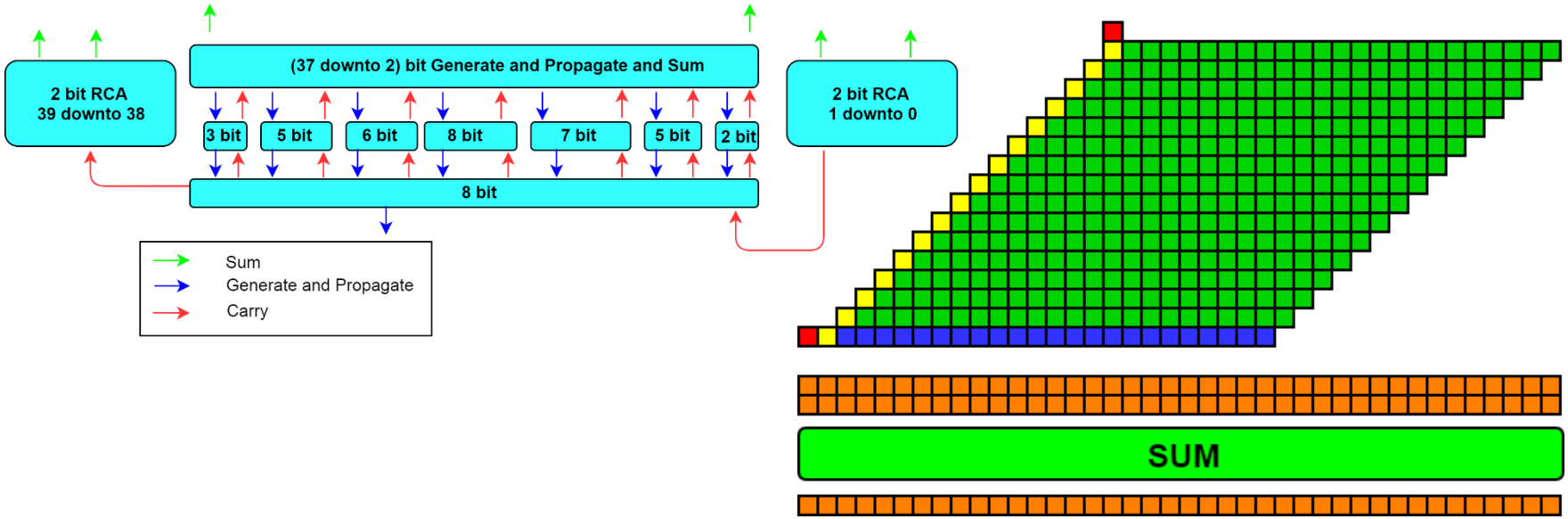




| WNS | LUT | FF |
|---|---|---|
| 0.768 | 5853 | 2170 |

# FIR Filter Design 3

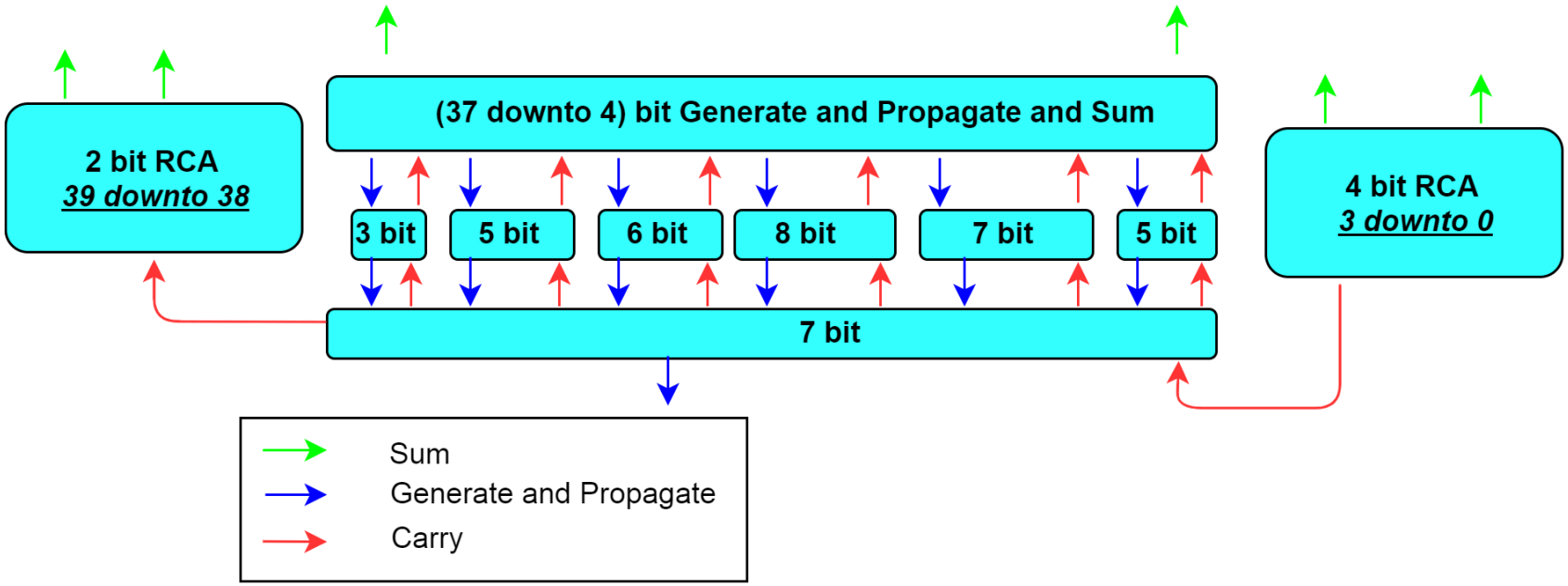
## Multiplier with 2 pipelining

Variable Block CLA with 4 bit RCA



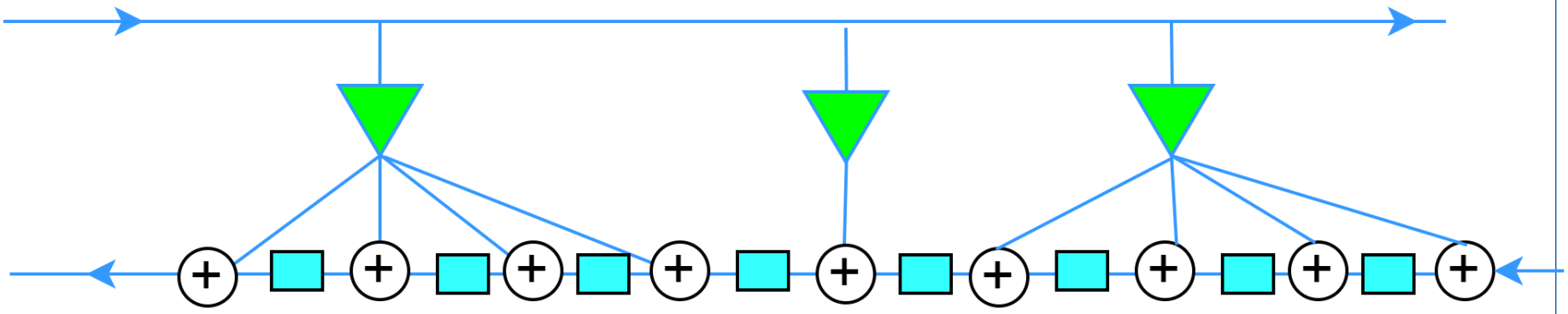

| WNS | LUT | FF |
|---|---|---|
| 1.367 | 5654 | 2153 |

# Variable Group CLA with 6 bit RCA

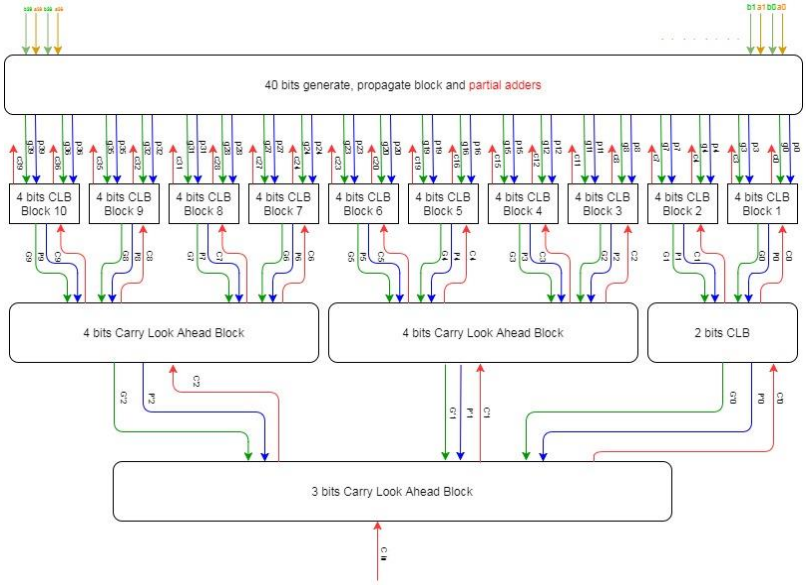


# Modified Coefficient Array

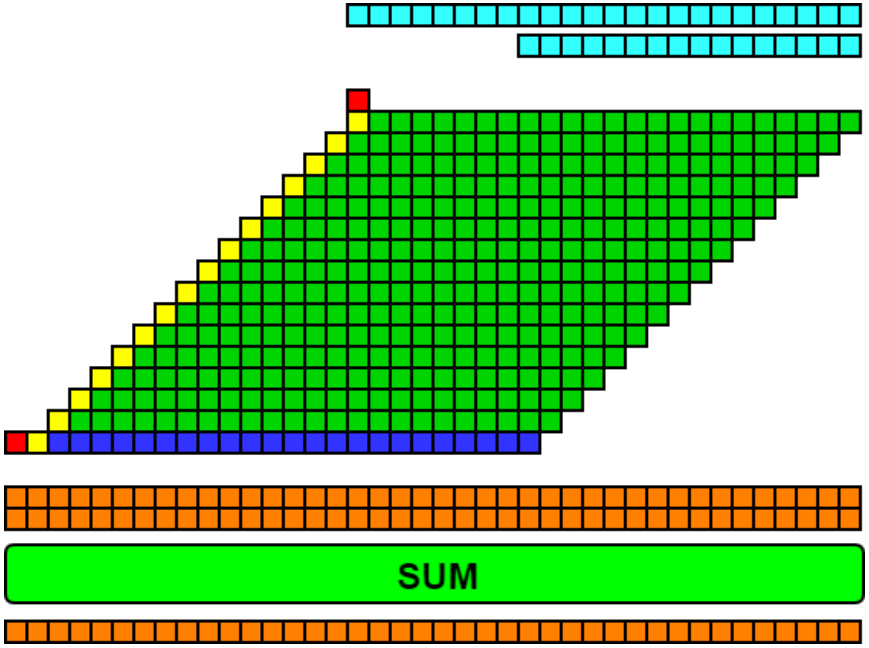
0 =20 , 1=19 , 2=18 , 3=17 , 4=5=15=16 ,
6=7=13=14 , 8=9=11=12 , 10



# FIR Filter Design 8




## Multiplier with 2 pipelining



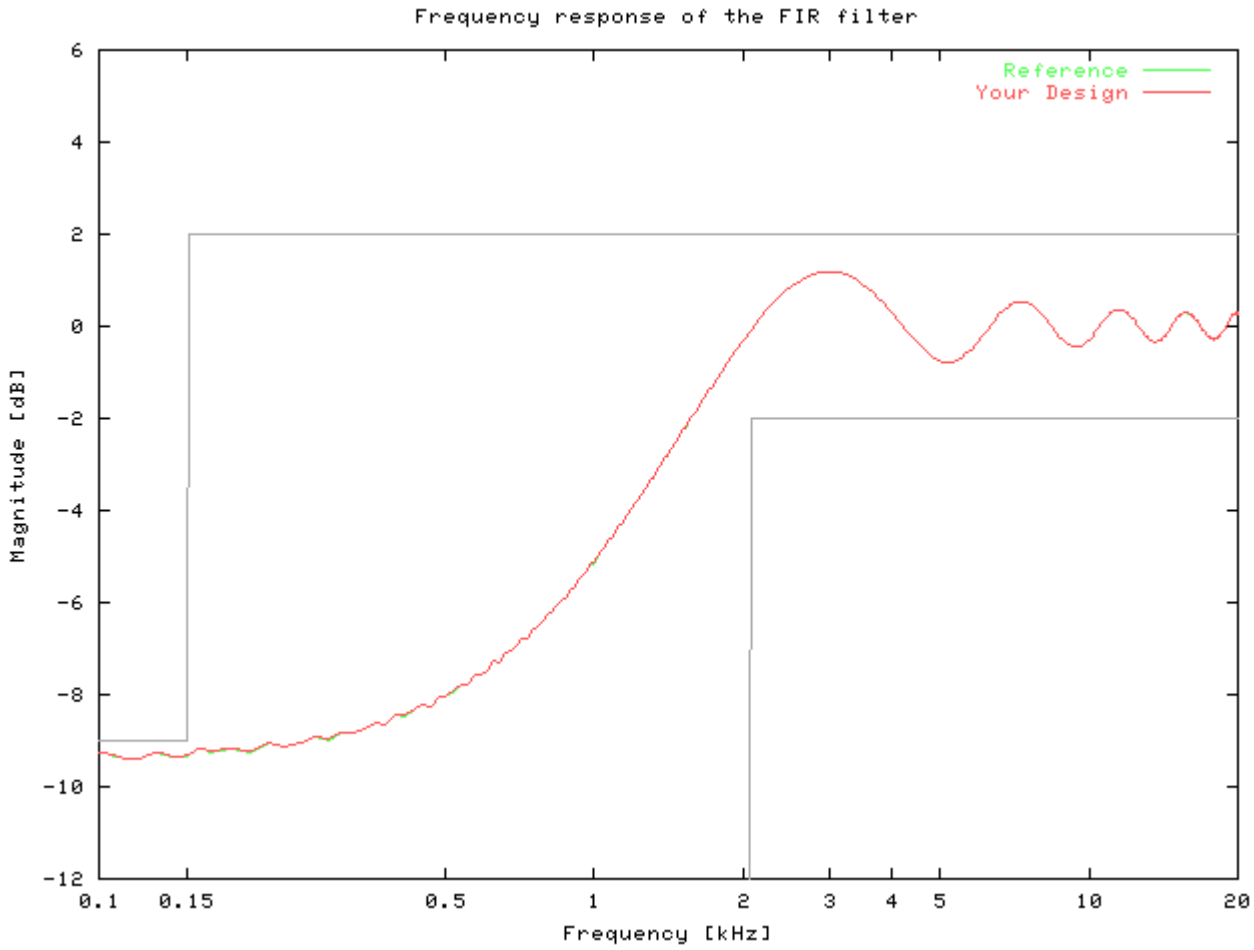

| WNS | LUT | FF |
|---|---|---|
| 2.143 | 3505 | 1529 |
| 1.97 | 3502 | 1529 |

# Observations

| WNS | LUT | FF |
|---|---|---|
| 1.962 | 4041 | 1438 |
| 2.143 | 3505 | 1529 |

| Values for FPGA | |
|---|---|
| Frequency | 154 MHz |
| Area (LUTs and FFs) | 5034 |
| Pipelines | 3 |
| Attenuation | -9.172396 |
| Metric | 7.19023629E-11 |

# Frequency Response



# Further Optimization to reduce Area

- Design of multiplier for fixed Canonical Signed Digits (CSD) as an input from coefficient array of filter. (Work under progress)

# THANK YOU