



Selected Topics in VLSI Design (Module 24513)

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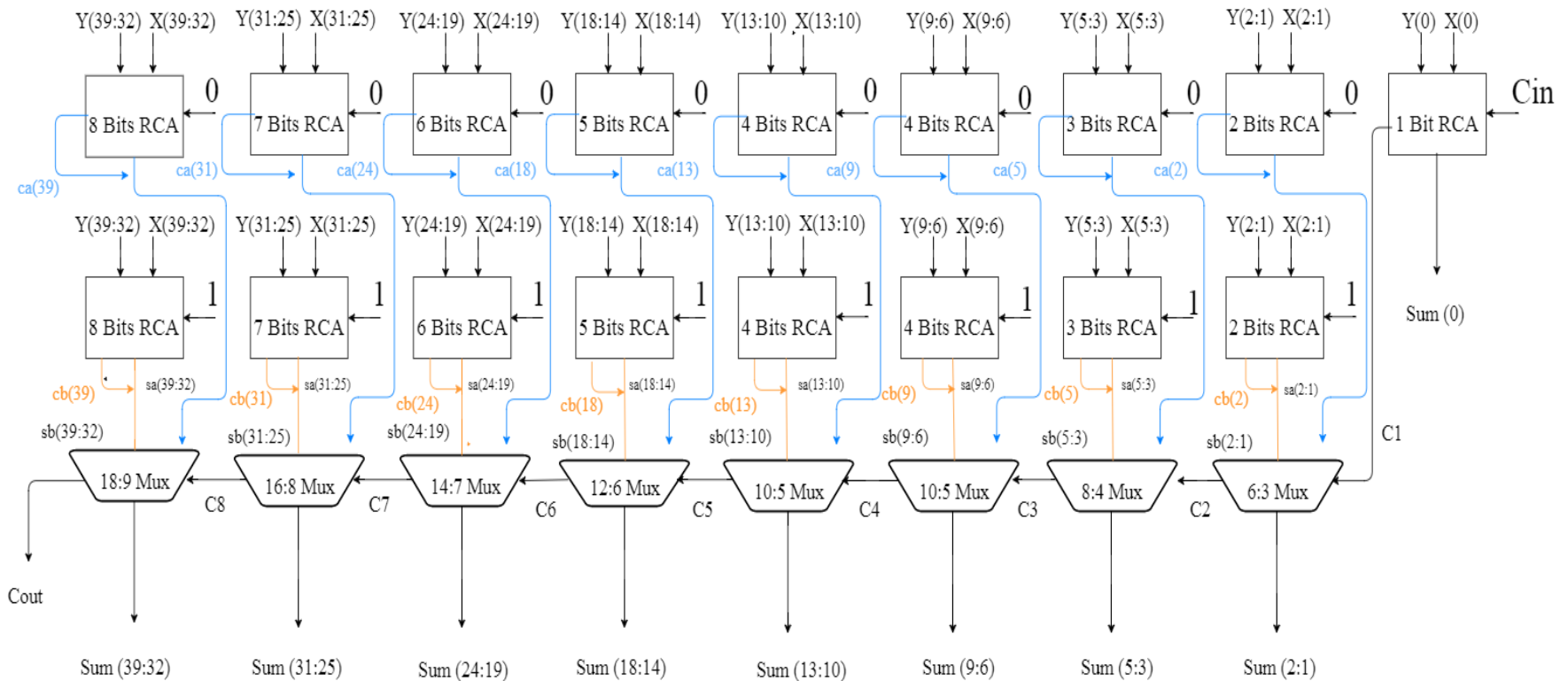
Project Member

Ahmed Aftab Mirza

Presentation on Task 3

Architectural Optimization & Testing your design
on a ZedBoard evaluation Platform

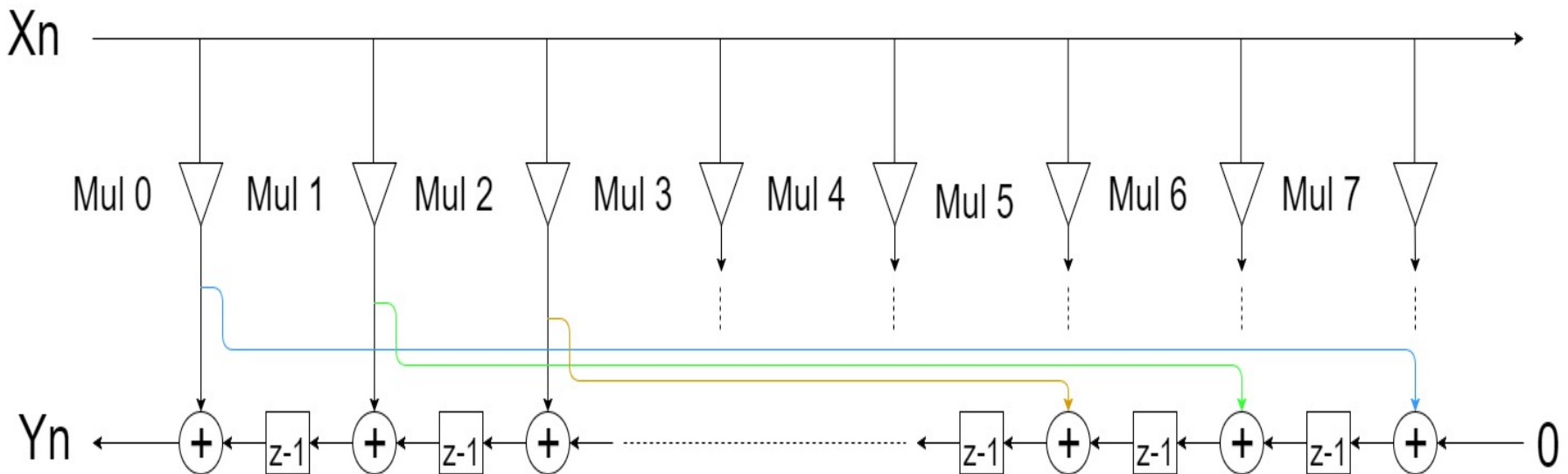
Carry Select Adder Implementation



Block Diagram of 40 Bit Adders

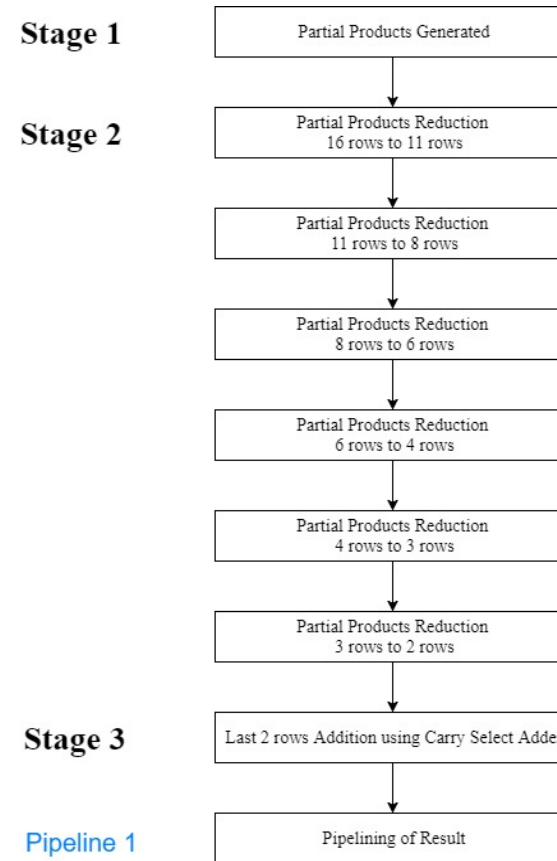
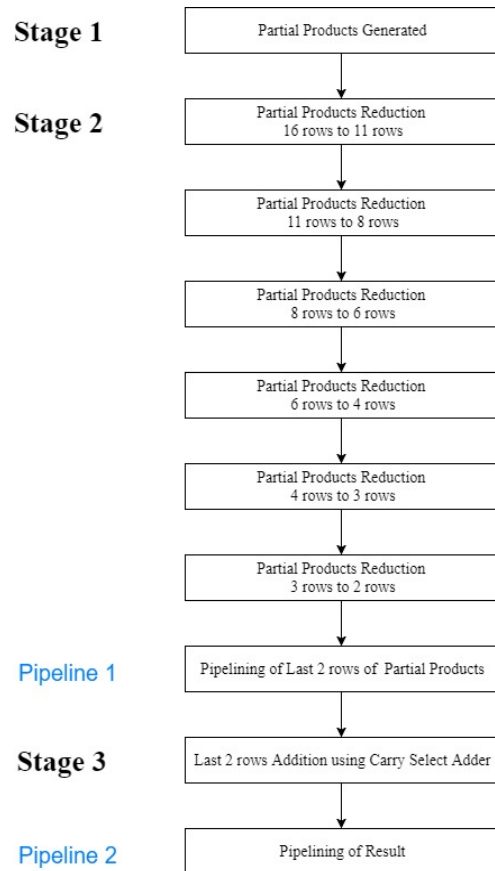
Similar Coefficients - Multiplier Reduction

Coefficient 0,20 (same)	Coefficient 1,19 (same)	Coefficient 2,18 (same)	Coefficient 3,17 (same)	Coefficient 4,5,15,16 (same)	Coefficient 6,7,13,14 (same)	Coefficient 8,9,11,12 (same)	Coefficient 10
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Similar Coefficient (Term Sharing)

Reducing Pipelining in Multiplier



Block Diagram of Multiplication Process with Pipelining

Block Diagram of Multiplication Process with Pipelining

Results Improvement

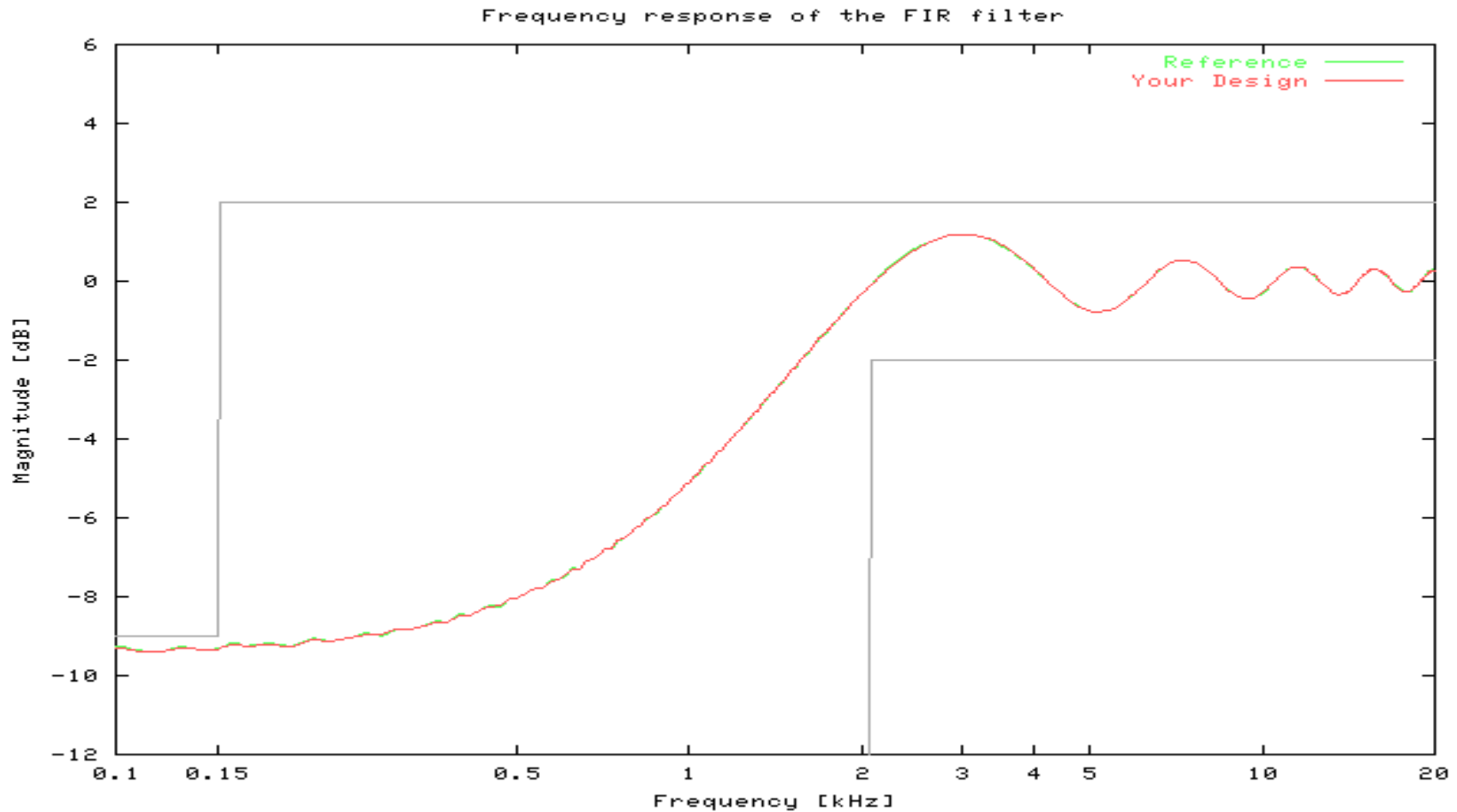
- Previous Result

Wns	0.248
Area (LUT + FF)	$(5438+1485) = 6923$

- Current Results

Frequency	103.5 MHz
Wns	0.344
Area (LUT + FF)	$(3411+1106) = 4517$
Attenuation	-9.182454
Metric	$-9.963421186 \text{ e-}11$
# Pipeline	3

Frequency Response of the FIR Filter



Further Optimization

Reducing Area

- Currently Working on Modified Baugh Wooley Multiplier.
- CSD.



Thank You