

Selected Topics in VLSI Design (Module 24513)

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Aim of Task 3

Presentation of results for an optimized design

Design Of Multiplier

Wallace Tree Multiplier

STAGE 1

Partial Product Generation

Partial Product Reduction
16 Rows to 11 Rows

Partial Product Reduction
11 Rows to 8 Rows

Partial Product Reduction
6 Rows to 4 Rows

Partial Product Reduction
6 Rows to 4 Rows

Partial Product Reduction
4 Rows to 3 Rows

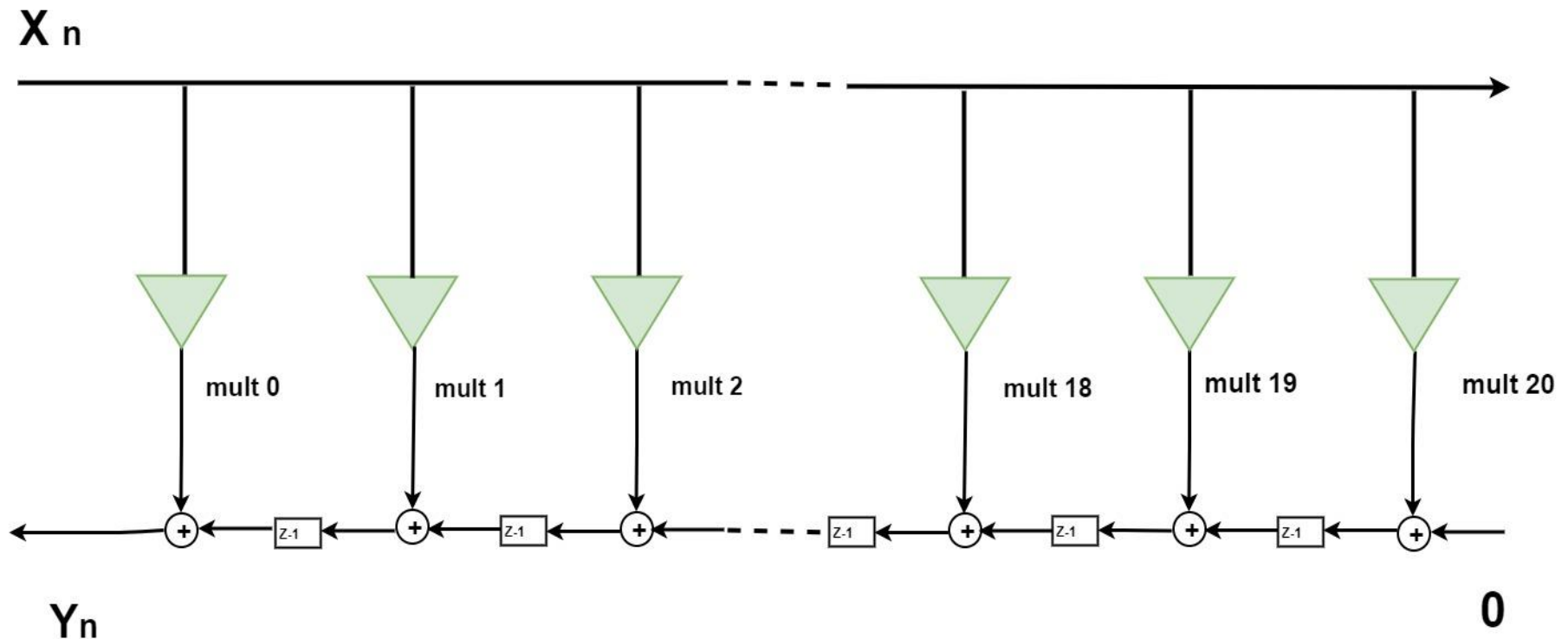
Partial Product Reduction
3 Rows to 2 Rows

STAGE 2

STAGE 3

Addition Of Last 2 Rows by Using
Carry Select Adder

Implementation Direct Form ii



Lookup Table

5400

Flip Flop

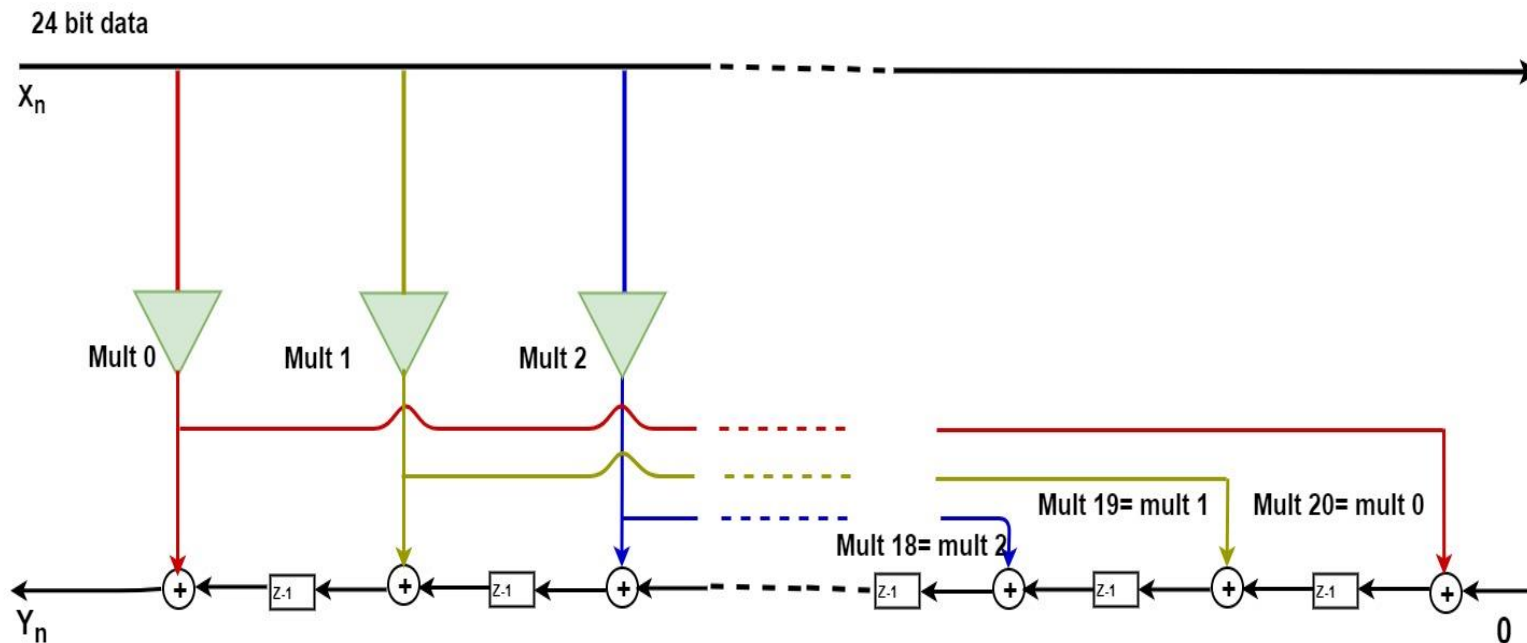
1458

Metric

2.8×10^{-11}

FIR Filter With Reduced Coefficient

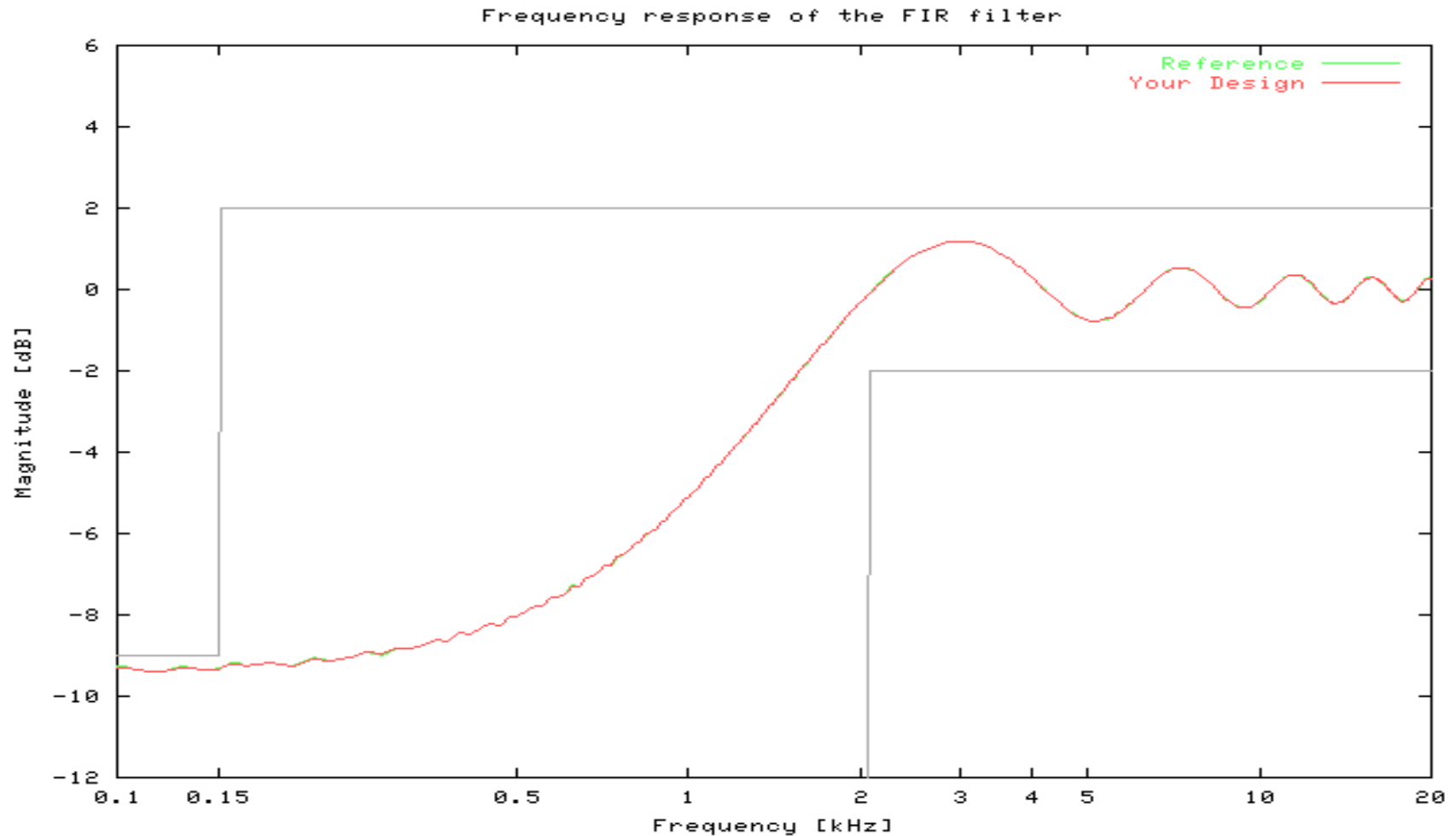
Coefficient are reduced from 21 to 8



Final Result

Frequency	100.00Mhz
Lookup Table	3298
Flip Flop	1105
Attenuation	-9.18 dB
Total Pipeline Stage	4
Matric	1.07×10^{-10}

Frequency Response of FIR Filter



Further Optimization

- Canonic Sign Digit
- Reduce the bit size of Coefficient

THANK YOU