Selected Topics in VLSI Design (Module 24513)

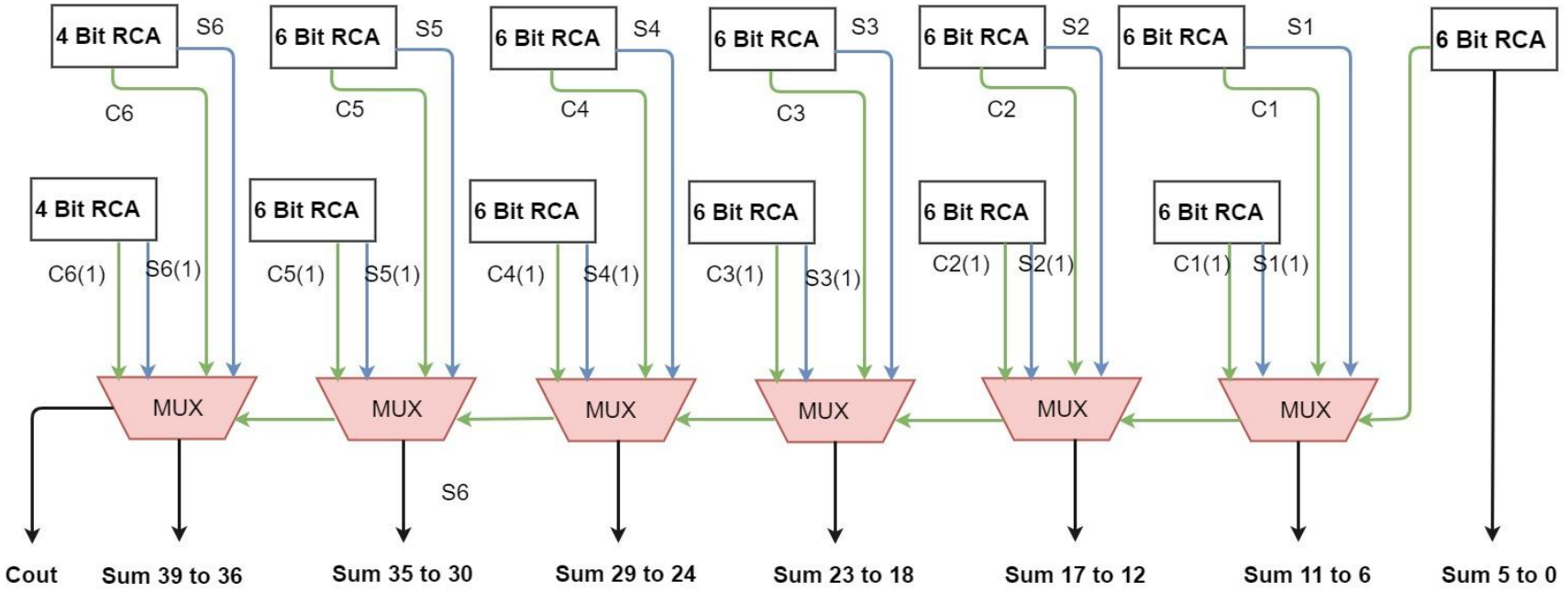
Ahsan Dilawar

Aim of Task 3

Presentation of results for an optimized design

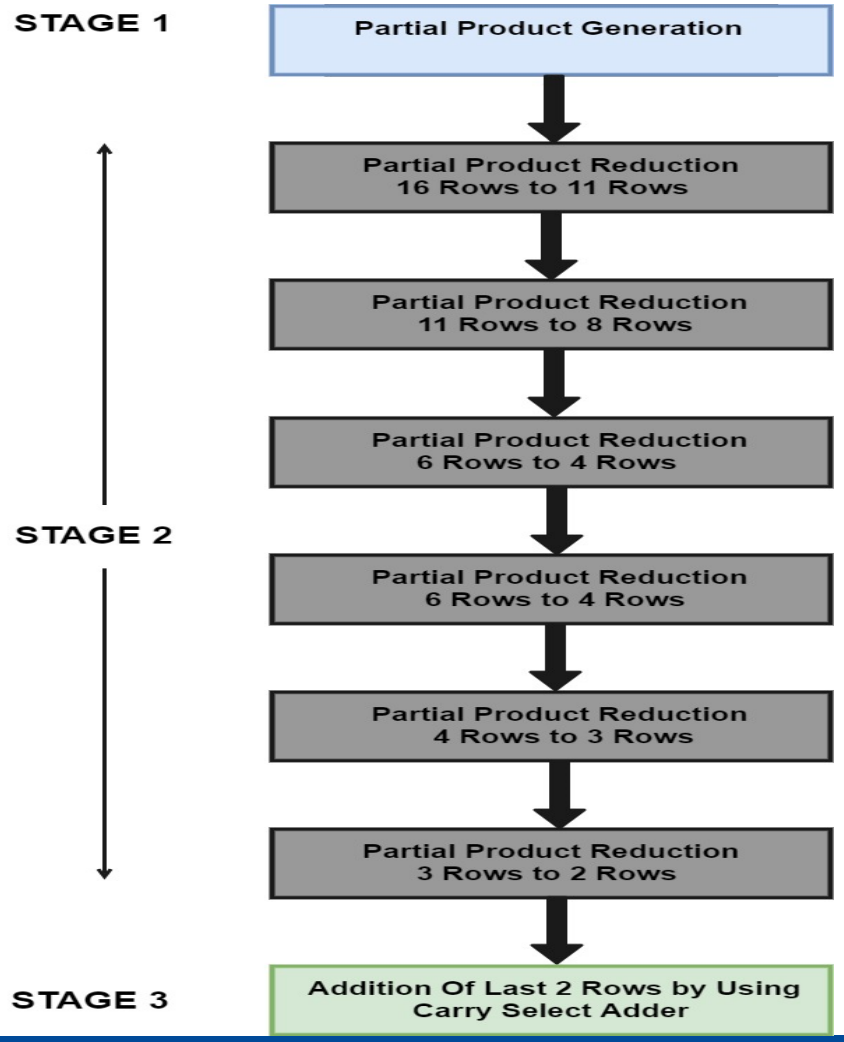
Design and Architecture

Carry Select Adder

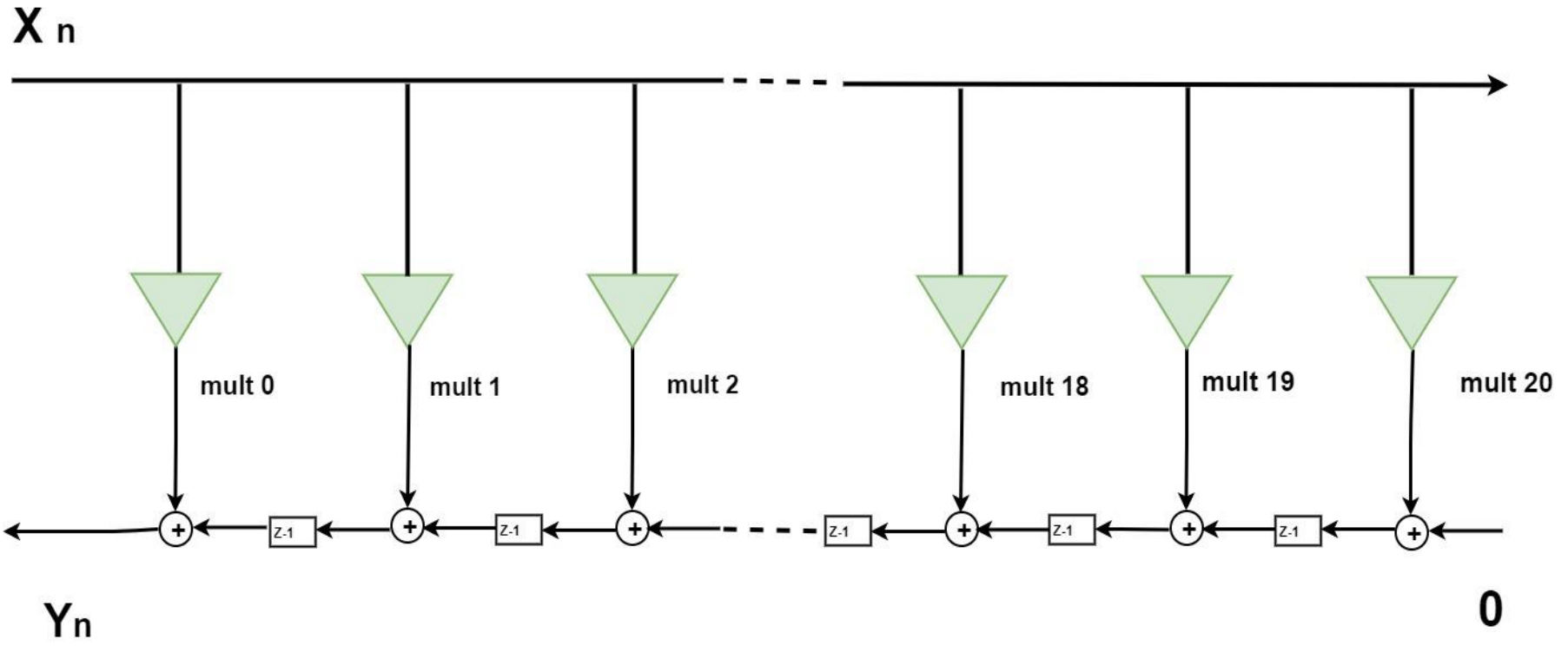


Design Of Multiplier

Wallace Tree Multiplier



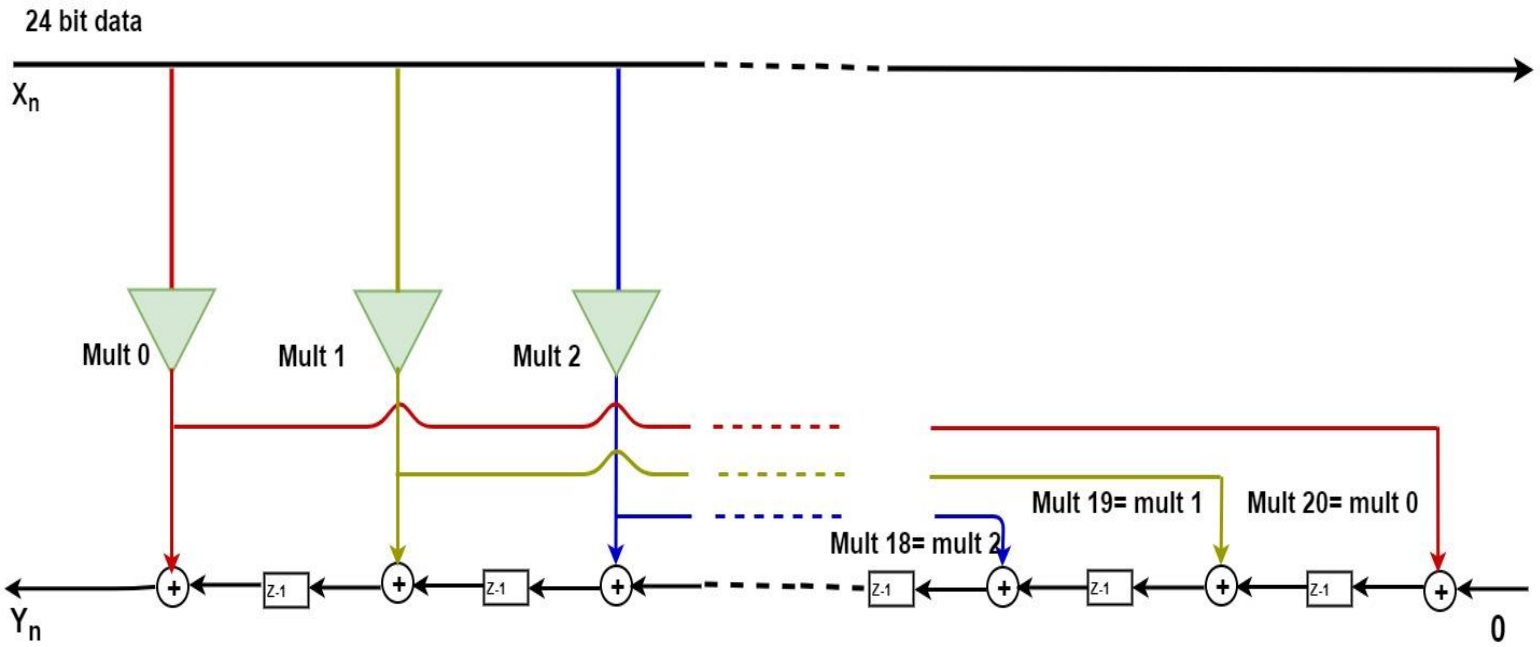
Implementation Direct Form ii



Lookup Table	5400
Flip Flop	1458
Metric	2.8 x 10-11

FIR Filter With Reduced Coefficient

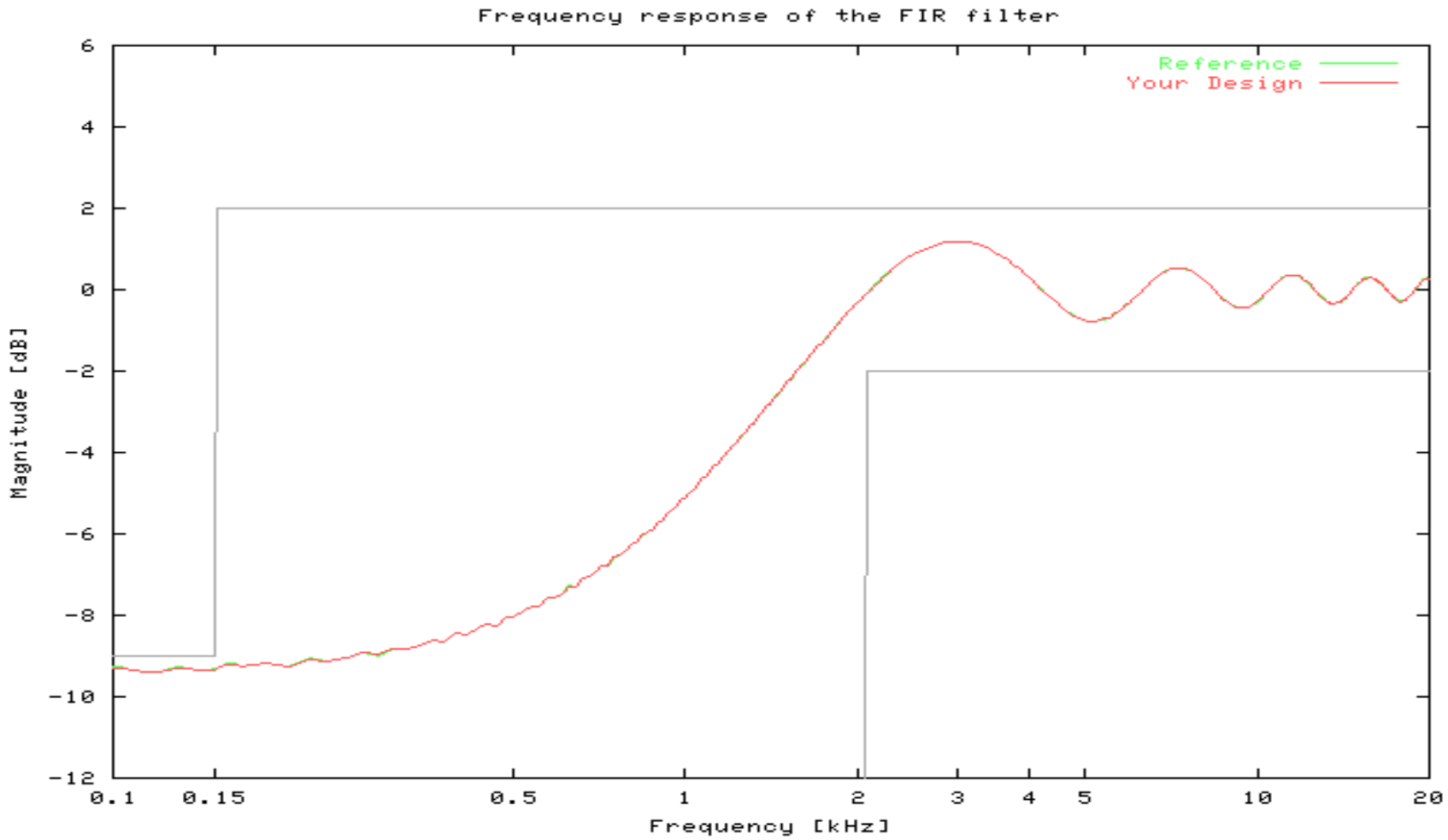
Coefficient are reduced from 21 to 8



Final Result

Frequency	100.00Mhz
Lookup Table	3298
Flip Flop	1105
Attenuation	-9.18 dB
Total Pipeline Stage	4
Matric	$1.07x10^{-10}$

Frequency Response of FIR Filter



Further Optimization

- Canonic Sign Digit
- Reduce the bit size of Coefficient

THANK YOU