Selected Topics in VLSI Design (Module 24513)

Course and contest – Intermediate meeting 1

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Outline

1. Presentation of first results
   - Chosen approach, results, outlook
2. Commentary on FPGA's
3. Task for phase 2

Presentation of first results

1. **Heller & Behl**
2. **Kammath & Hussain & Raj**

Consider: 5 minutes for each presentation

Hints:

1. Present your metric and frequency response
2. Use Matlab to design a better filter
   - Conversion-Skript
   - FDATOOL
3. Use gnuplot-script
4. Adjust pipeline stages and FIR order in the testbench

```
-- this value determines how many sinus samples are computed to test every frequency
-- higher values increase accuracy of results and the picture generated by gnuplot but slow down simulation
constant PIPELINE_DEPTH    : positive := 2;     --addapt to additional pipeline-stages
constant FIR_ORDER         : positive := 42;    --addapt to the filters order
constant DATA_WIDTH        : positive := 24;    --filters input and output datawidth. Don't change
constant number_of_samples  : integer := 600;
constant clockcycle  : time    := 10 ns;  -- 100 MHz
constant holdtime    : time    := 1 ns;
constant REFERINCE_FIR_ORDER        : positive := 16;
constant REFERINCE_PIPELINE_DEPTH   : positive := 2;
--constant tolerance   : real    := 1.0;
```

5. Start working early!

Metric

Phase 1-3 – FPGA:

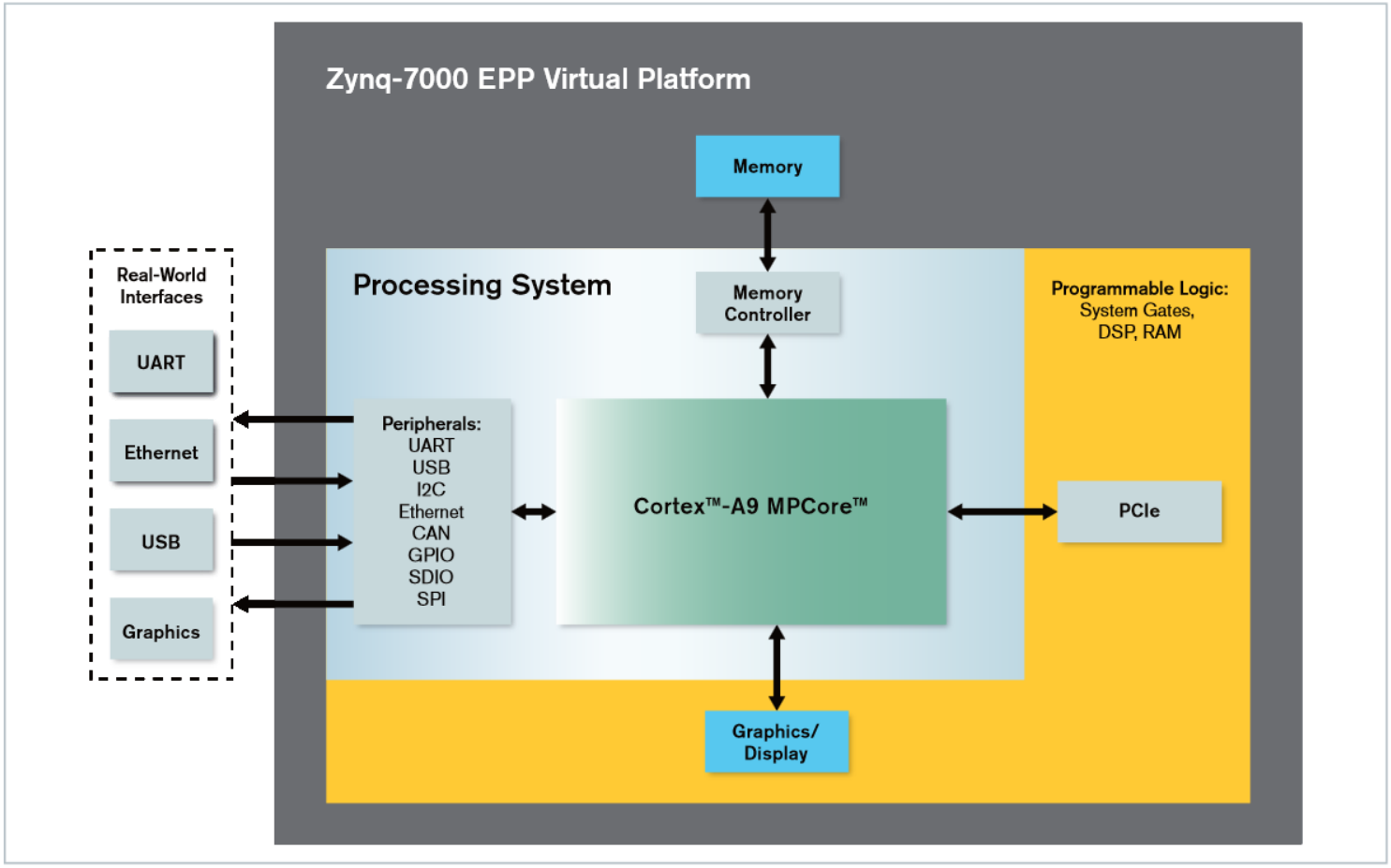
$$Metric_{FPGA} = \frac{\text{Attenuation}}{(\#LUTs + \#FF)^3}$$

Metric

z.B.:

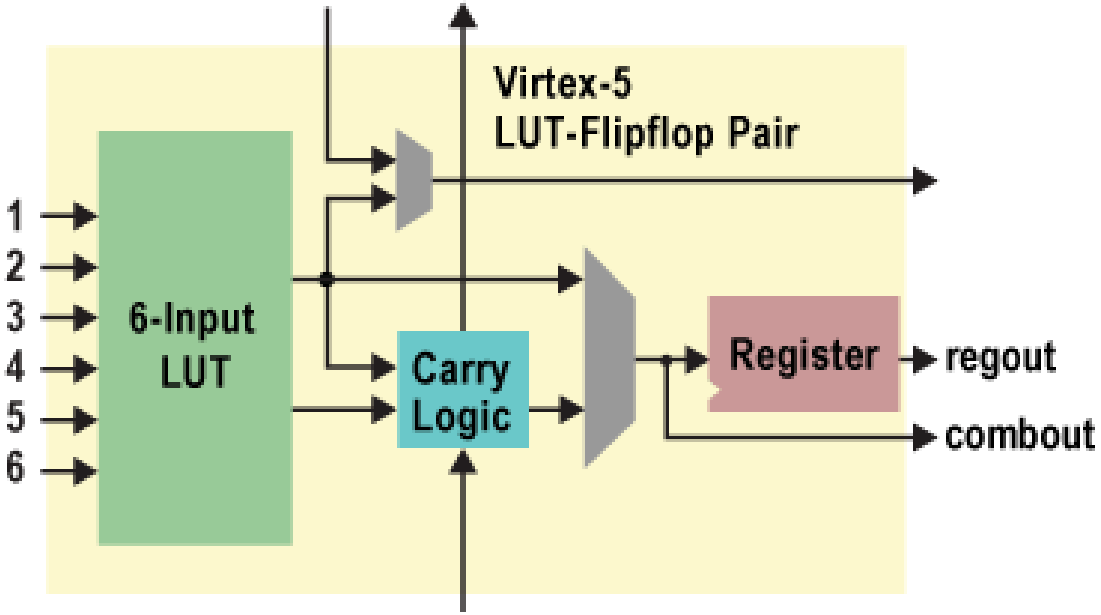
$$Metric_{FPGA} = \frac{16.08\text{dB}}{(\#7791+\#446)^3} = 2.877 * 10^{-11}$$

Xilinx Zynq - 7000



Characteristics of FPGAs

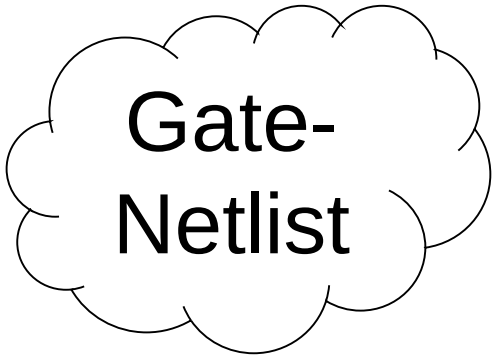
- Logic is mapped to Configurable logic blocks (CLB)
- Each CLB consists of a lookup table (LUT) and a register
- LUTs are SRAM-based
- Dedicated Carry Path



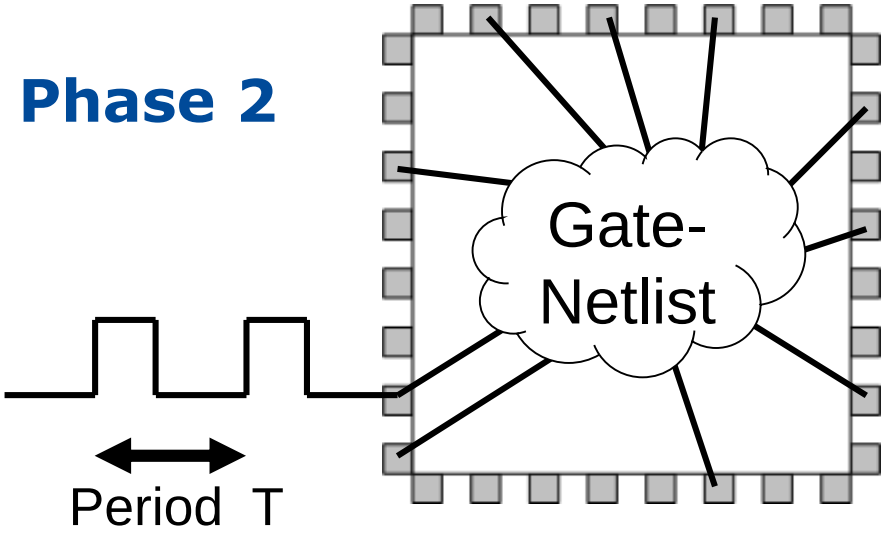
Task for phase 2

- Target: Results for an improved design, running at 100MHz
- Present parameters for:
  - Synthesized design
  - Backannotated design (implement design)

Phase 1



Phase 2



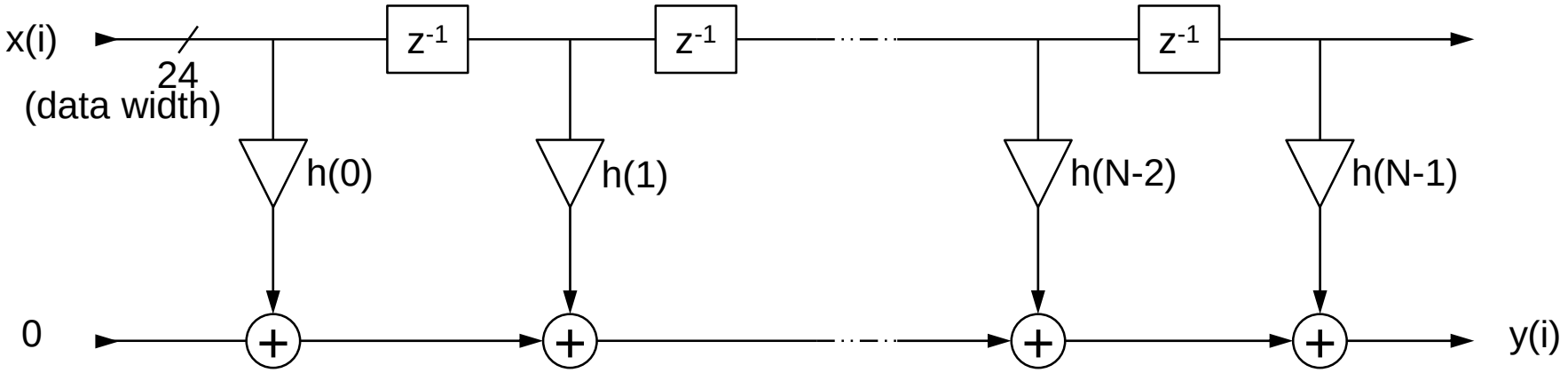
Task – Phase 2

Considerations for design handover

1. Test Place&Route / Backannotation early because significant changes are possible
2. Submit the following files: *.vhd, your_filter.xdc, your_filter_utilization_placed.rpt, your_filter_timing_summary_routed.rpt

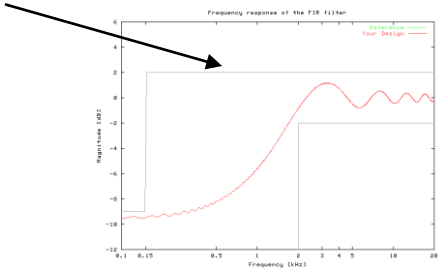
Info for award

Next meeting defines final FPGA metric



Example optimizations:

- Change Filter Form (DF I, DF II)
- Enhance coefficients h – be careful, check filter boundaries!
- Optimize Adders and Multipliers
- …



Questions?

Next meeting: November, 10th

Aim:

Presentation of results for an optimized design (Explain your motivation, pros and cons).