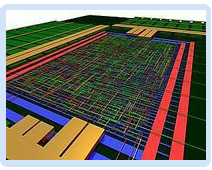
Selected Topics in VLSI Design (2015)

Official tutors

- Prof. Dr.-Ing. Dirk Timmermann
- M.Sc. Christoph Niemann
- M.Sc. Henning Puttnies
- M.Sc. Arne Wall
- M.Sc. Eike Björn Schweißguth



Course info

Schedule: The project **starts on October 15th, 2015** and **ends on January 14th, 2016** (WS 2015/16).
Title: Selected Topics in VLSI Design, Module Nr. 24513

Meetings will take place as scheduled in the Timetable, i.e. mostly Thursday@ 11:15 a.m. in room 1216.

Good and very good grades depend on various aspects like attending ALL meetings, independent and regular work on the given tasks, proper and methodical documentation as well as qualified presentations of achieved results, conclusions and optimizations! Please send all your paper work (docs, hints & advices, slides) and slides to Christoph Niemann **and** Henning Puttnies. Your presentation slides must be sent **1 DAY BEFORE** the scheduled meeting for the presentation! Your work will be added to this website.

As the work is primarily performed in our laboratories, consider the associated general rules of regulation.

Presentation

- Each presenter has 5 minutes. The last minute will be indicated. Be aware of your time (5 min), no extra time will be given. Thus, prepare and test your talk at home.
- Accepted file formats are solely ppt and pdf (to avoid conflicts with faulty display do not use latest versions or features that might not be widely supported)
- We want to know:
  - Which problems and room for optimization did you observe in your last design/approach? (with the design, not with the tools)
  - How did you try to tackle the problem(s), what did you expect before starting to investigate (i.e. in theory)?
  - Do your results prove your approach? Why or why not?
- Please do not just copy and paste blurry and skewed images from the literature into your slides. We appreciate self-made diagrams, pictures and sketches. It simply looks better and makes the understanding easier!
- Presentations can be given in GERMAN. However slides have to be prepared in ENGLISH.
- Here, a template for your slides can be downloaded: template_slides.ppt

Phase 1 (2 weeks)

- Tutors:
  - M.Sc. Christoph Niemann
  - M.Sc. Henning Puttnies
- Tasks:
  - Get familiar with filter theory and its operation
  - Use the Xilinx FPGA synthesis tools and the ModelSim simulation environment
  - Direct implementation of the FIR filter (do not use + and *-operators)
  - The target Hardware you have to choose in the Xilinx Vivado Project is a Zedboard.
  - Template and important hints for the presentation of achieved results: see below (can be used, no must)
  - The constraints-file (.xdc) is required to define a targeted operating frequency for the synthesis tools
  - **Target**: Your first working FIR filter design
- Materials:

2015_vlsi_1.pdf	
How_to_Setup_your_Project.pdf	
vhdl_recap.pdf	
sources.zip	

Phase 2 (2 weeks)

- Tasks:
  - Architectural / component optimization (adders, multipliers, CSD, pipelining, parallelization, term sharing, ...)
  - Results for the next presentation have to include values for the synthesized and backannotated design
  - The constraints-file (.xdc) may be used to define further directives (e.g. for pin positions or timing constraints for various signals)
  - **Target**: A better design, in terms of the metric
- Materials:

FirResults.plt	1.0 K
fir_filter_tb.vhd	25 K
generate_coefficients.m	6.0 K
2015_vlsi_2.pdf	324 K

Phase 3

Phase 3 (2 weeks)

- Tasks:
  - Architectural / component optimization (adders, multipliers, CSD, pipelining, parallelization, term sharing, ...)
  - Test your design on a ZedBoard evaluation Platform
  - Present the quality of your filter to the audience of the next meeting
- Materials:

2015_vlsi_3_-_write_bitstream.pdf	369 K
zedboard_fw.zip	19.9 K

Phase 4 (2 weeks)

- Tutors:
  M.Sc. Christoph Niemann
- Tasks:
  - Mapping on ST65 technology
  - Further design improvements using the synthesis scripts and tools (architectural changes are welcome but we want to primarily see an adaptation of your design due to the ASIC technology instead of the FPGA and we expect you to purposefully enhance the synthesis scripts for your design requirements)
  - Remark: For a correct power simulation, your design hierarchy must be flat (ungroup)!
  - **Target**: A working and optimized ST65 netlist
- Materials:

2015_vlsi_4_synthesis.pdf	0.9 M

Phase 5 (2 weeks)

- Tutors:
  - M.Sc Christoph Niemann
- Tasks:
  - Layout for ST65 technology
  - However, investigations and optimizations in all phases are welcome (this is the last phase for the design contest)
  - Usage of Cadence Encounter and Synopsys to achieve backannotated results of a chip layout
  - Remark: Your final netlist may not include slashes and backslashes
  - For presentation: Include a picture of your chip layout together with the results (f, P_{dyn}, P_{leak}, A_{core}, chip utilization, metric)
  - **Target**: Complete ST65 layout and backannotated results
- Materials:
  - 2015_vlsi_5_layout.pdf
  - filter_power_cadence.tcl
  - start_power_analysis.sh
  - setload_fix.pl

Attendees & slides

Name	1st Meeting	2nd Meeting	3rd Meeting	4th Meeting	5th Meeting
Felix Uster	G1P1	G1P2	G1P3	UsP4	UsP5
Matthias Clahsen	G1P1	G1P2	G1P3	ClP4	ClP5
Sascha Rohde	G2_3P1	G2P2	G2P3	RoP4	RohP5
Daniel Ziese	G2_3P1	G3P2	G3P3	ZiP4	ZiP5
Daniel Roisch	G2_3P1	G3P2	G3P3	RoiP4	RoiP5

Latest results for the frequency and the benchmark metrics

Name	2nd Meeting	3rd Meeting	4th Meeting	5th Meeting
Felix Uster	3.87*10^-8	9.49*10^-8	2.24*10^10	1,56*10^10
Matthias Clahsen	3.87*10^-8	9.49*10^-8	1.52*10^10	3,33*10^8
Sascha Rohde	6.7*10^-9	2.03*10^-7	9.3*10^10	--
Daniel Ziese	1.08*10^-9	6.89*10^-8	8.42*10^8	1,12*10^9
Daniel Roisch	1.08*10^-9	6.89*10^-8	9.7*10^9	7,85*10^9

Timetable

Status	Date	Milestone	Description
done	October 15th	Kick-Off Meeting: Start Phase 1	Introduction and start with an exemplary design
done	October 15th	VHDL-Recap	Recapitulation of VHDL, tools and flow
done	October 29th	Intermediate meeting: Start phase 2	Initial results for Xilinx FPGA
done	November 12th	Intermediate meeting: Start phase 3	Results with backannotated optimizations for Xilinx FPGA
done	November 26th	Intermediate meeting: Start phase 4	Final FPGA-Design
done	December 10th	Intermediate meeting: Start phase 5	Results from Cadence First Encounter, latest improvements, description of best/final architecture; picture of layout; final results on speed, area, Netlist for ST65; results for speed, power, area and the benchmark metric from Synopsys tools
	January 14th	Final meeting	Results from Cadence First Encounter, latest improvements, description of best/final architecture; picture of layout; final results on speed, area, power and the benchmark metric
	January 14th - 18:00	Dinner	

Design infos

- Prof. Timmermann lecture Advanced VLSI Design
- Prof. Timmermann lecture HIS - Highly Integrated Systems (Hochintegrierte Systeme)
- Prof. Timmermann seminar Applied VLSI Design (former events of this seminar)
- Brief description of steps from ASIC design to volume production Design steps, provided by Europractice; see also full Activity Report 2014 (you may also check successive reports for further Information)
- Citeseer: Huge and uptodate database of scientific papers. Use appropriate keywords for your search.
- DBLP: Another database of scientific papers is from the University of Trier.
- IEEE: From within the university network, you can search the IEEE proceedings etc...

Arithmetic structures

- Book „Architekturen der digitalen Signalverarbeitung“, Peter Pirsch
- Book "Computer Arithmetic: Algorithms and Hardware Designs", Behrooz Parhami
  - Pipelined Algorithms
- Booth-Algorithmus
  - Booth and modified Booth
- As Filters mainly consist of Adders and Multipliers, you may find interesting information here:
  - Binary Adder Architectures for Cell-Based VLSI and their Synthesis (Document)
  - Arithmetik, University of Flensburg
  - Hints for speed freaks:
    - Conditional Sum
      - excellent for speed but needs fast multiplexers
      - in CMOS this can be done using transmission gates
      - however, cascaded transmission gates are slow unless buffers are used
    - Carry Lookahead (CLA)
      - fast, but irregular and large layout, built up of active gates
      - variants of CLA
        - Brent Kung adder
          - small and regular layout, but a bit slow
        - Kogge Stone adder
          - larger but faster
        - Han Carlson adder
          - tradeoff between BK and KS
        - others?
- For everything else: Google

Information on Synopsys and ST

- To be able to work with all the tools you need an account for the local laboratories and the general one from the "ITMZ". Please refer to Mrs. Krueger (room 1312) for the local account if you do not have one yet.
- If you want to build the designs out of basic cells you can find the component declarations for Xilinx at $XILINX\vhdl\src\unisims\unisim_VCOMP.vhd on the machine. Consider that not all gates and specialized functions for FPGAs can also be synthesized for an ASIC.
- Use the menu entry "Help->Man pages" for command reference within Synopsys
- Synopsys tutorials, user guides etc. can be found here: /opt/lehre/vlsi/

Cadence FE

Information on Cadence First Encounter:

- The following manuals refer to Silicon Ensemble (previous tool) but are helpful and in part still valid:
  - Using the Power Analyzer to evaluate the power consumption: Power Analyzer
  - Silicon Ensemble Lecture Slides
  - Silicon Ensemble Handout
  - A tutorial for the clock tree synthesis: CTgen-Files
  - A good tutorial from Lunds University with additional infos can be found.

Lehrstuhl "Rechner in Technischen Systemen"
Prof. D. Timmermann

Laboringenieur
Dipl.-Ing. Th. Wegner
Büro: W1315
Tel.: 498 7267

Content
Official Tutors
Course info
Timetable
Attendees & more
Design infos
Arihtmetic structures
Information on Synopsys and ST
Cadence FE

Old Projects:
2014
2013
2012
2011
2010

Schnelleinstieg
Publikationen
Anfahrt
Kontakt
Laborpraktikum
Lehrangebot
Highlights
Projekte