1. Download an unzip the sources.zip folder from the website
2. Open Vivado
3. Setup your Project:
    a. Klick on **Create New Project**
    b. Select a name and location and klick **next** and **next** again (Important: you must use your student directory (G) and spaces are not allowed in the path**)**
    c. In the **Add Sources** dialog click on **Add Files**
    d. Add the following files (from the sources.zip folder):
        i. Fir_filter.vhd
        ii. Fir_filter_tb.vhd
        iii. Fir_filter_tb_pack.vhd
        iv. Makros.vhd
        v. Syslos.vhd
        vi. Your_filter.vhd
    e. In the column **HDL Source For** select **Simulation only** for the following files:
        i. Fir_filter_tb.vhd
        ii. Fir_filter_tb_pack.vhd
        iii. Makros.vhd
        iv. Syslos.vhd
    f. Klick **next** and in the **Add Existing IP** dialog click **next** again
    g. In the **Add Constraints** dialog click **Add Files** and add the following constraints files (from the sources.zip folder):
        i. Filter.xdc
    h. Click **next**
    i. In the **Default Part** dialog select **boards** and under **Dispay Name** select the **Zedboard Zynq Evaluation and Development Kit** which we will use as target device
    j. Click **next** and **finish** afterwards
    k. In the **Flow Navigator** (left column in the Vivado IDE) under **Project Manager** click on **Add Sources** select **Add or create simulation sources** and click **next**
    l. Click on **Add Files**
    m. Select **Files of type** as **All Files** and add the following file, which contains the input values for the testbench:
        i. SineVals.txt
    n. Click on **finish**
    o. In the **Flow Navigator** (left column in the Vivado IDE) under **Synthesis** click on **Synthesis Settings** and in the option dialog set **-max_dsp** to **0** (This will make Vivado use only LUTs and FFs and no DSP-Slices in the synthesis process and consequently you will get the correct metric for your filter)
4. Test your Project:
    a. In the **Flow Navigator** (left column in the Vivado IDE) under **Simulation** click on **Run Simulation** and **Run Behavioural Simulation**
    b. To simulate your design completely type the command **run –all** into the **console**
    c. The simulation was successful, when the following was stated in the **console** windos:
        i. Summary: 0 error(s), 0 warning(s) and 0 note(s)
5. It is highly recommended to use Modelsim as Simulator because it runs more stable and quickly compared to the internal Vivado Simulator. To use Modelsim:
    a. In the **Flow Navigator** (left column in the Vivado IDE) under **Project Manager** click on **Project Settings**

   b. Click on **Simulation** and select as **Target Simulator** the entry **QuestaSim/ModelSim Simulator** click **Yes** and **OK**
   c. Select **Tools** and **Compile Simulation Libraries** and select **compile**
   d. Wait until the compilation was finished (this is only needed to be done once)
6. To create a new hdl-file and add it to your Project:
   a. In the **Flow Navigator** under **Project Manager** click on **Add Source**
      i. When you want to create a synthesizable source (e.g. Adder, Multiplier) select **Add or create design sources**
      ii. When you want to create a non-synthesizable source (e.g. Testbench) select **Add or create simulation sources**
   b. Click **next** and **Create File** and select a name
   c. Click **Finish**
7. To Synthesize your project under **Synthesis** select **Run Synthesis**