

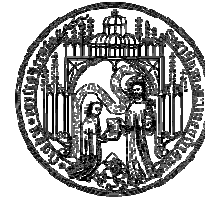
Utilizing Parallelism of TMR to Enhance Power Efficiency of Reliable ASIC Designs

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Outline

- Motivation
- Power-efficient TMR approach
 - Design idea
 - Design structure
 - Results
- Conclusion / Outlook

Motivation



- Power reduction for mobile applications



- Reliability suffers with every new technology and becomes more and more a concern of VLSI designers



- Redundancy – traditional approach to enhance reliability
 - At the cost of area and power consumption

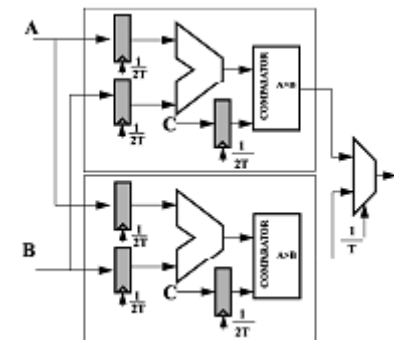
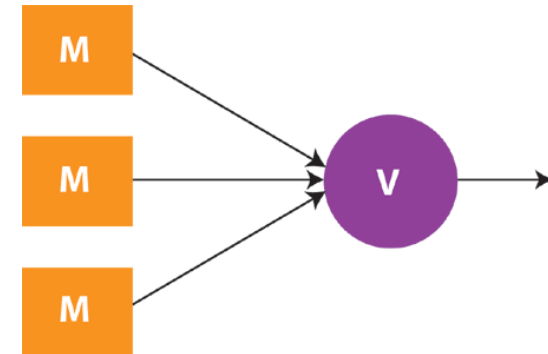


Design Idea

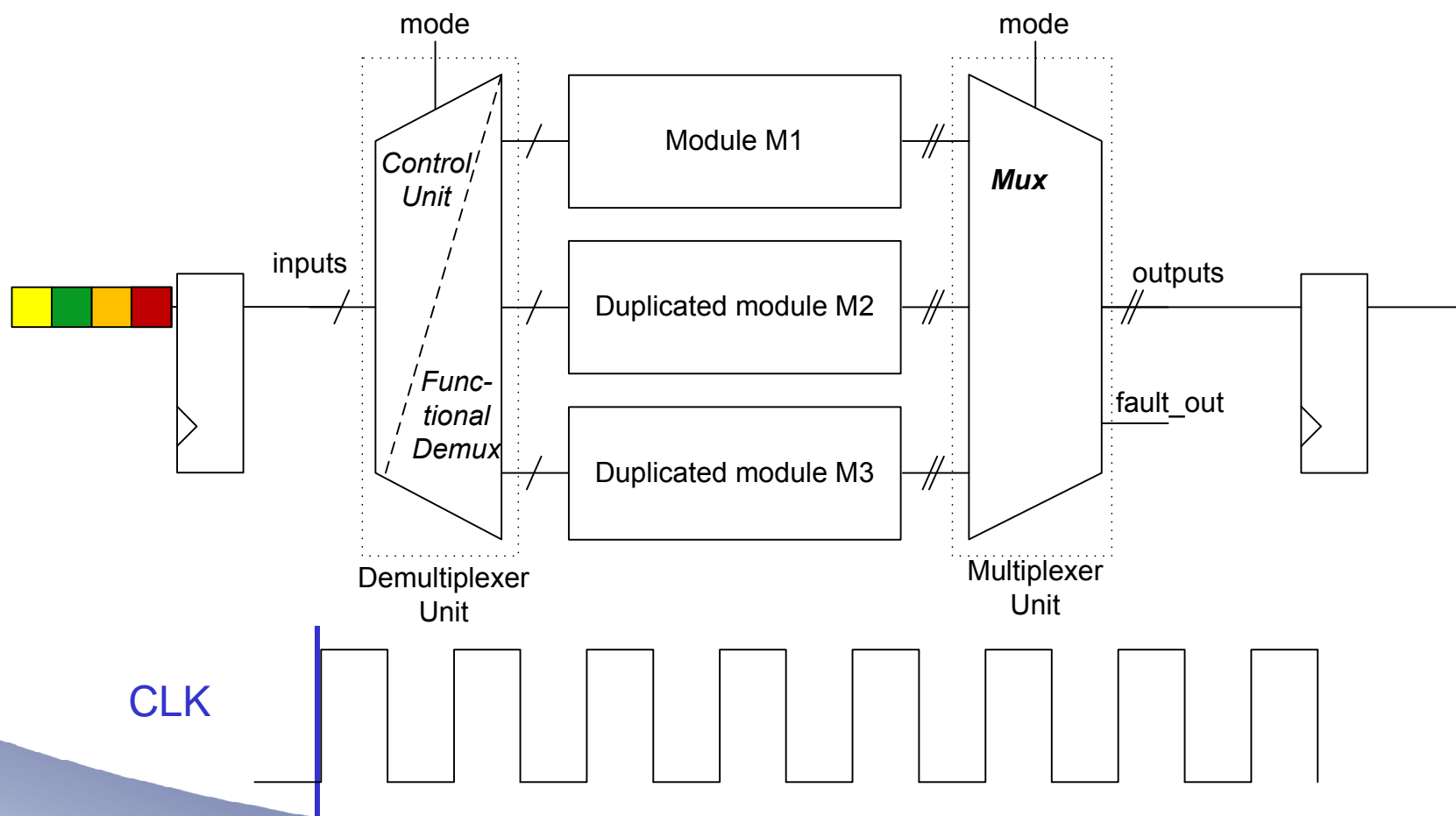
- TMR – Triple modular redundancy
 - Three identical units
 - Same input for every module
 - Results are merged by a voting unit
 - Threefold power consumption and area

- Parallelized data paths
 - Reduced operating frequency and supply voltage
 - Same throughput
 - Larger design area

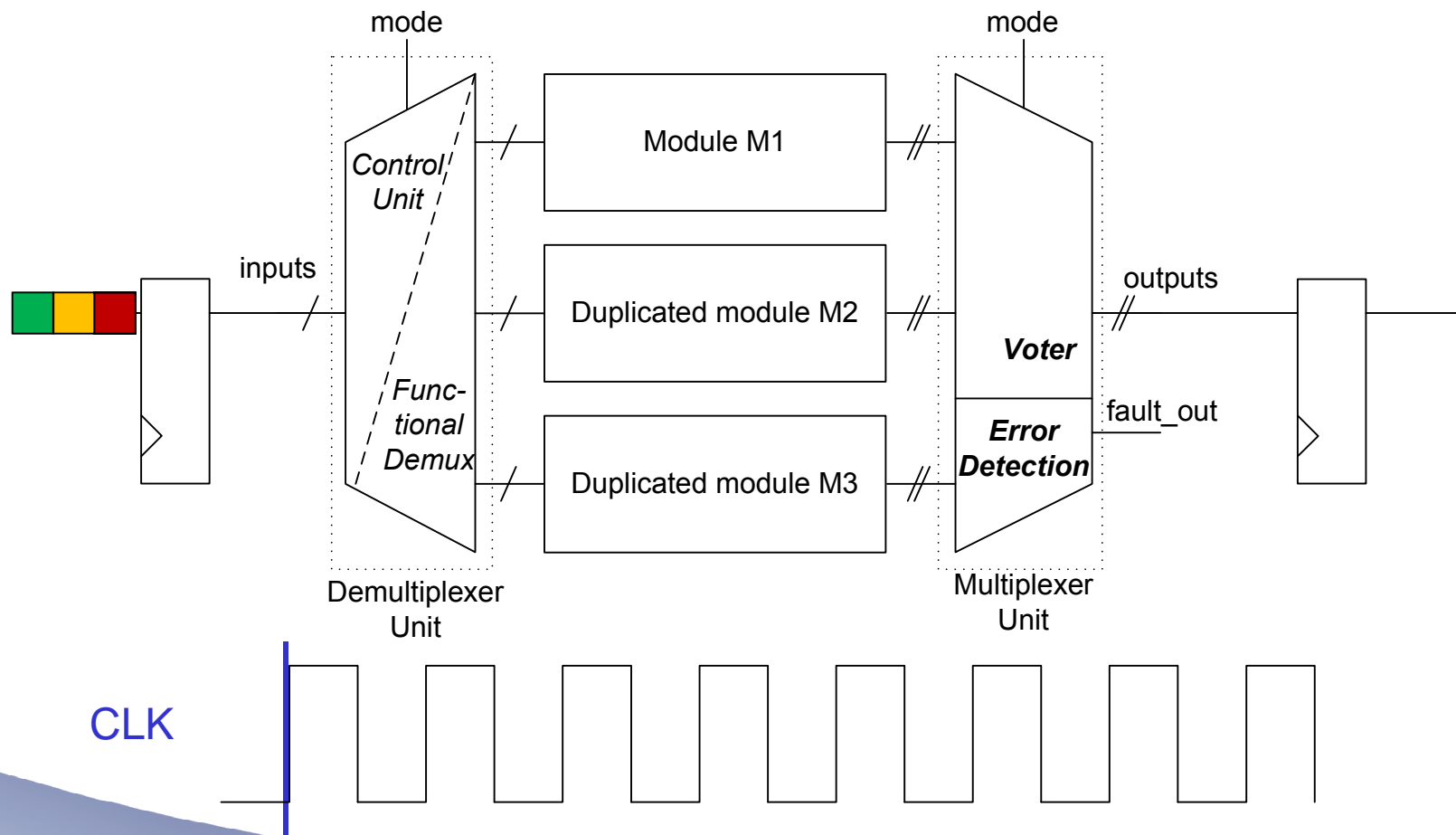
- Inherent parallel data paths of TMR
 - Power reduction possible



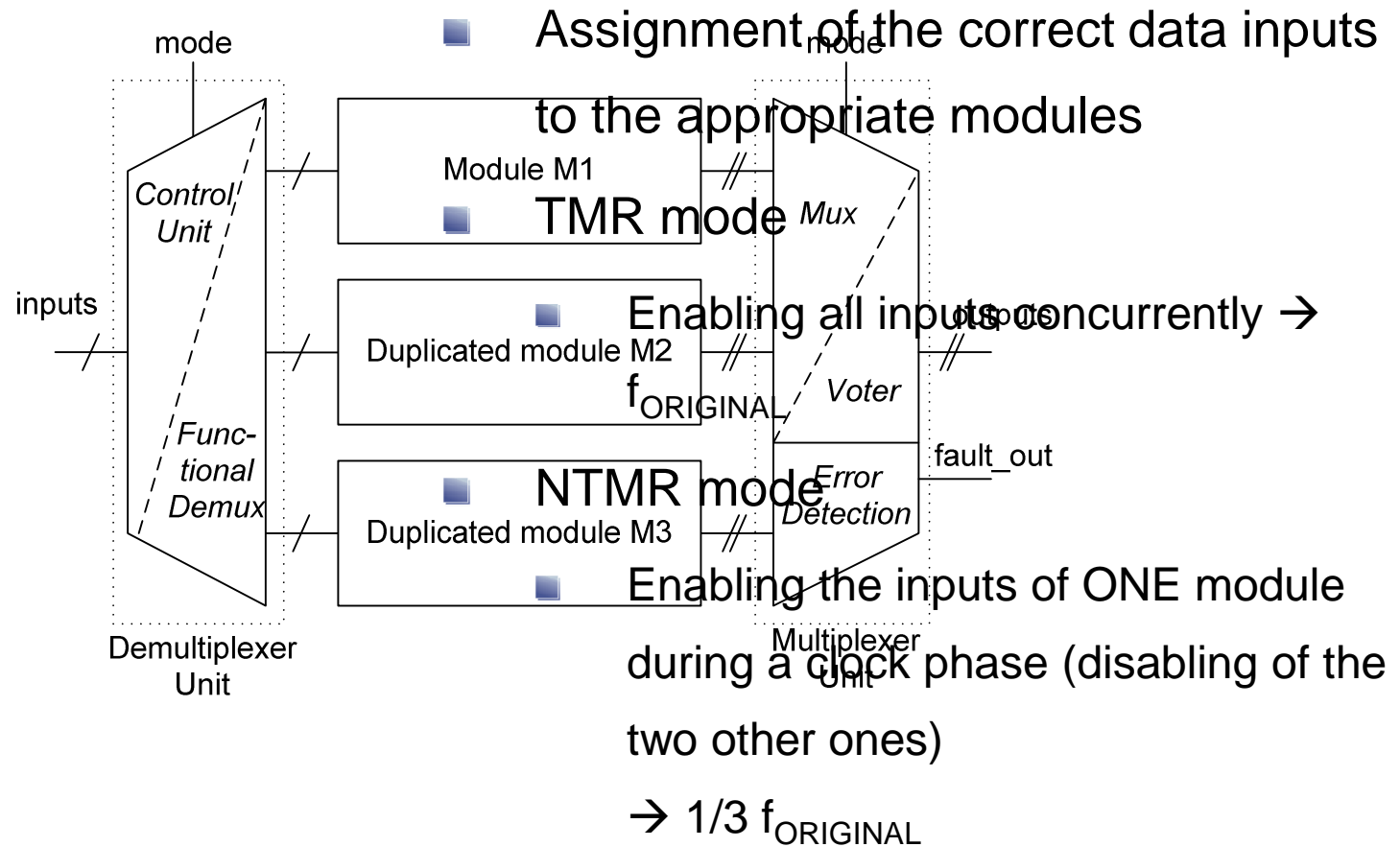
Design idea – NTMR operation mode



Design idea – TMR operation mode



Design Structure – Demultiplexer Unit



Design Structure – Multiplexer Unit

- Assignment of the correct data output

- TMR mode

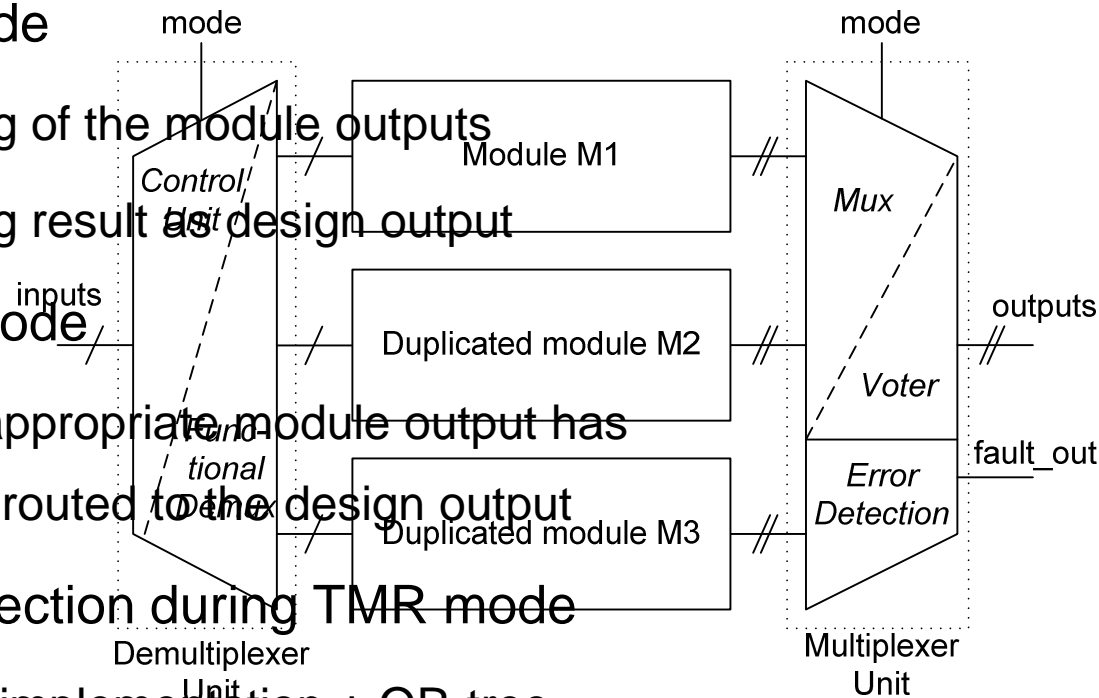
- Voting of the module outputs
- Voting result as design output

- NTMR mode

- The appropriate module output has to be routed to the design output

- Error detection during TMR mode

- XOR implementation + OR-tree
- Small amount of inherent reliability due to 3 XORs per output

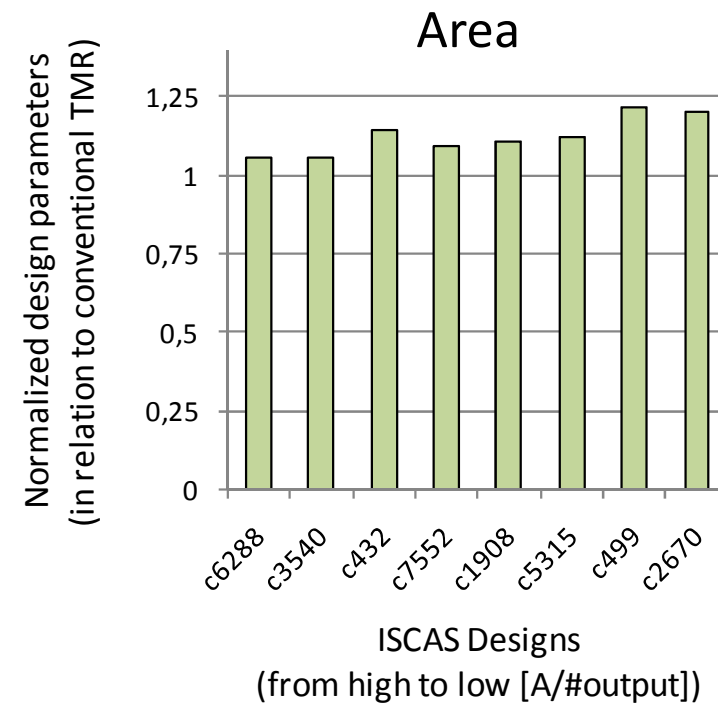
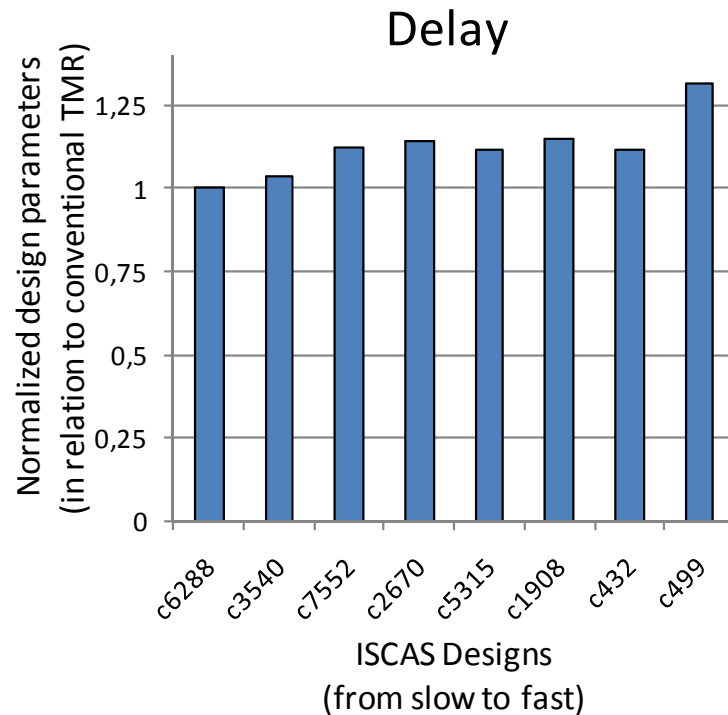


Simulation Setup

- Industrial 65 nm technology
- Gate level simulation
- Toggle rate analysis for power calculation

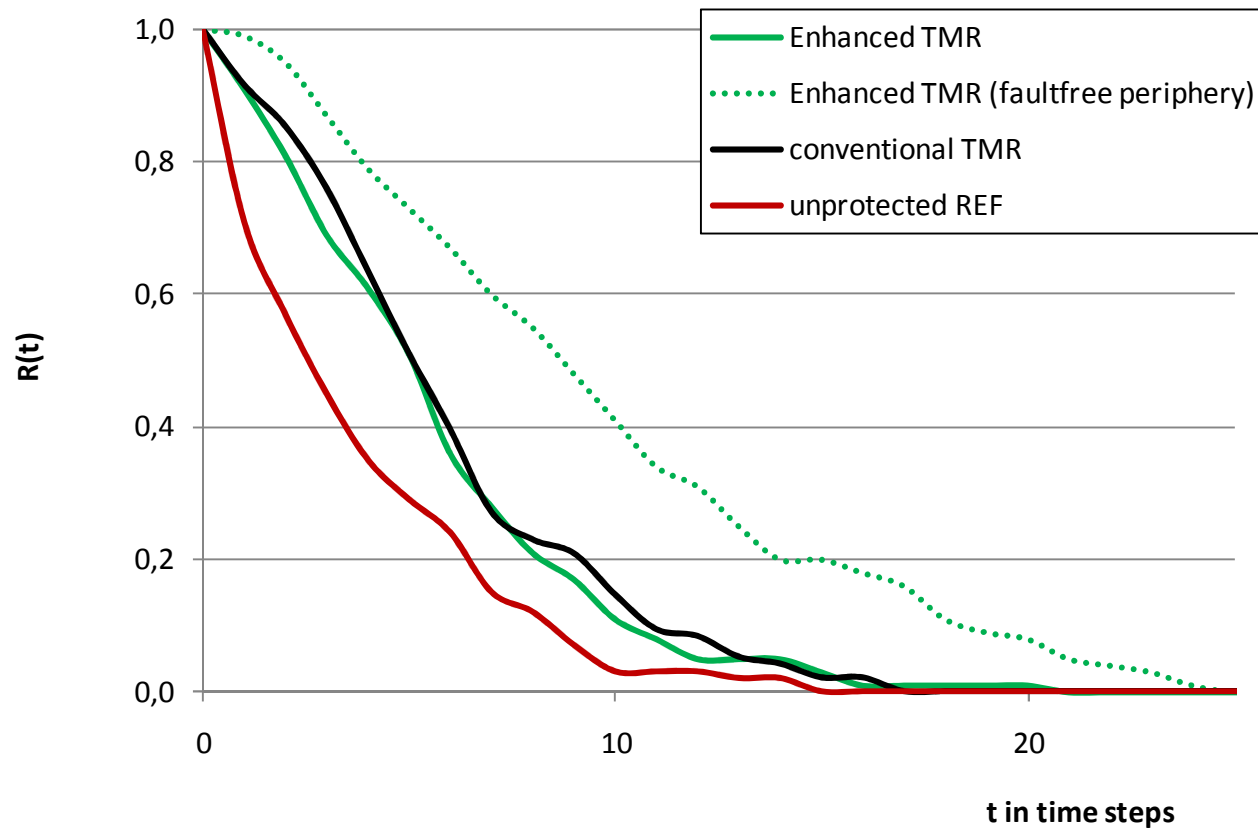
- Stuck-at faults with randomly chosen locations
(incl. periphery)
- Constant failure rate for every net of the system
→ Area dependent system failure rate

Results – Design overhead



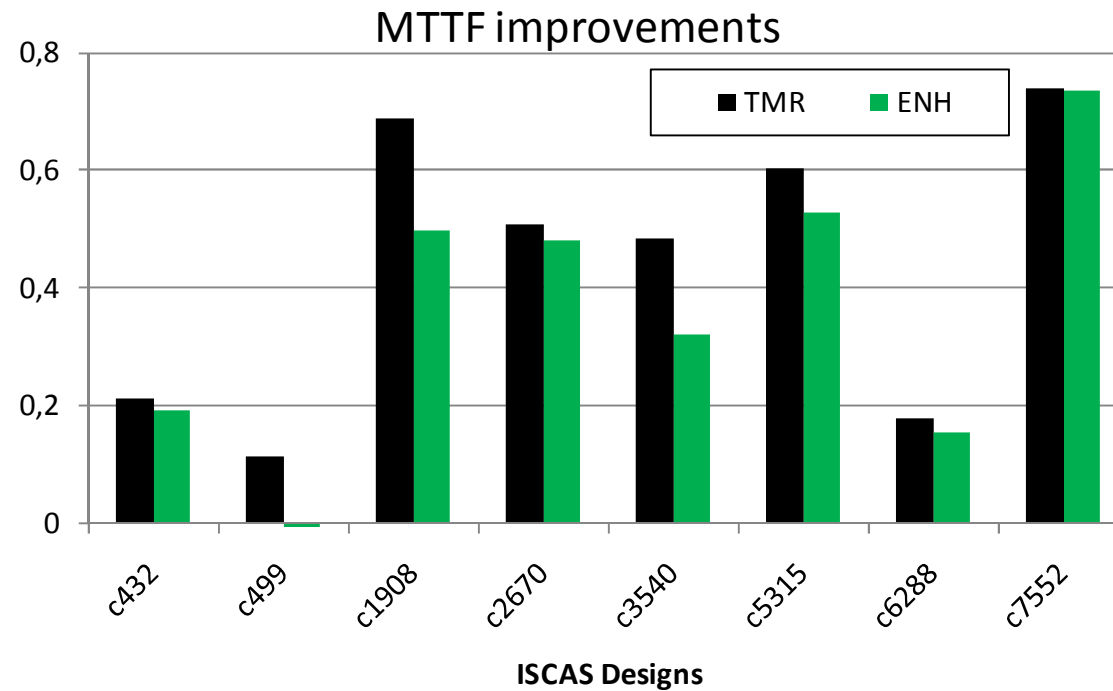
- Lowest overhead for large and slower designs with few output bits

Results – Reliability



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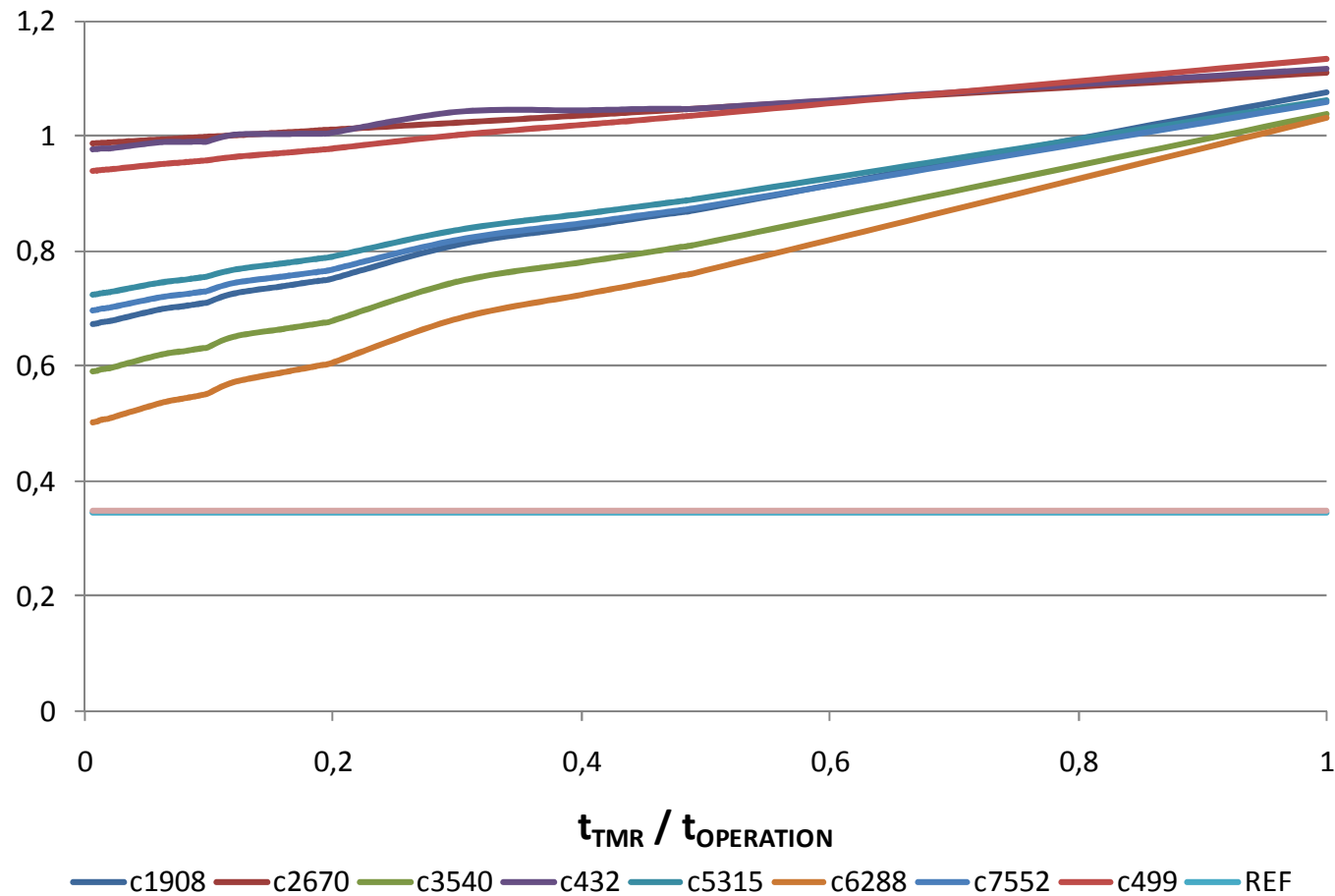
Results – MTTF improvements



- Larger designs suffer less from area overhead

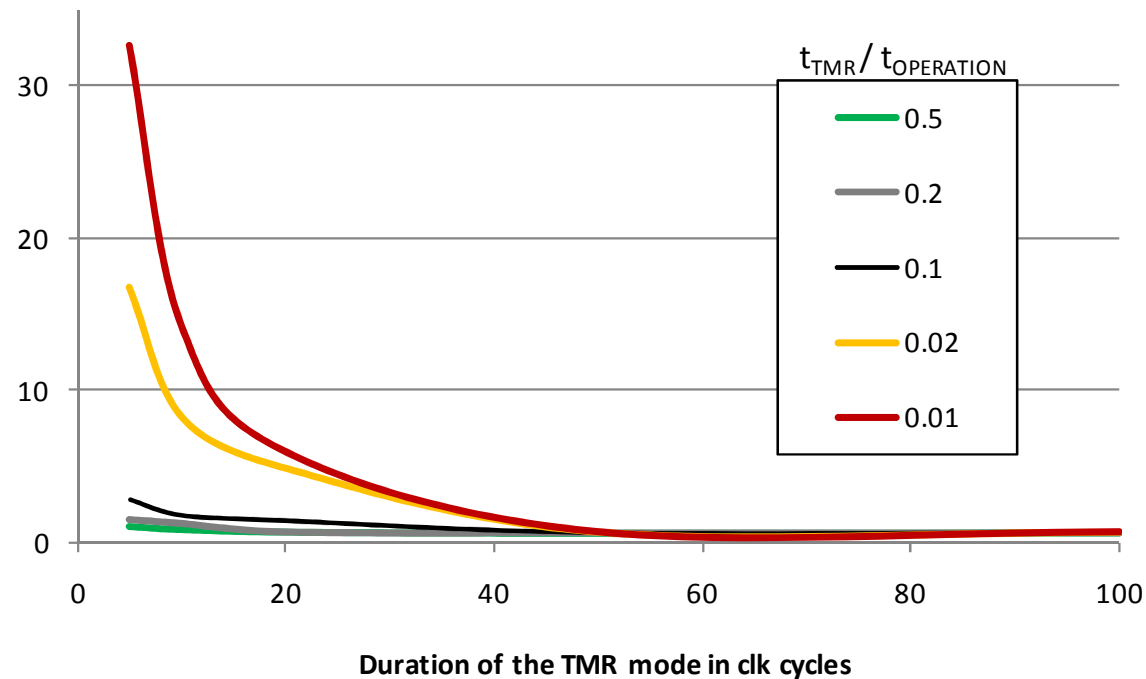
Results – Power consumption

Power Consumption
(normalized to conventional TMR)



Results – Switching Strategies

Number of errors before detection



- Fast detection of faults in the module with
 - Sufficient high $t_{TMR} / t_{OPERATION}$ rate
 - Sufficient long TMR mode duration → possible low $t_{TMR} / t_{OPERATION}$ rate

Conclusion / Outlook

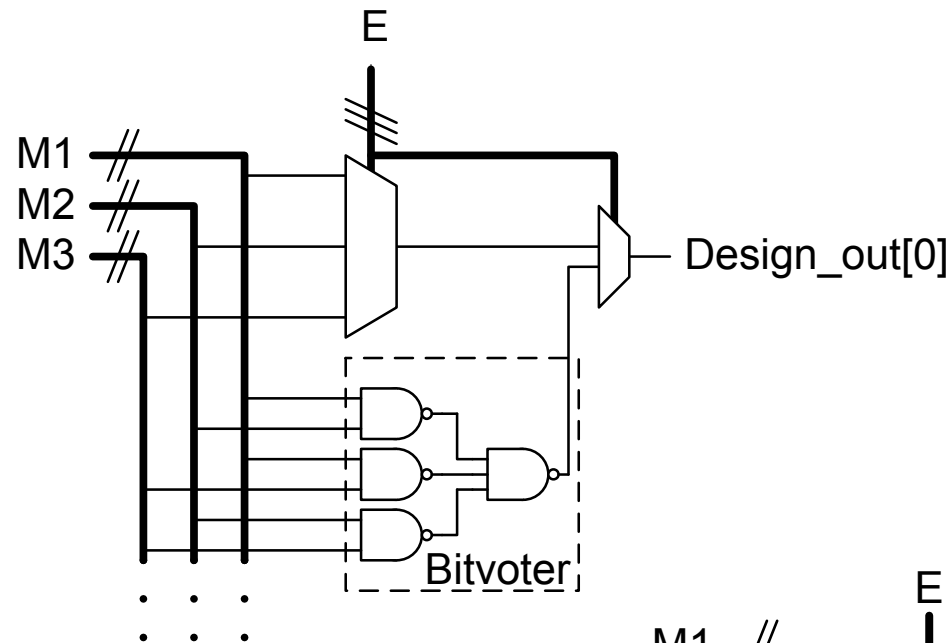
- Lifetime reliability will be a major issue in circuit design
- Design of an enhanced power-efficient TMR design using the inherent parallelism of TMR
- Power savings up to 50 % compared to conventional TMR are achievable with a slightly overhead in area, latency

- Further enhancements
 - *Reduced Supply voltage*
 - *More reliable periphery*
 - *Implementation of further operation modes*

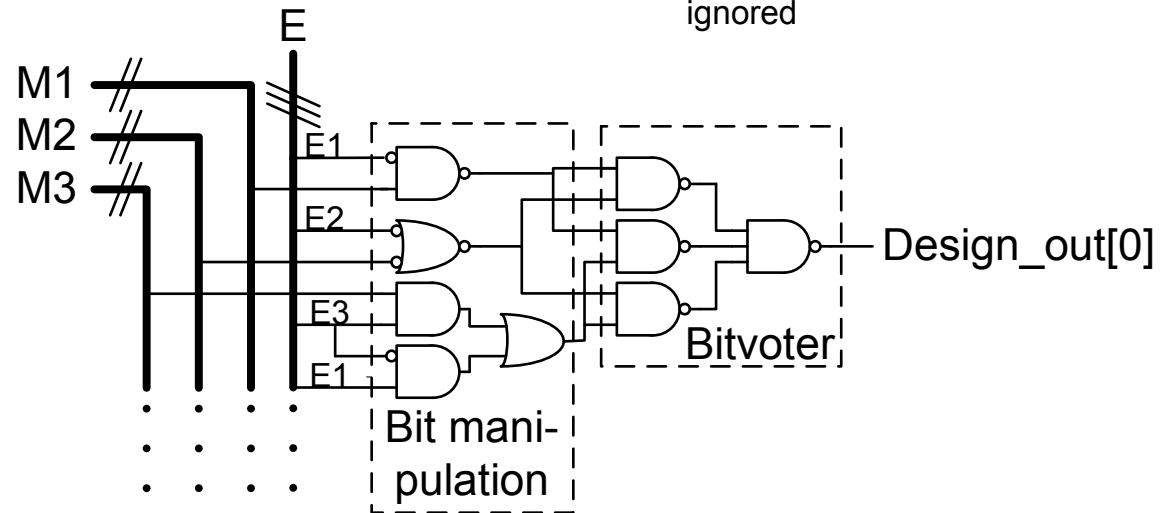


Backup

Backup – Voter implementations



Ex = 0 → outbit bits of Mx are ignored



Backup – Error detection

