DDECS 2010, Vienna, Austria

Modeling Temperature Distribution in Networks-on-Chip using RC-Circuits

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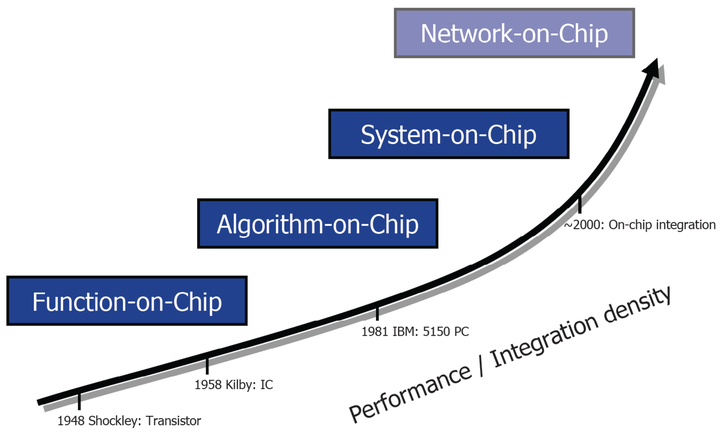
Motivation



Network-on-Chip

- Promising properties to overcome or mitigate current issues:
  - Modularity
  - Encapsulation
  - Portability
  - Reuse
  - Scalability
  - Parallelism
  - …

Temperature related Issues

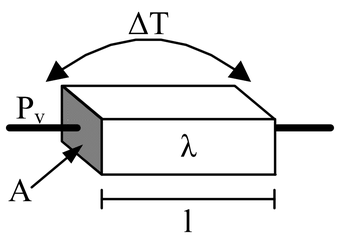
- Power consumption
- Leakage currents
- Reliability
  - Electromigration
  - Time Dependent Dielectric Breakdown

→ High temperatures accelerate all of these
→ Need for temperature aware system management

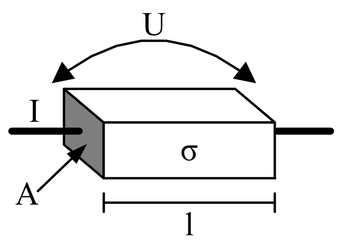
Need for a generic, flexible, fine grained TEMPERATURE MODEL

Simulation flow based on a generic RC-grid

Dualism of thermal and electrical energy

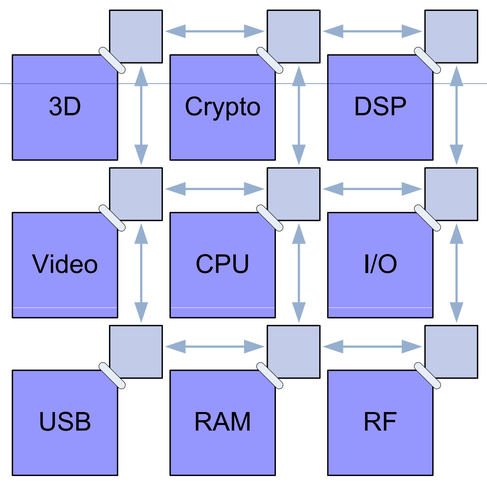


Thermal resistance

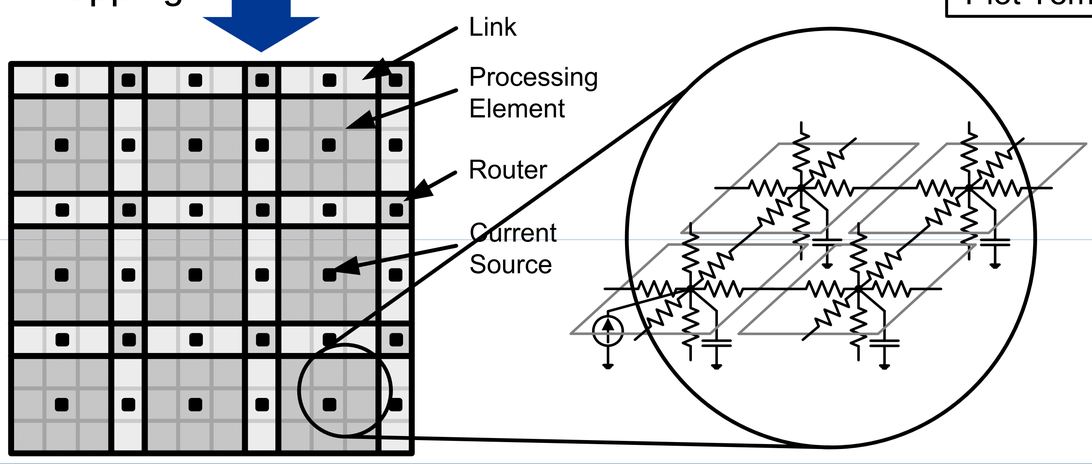


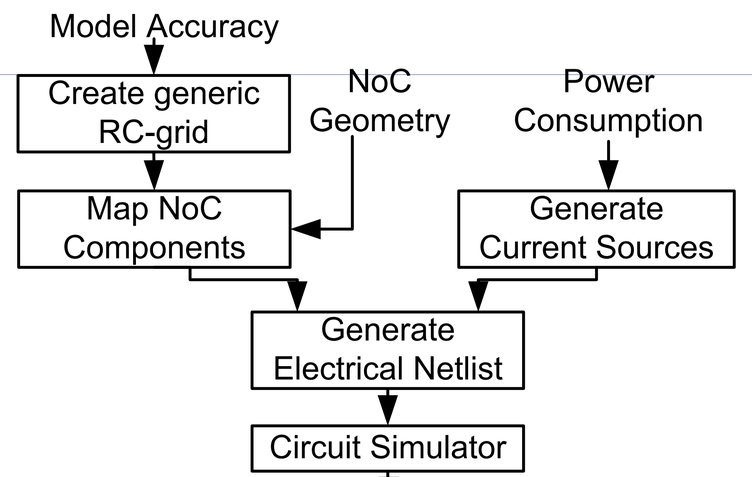
Electrical resistance

Thermal Model	Unit of Measurement	Electrical Model	Unit of Measurement
Heat Flow	P [W]	Current	I [A]
Temperature	T [K]	Voltage	U [V]
Resistance	R_{th} [K/W]	Resistance	R [V/A]
Capacity	C_{th} [J/K]	Capacity	C [As/V]
Time constant	τ [s]	Time constant	τ [s]
Thermal conductivity	λ [W/(K·m)]	Electrical conductivity	σ [A/(V·m)]

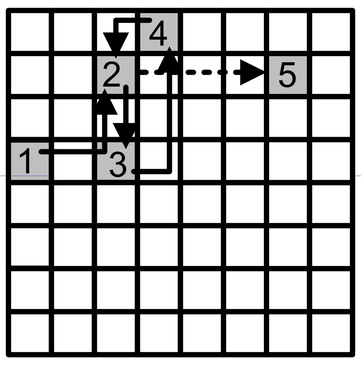


Mapping





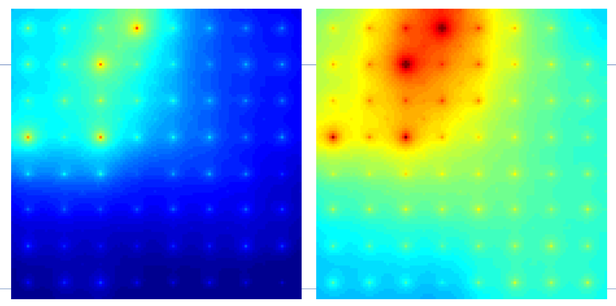
Exemplary application scenario



1 I/O
2 CPU
3 Crypto
4 RAM
5 CPU remapped

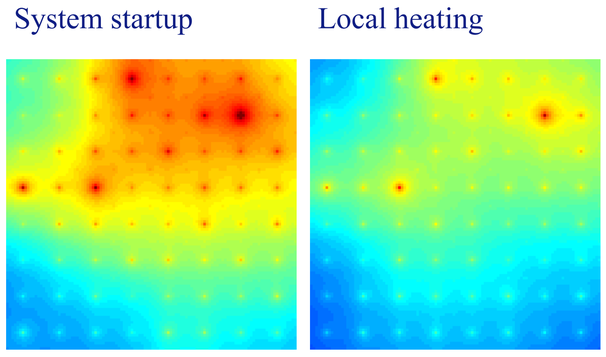
Mapping of processing elements and their associated communication paths within the application scenario of an 8x8 Noc.

Temperature simulation



System startup

Local heating



Remapping of CPU

Frequency and voltage scaling

Future Work

- Adjusting electrical parameters
- Investigations on accuracy vs. simulation speed
- Integration into existing NoC simulators
- (Acceleration using graphic processing units)

- Evaluation of:
  - Control algorithms
  - Mapping algorithms
  - Routing algorithms

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