Cadence + AMS-Hitkit

Totorial for creation of an inverter cell from schematic to layout with CADENCE using AMS-Hitkit and hints for multi-input gates

1. Using the Linux (CentOS) environment
2. Starting CADENCE with AMS-Hitkit
3. Creating a new library
4. Schematic entry
5. Creating a symbol and a testbench
6. Spice-Simulation using ADE XL
   - Analyses selection and setup
   - Using global variables
   - Parametric simulation
7. Starting Layout XL
   - Generate layout from schematic
   - The layer window
   - Wires, vias/contacts, wells
8. Design rule check
9. Layout versus schematic check (LVS)
10. Parasitic extraction (QRC)
11. Simulation of the extracted model (Post-layout simulation)

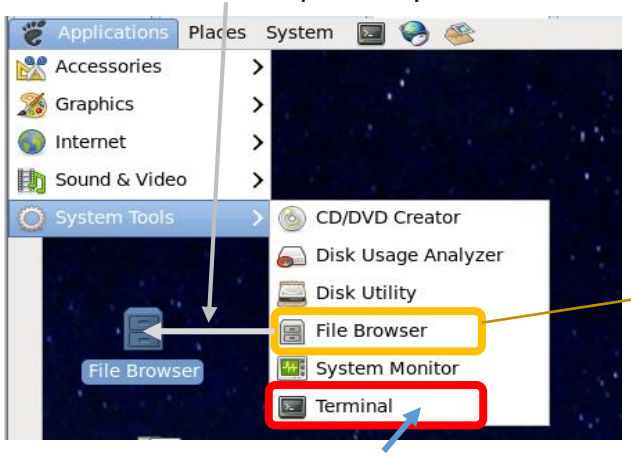
Some UNIX-commands

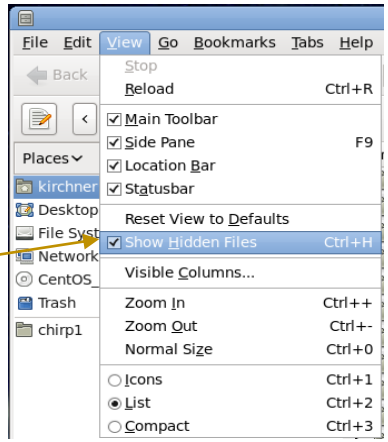
We use CentOS-Linux (Free version "**C**ommunity **Ent**erprise **OS**" of RedHat), because Cadence supports RedHat or Suse.
We use the Kornshell (ksh), because it is the standard shell at ITMZ Uni Rostock.

Our client computers use the "supported" CentOS 6,
but the server is CentOS 7 (not yet supported to run Cadence)

pwd	print working directory
ls, ls –alsi, ls *dir*	list
cd -> cd /~/ske -> cd ./ske	change directory
mkdir *newdir*	make directory
cp , cp -r, cp -p	copy files/directories (recursive, preserve attributes)
mv	move or rename directories
chmod, chmod –R chmod 744 *file*	change file mode bits (security) -> -R recursive
grep	filter for pattern
use of | for pipeline -> ls | grep *pattern*	use command output as input for next command
rm, rm –r	remove/delete
rmdir	remove directory
cat file	show file at standard output
man *cmd*	show manual of cmd

Move icon to desktop for easy use





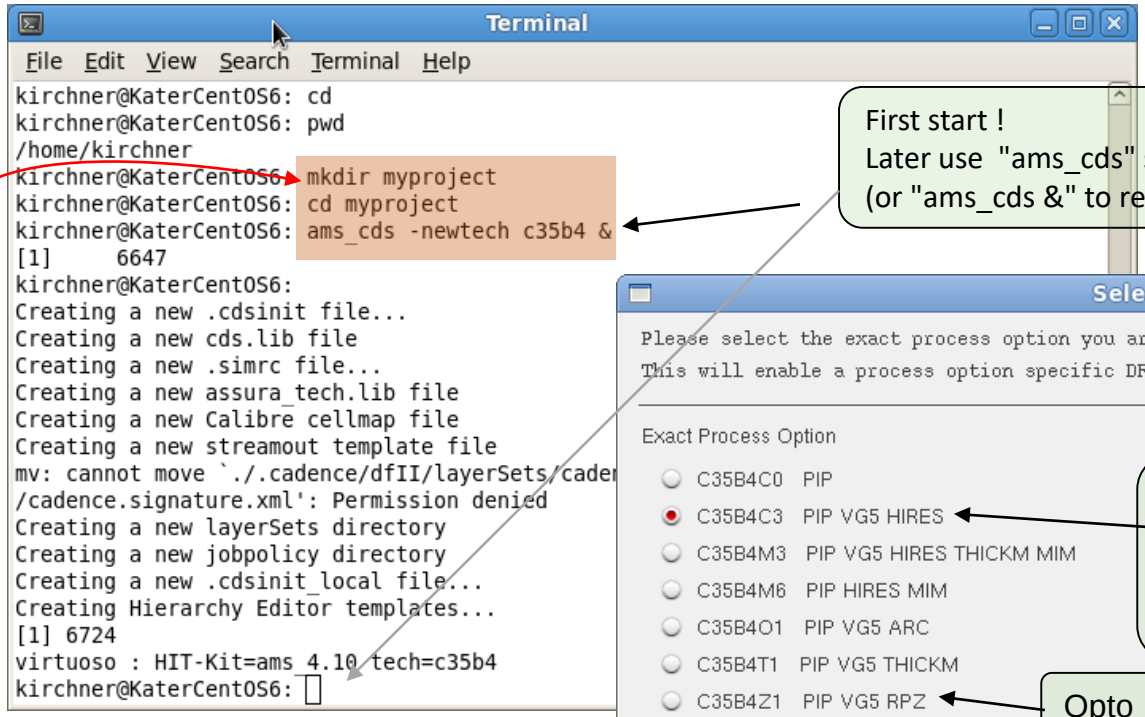
Or Right-Mouse on Background and select "Open Terminal"

To save windows images (.png) : Alt-Print

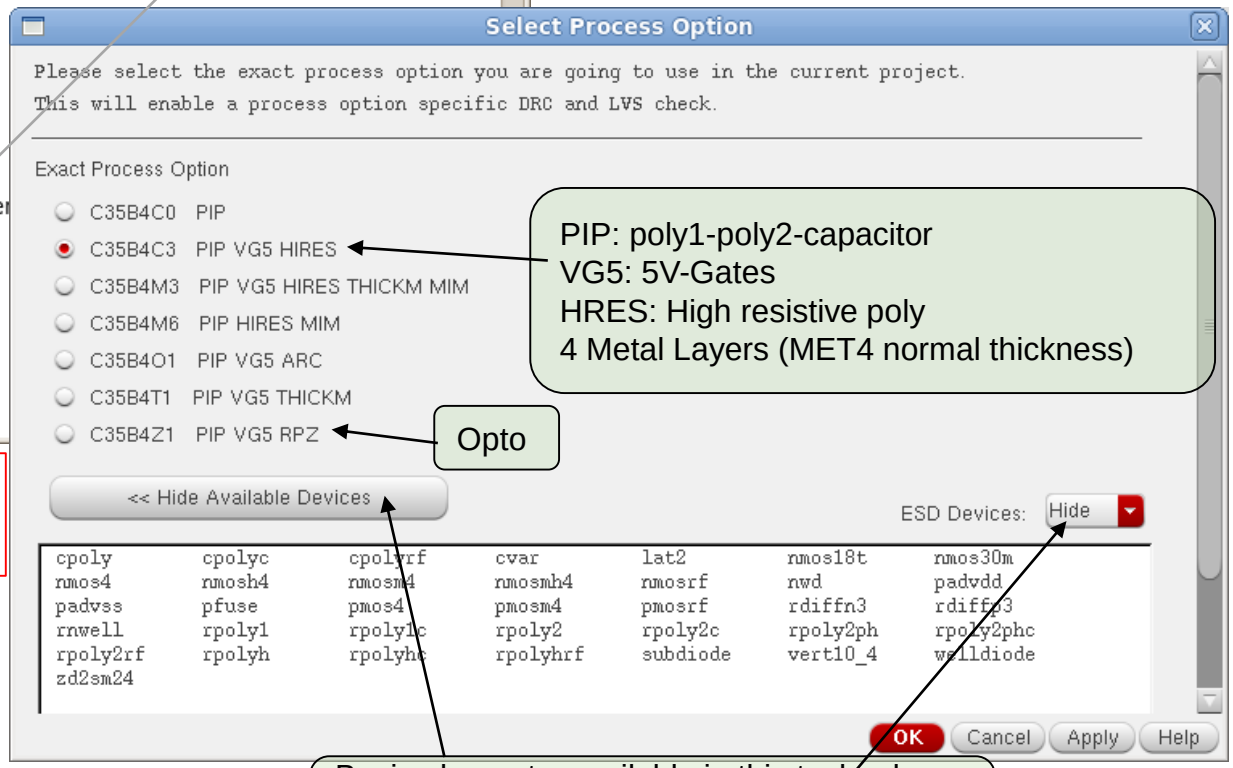
Unix-command to remove Cadence lock files (Close all Cadence programs before!) **: find ~/ -name "*.cdslck" -exec rm {} \;**

AMS-HitKit - Start

= Starting Cadence Design Framework with Libraries, Rules, Scripts provided for AMS-technology



First start !
Later use "ams_cds" simply!
(or "ams_cds &" to release the terminal for further use)



PIP: poly1-poly2-capacitor
VG5: 5V-Gates
HRES: High resistive poly
4 Metal Layers (MET4 normal thickness)

Opto

Do not use your homedir!
Create a separate project directory!

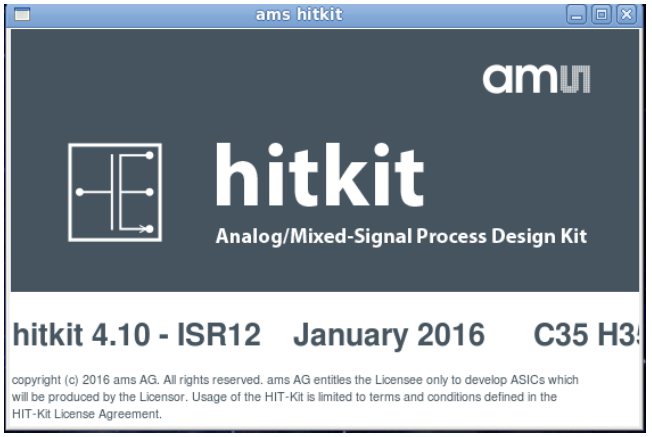
Make your favourite directory structure
~/ske
~/ske/inverter

Basic elements, available in this technology
Show additional elements for ESD
Electro**S**tatic **D**ischarge

You may use one single directory for different designs.

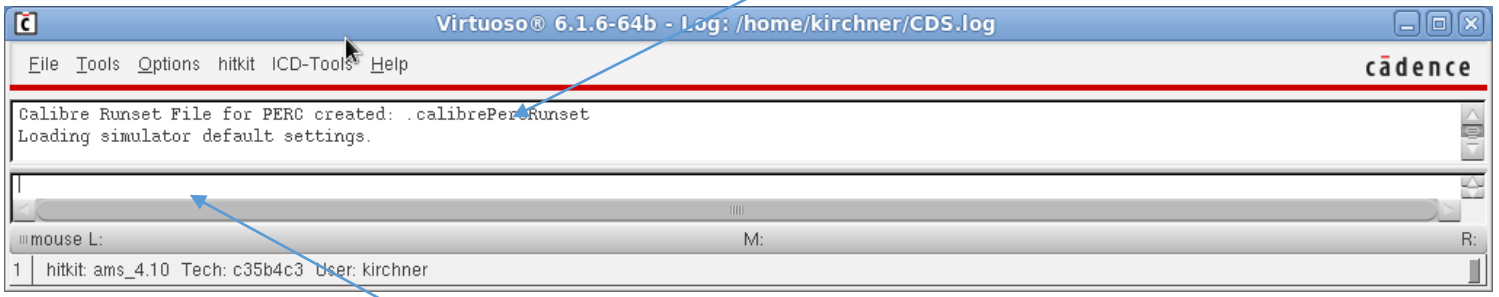
AMS-HitKit - Start

Would stay open as long as ams_cds is running



Window open for some seconds after ams_cds start

Command Interpreter Window - CIW



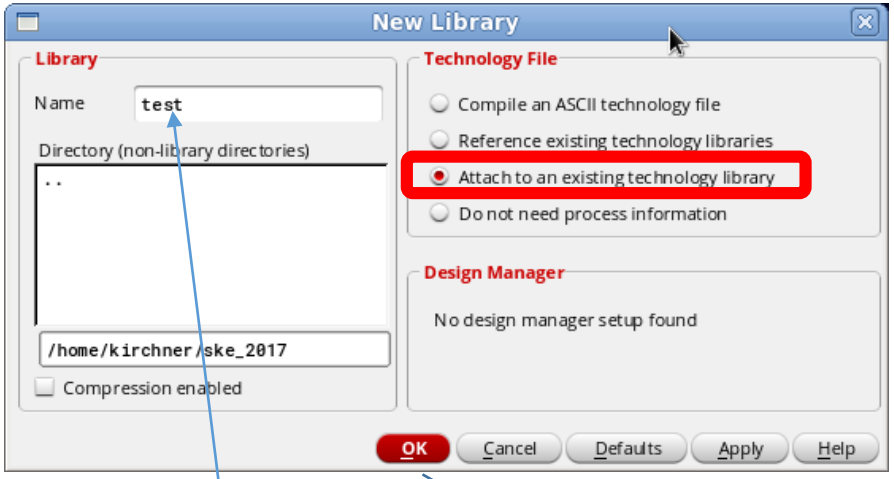
Messages

Command Inputs

AMS-HitKit - A new library

Command Interpreter Window - CIW

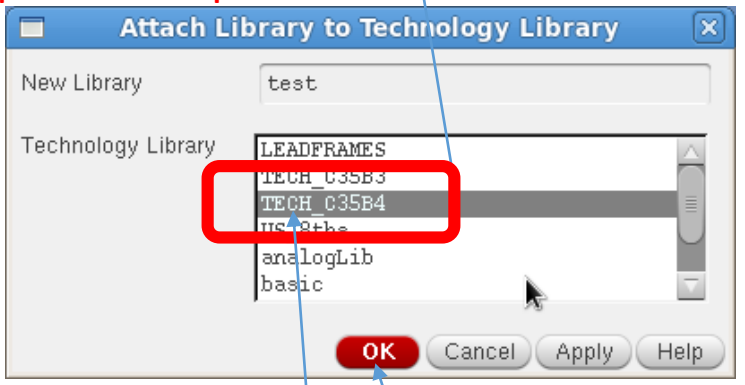
File -> New -> Library



Choose a name for your library!
(You may use one library for different designs.)

Select
"Attach to an existing technology library" -> OK

important step!



We use the 4 metal layer technology here.
Do not press OK before you have selected the TECH-library!

Quit with OK!

AMS-HitKit - A new cellview

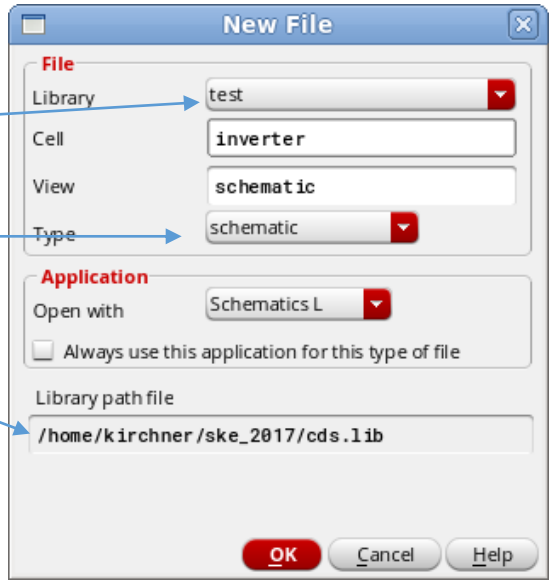
Command Interpreter Window CIW

File -> New -> Cellview

Your new library

Start with schematic view

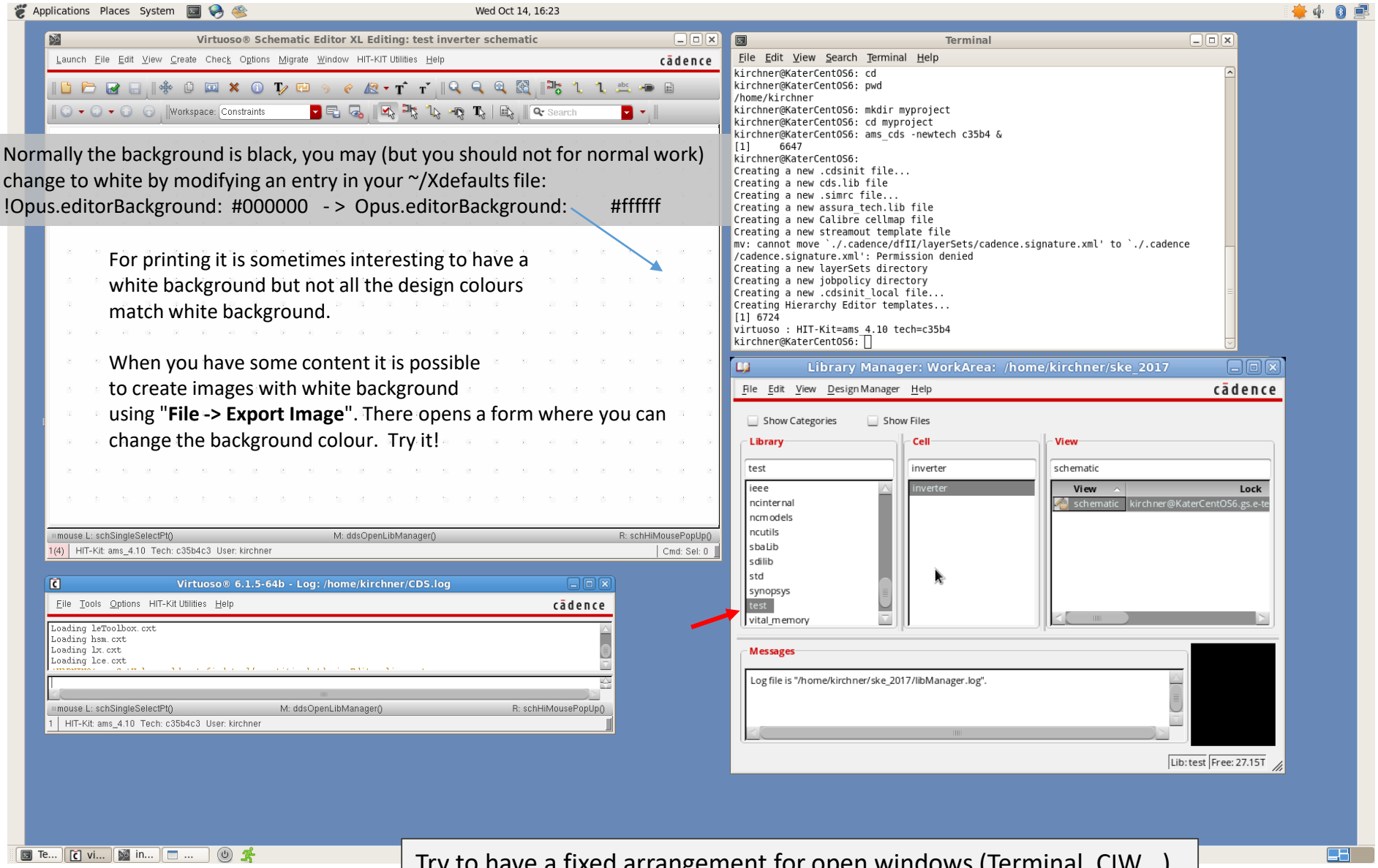
Depends on your project path



Choose a cell name, check "schematic" as cellview -> OK

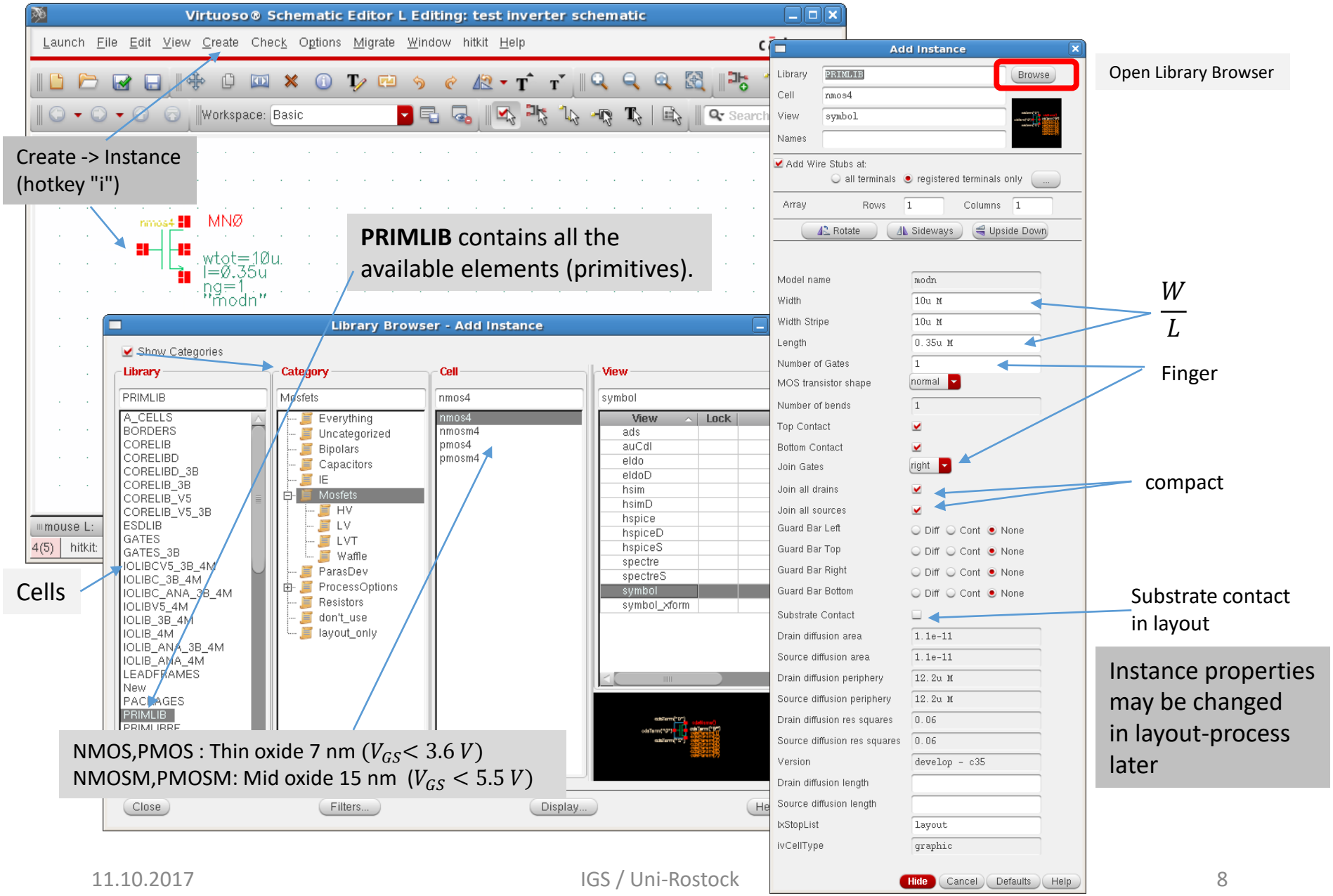
Quit with OK !

AMS-HitKit Schematic Editor is open

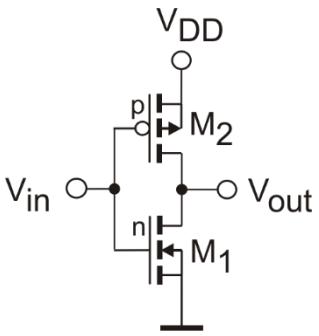


Try to have a fixed arrangement for open windows (Terminal, CIW ..)

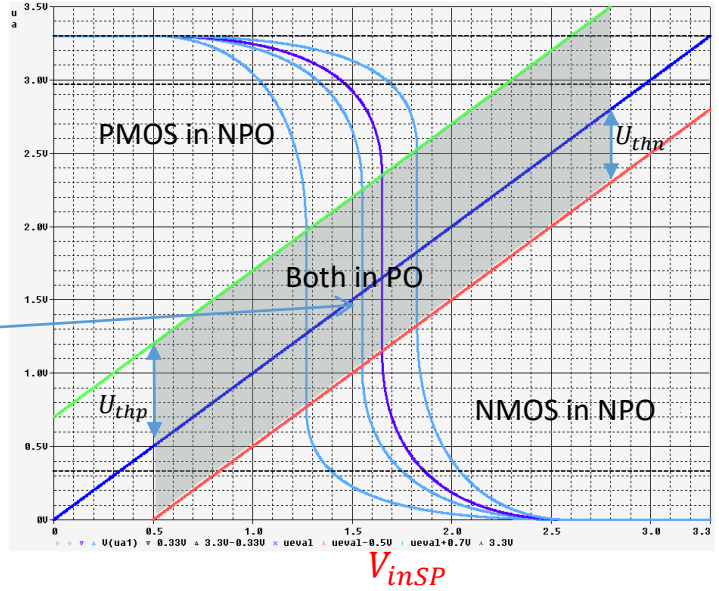
Schematic entry - Components



CMOS Inverter calculation



There is the same current flowing through both transistors.Beide. For ideal switching point is $V_{in} = V_{GSn} = V_{SGp} = V_{out} = V_{DSn} = V_{SDp} = \frac{V_{DD}}{2}$.
Because of $|V_{DS}| > |V_{GS} - V_{th}|$ both transistors are in the pinch-off state and we can assume:



$$\frac{\beta_n}{2}(V_{inSP} - V_{thn})^2 = \frac{\beta_p}{2}(V_{DD} - U_{inSP} - U_{thp})^2$$

$V_{thn} = 0.5\text{V}, \text{KPN} = 170\ \frac{\mu A}{V^2}$

$V_{thp} = 0.65\text{V}, \text{KPP} = 58\ \frac{\mu A}{V^2}$

Dissolving for V_{inSP}:

$$\sqrt{\beta_n}(V_{inSP} - V_{thn}) = \sqrt{\beta_p}(V_{DD} - V_{inSP} - V_{thp})$$

$$V_{inSP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{thn} + V_{DD} - V_{thp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

For desired $V_{inSP} = \frac{V_{DD}}{2}$ we calculate the relation $\frac{\beta_n}{\beta_p}$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - U_{thn}}\right)^2$$

$$\beta = KP \cdot \frac{W}{L}$$

using: $KPN = 3 \cdot KPP$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}}\right)^2 \approx \frac{1}{3}$$

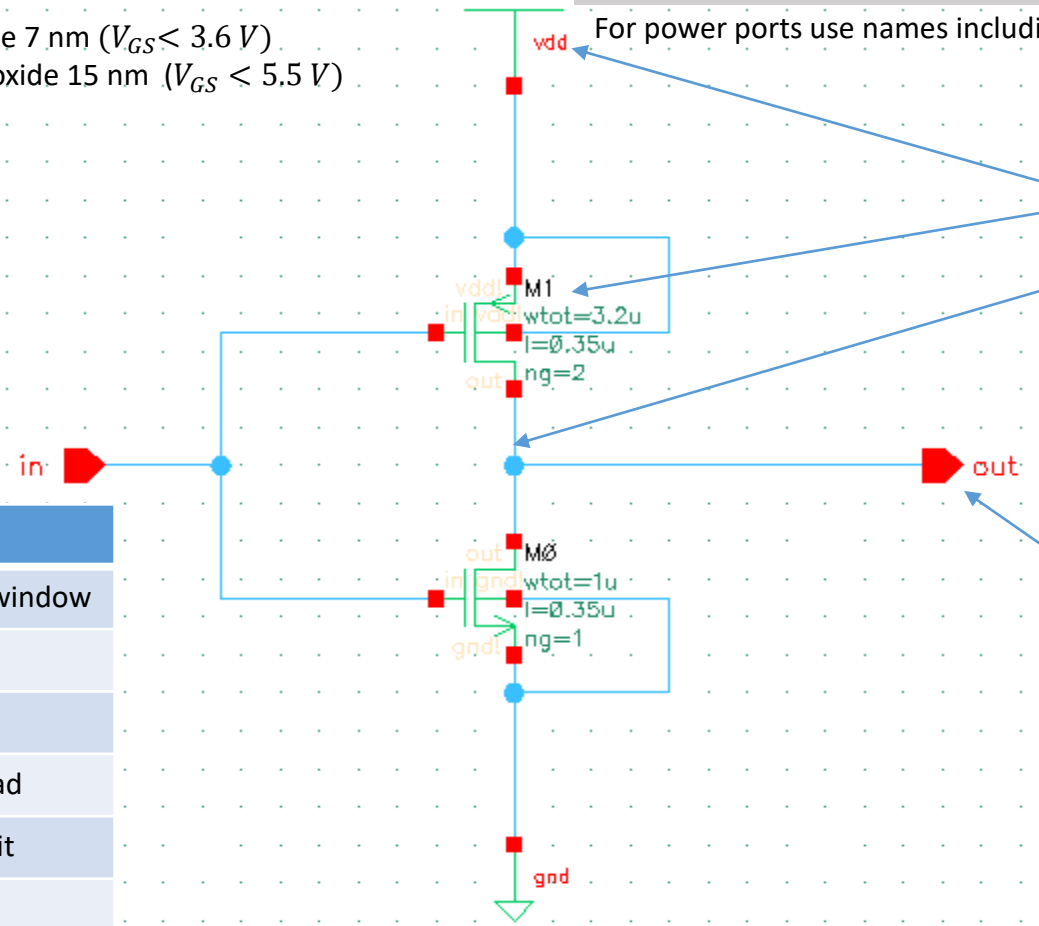
for $|V_{DD}| \gg |V_{thp} - V_{thn}|$

Inverter schematic

NMOS,PMOS : Thin oxide 7 nm ($V_{GS} < 3.6\ V$)
NMOSM,PMOSM: Mid oxide 15 nm ($V_{GS} < 5.5\ V$)

vdd, gnd etc. from library "**analogLib/**globals"

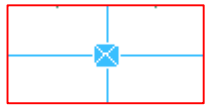
For power ports use names including "vdd" or "vcc"



key	function
i	create instance
w	create wire
M	move
m	stretch (im Layout "S" !)
c	copy
q	object properties
p	add pin
l	add wire name (label)
x	check current cellview
f	fit
]	zoom in
[	zoom out

key	function
F3	show option window
u	undo
U	redo
e	descend & read
E	descend & edit
CTRL-e	return
DEL	delete

For ground ports use names including "gnd".
(Some scripts (ERC) need this naming convention.)

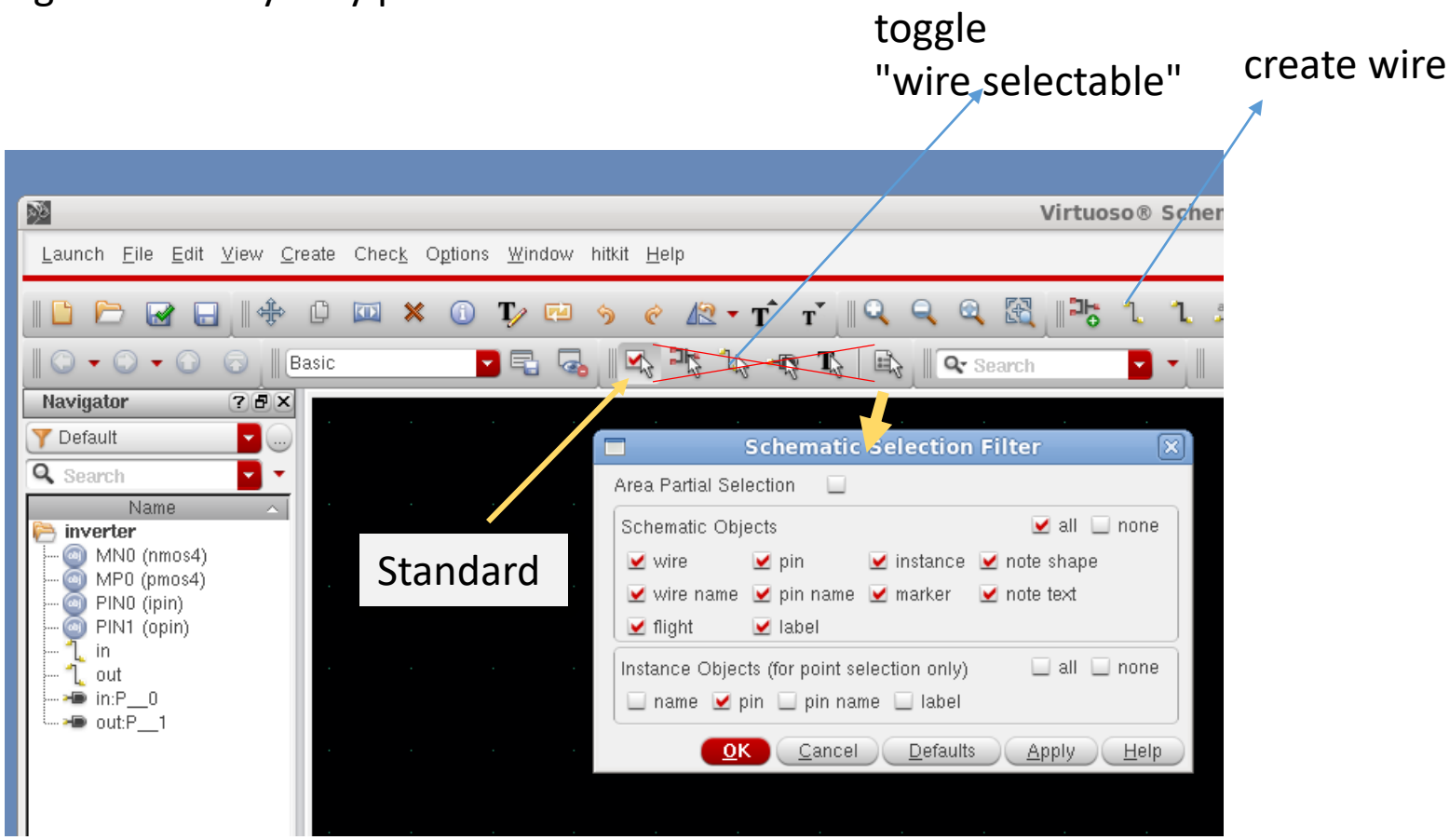


Avoid crossover dots.
Warnings! May be deselected
Check-> Rules-> Physical

File -> Check and Save (shft-x)

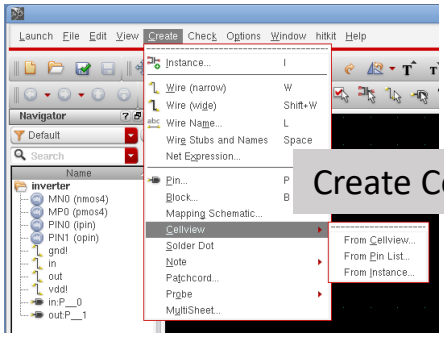
Schematic Editor: Filter

Schematic editor has a filter function for selectable objects!
Changing accidentally may prohibit selection!

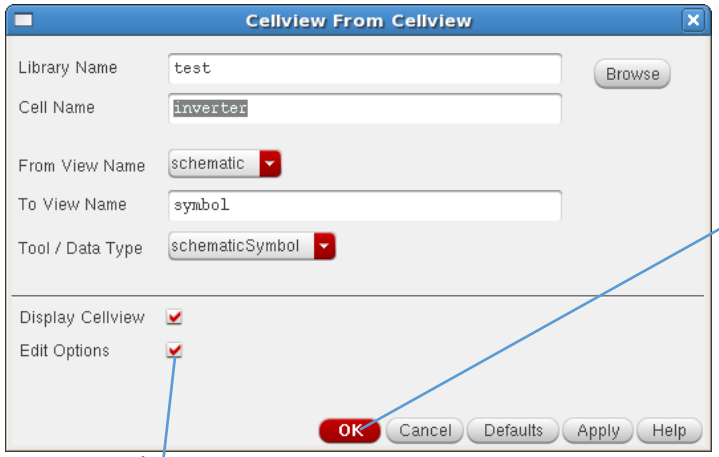


Inverter Symbol from Schematic

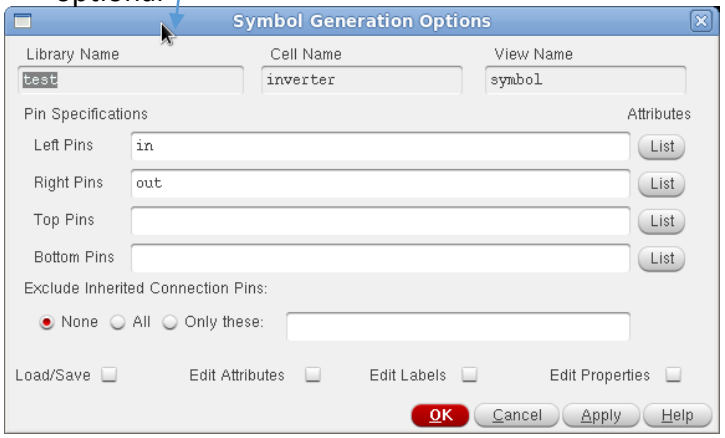
Symbol needed to use our design in higher levels of hierarchy.
First Example is the insertion of the design in a testbench.



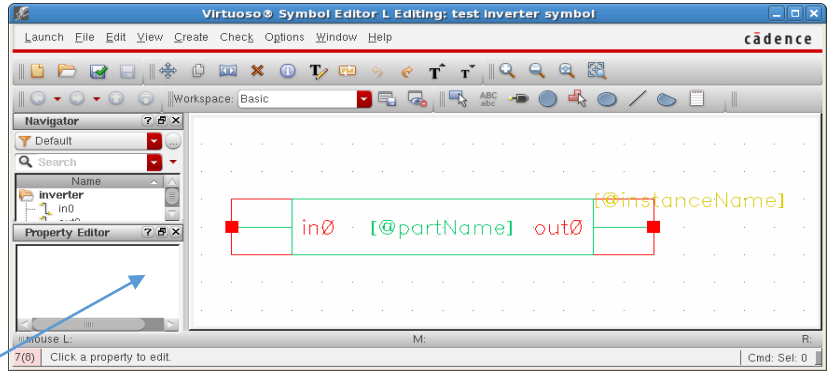
Create Cellview -> From Cellview -> OK



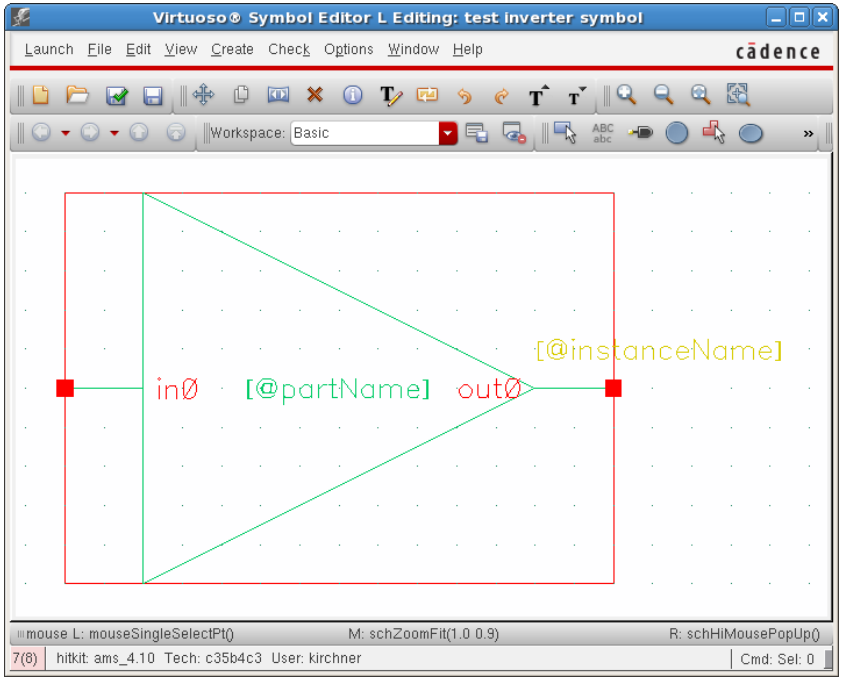
optional



Standard: rectangle

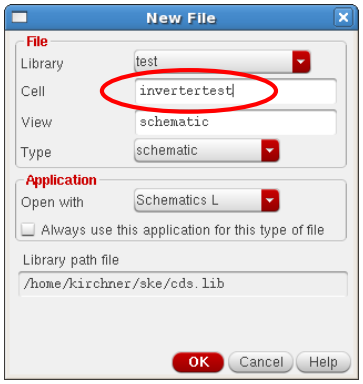


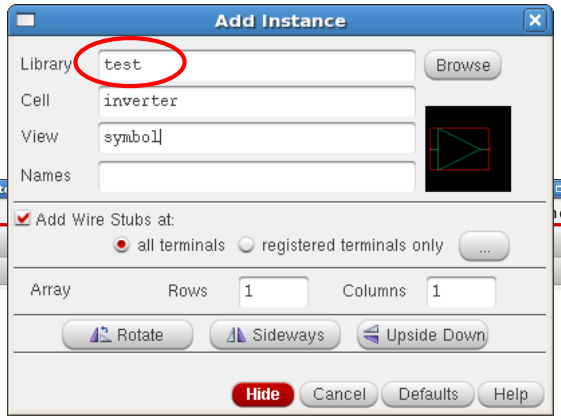
One may change shapes:
outline (green), selection frame (red)
use: stretch, delete,move,create polygon

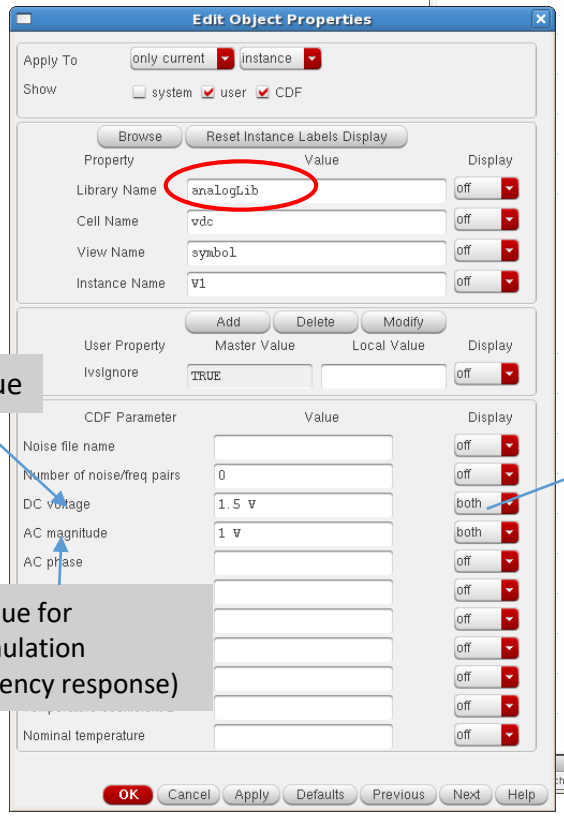


Inverter Schematic for Simulation -> Testbench

In CIW (or Library Manager): File -> New -> Cellview







DC-value

AC-value for ac-simulation (frequency response)

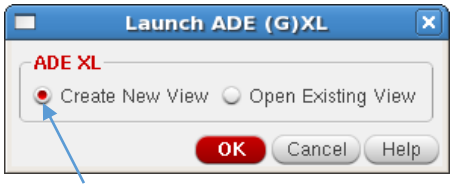
Real value for C?
Answer later.

Simulation ADE GXL Start

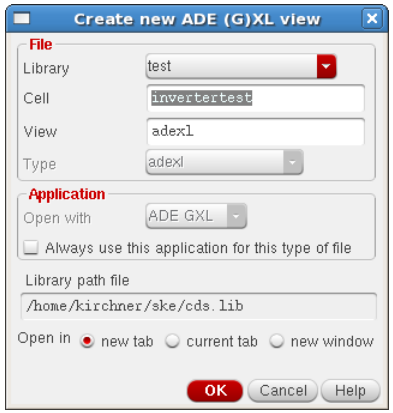
From the Schematic Editor -> **Launch -> ADE GXL**

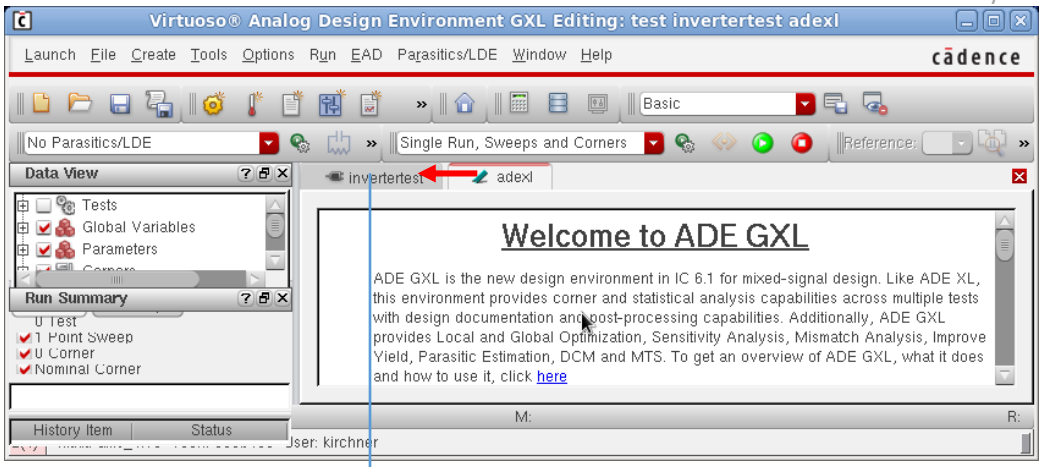
ADE (G)XL usage differs from ADE L
Most tutorials use older ADE L

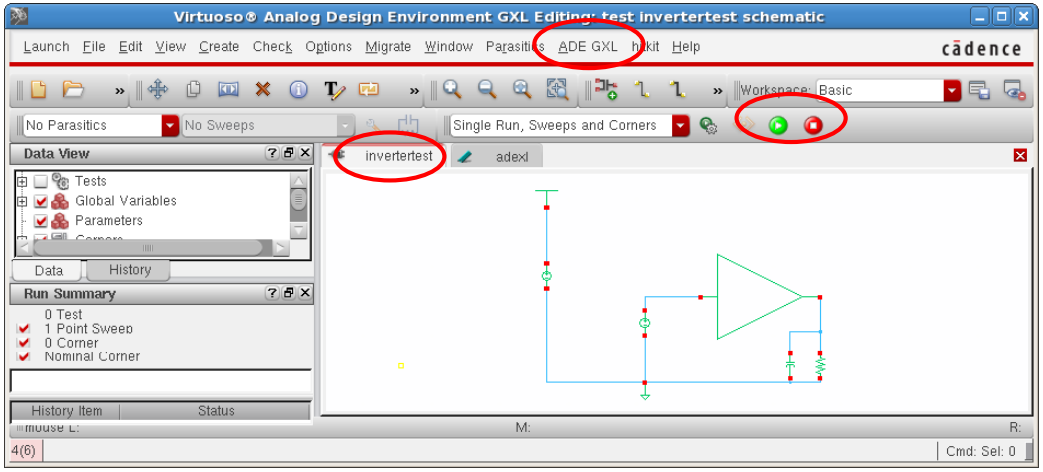
LDE Layout Dependent Effects
EAD Electrically Aware Design



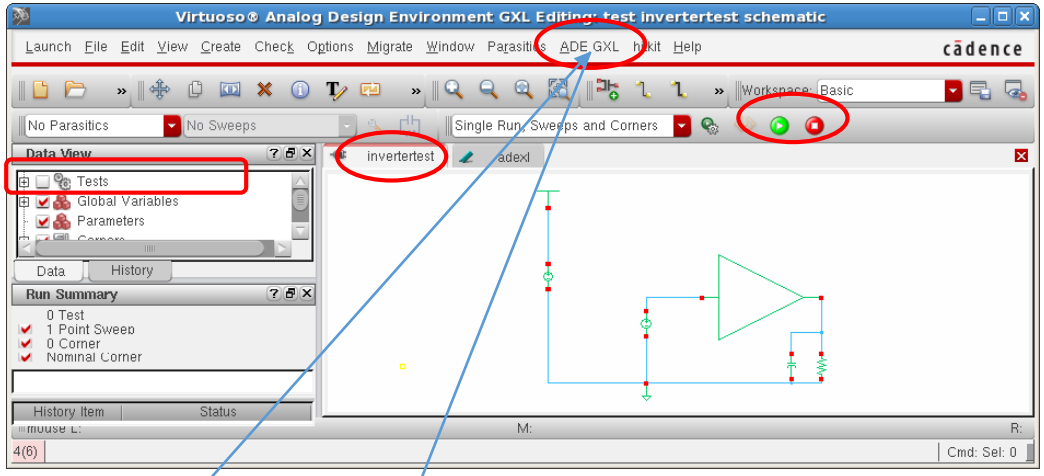
ADE XL creates a new view!



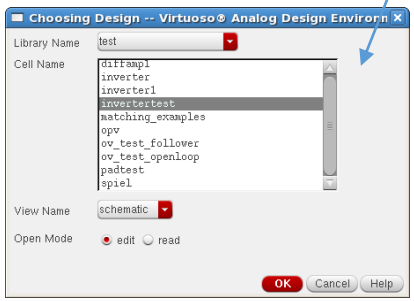


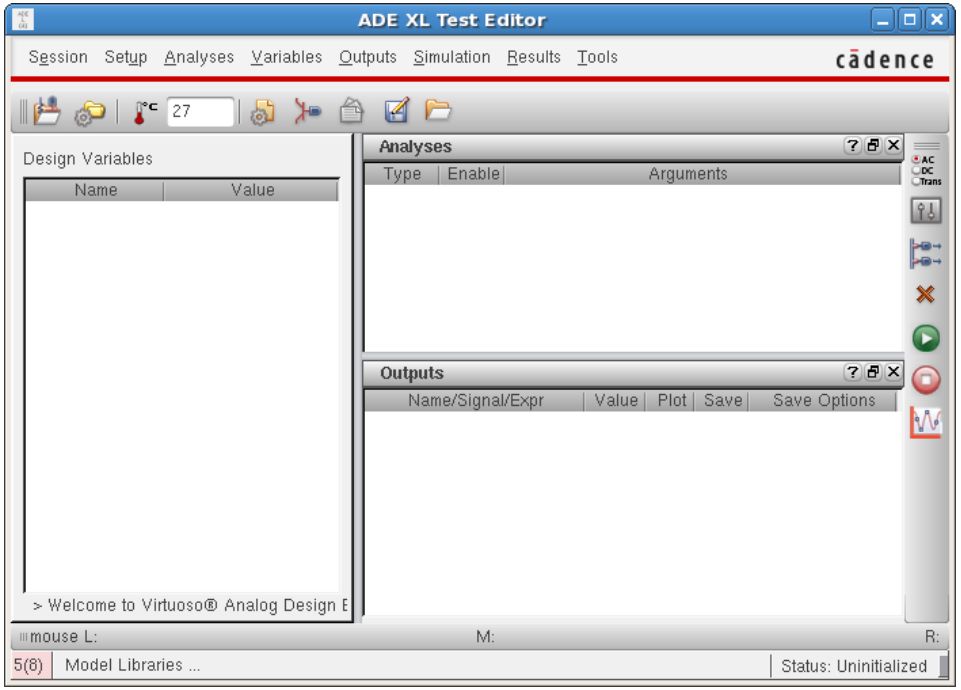


Simulation ADE GXL Create Test

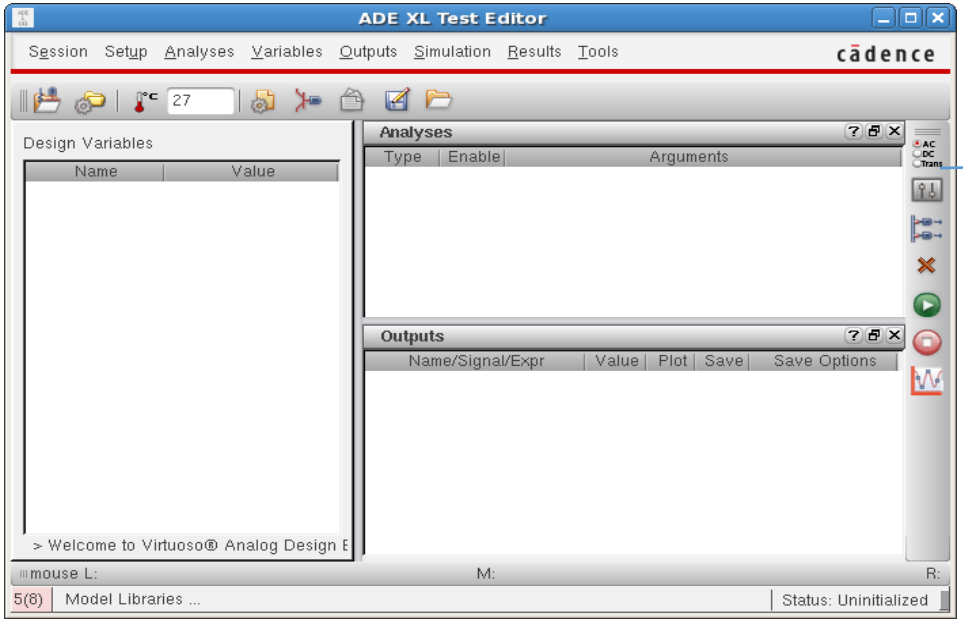


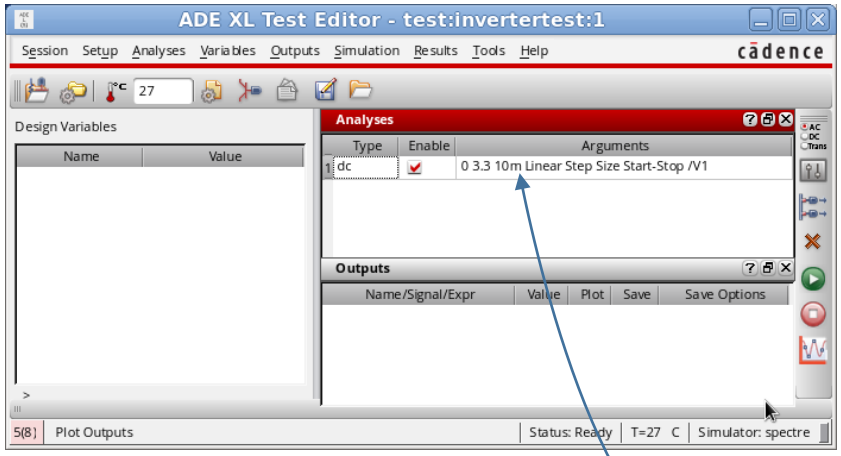
Choose: ADE GXL -> Create -> Test

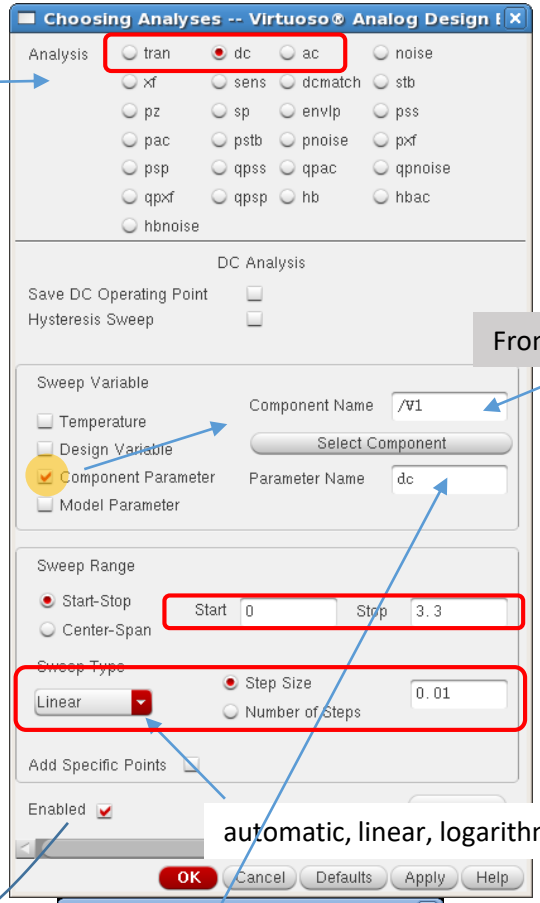




Simulation ADE GXL Create Analyses

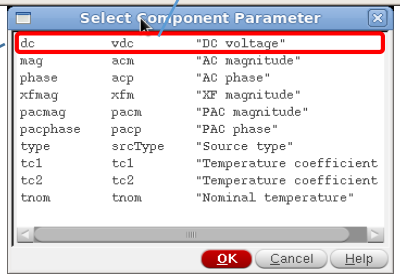






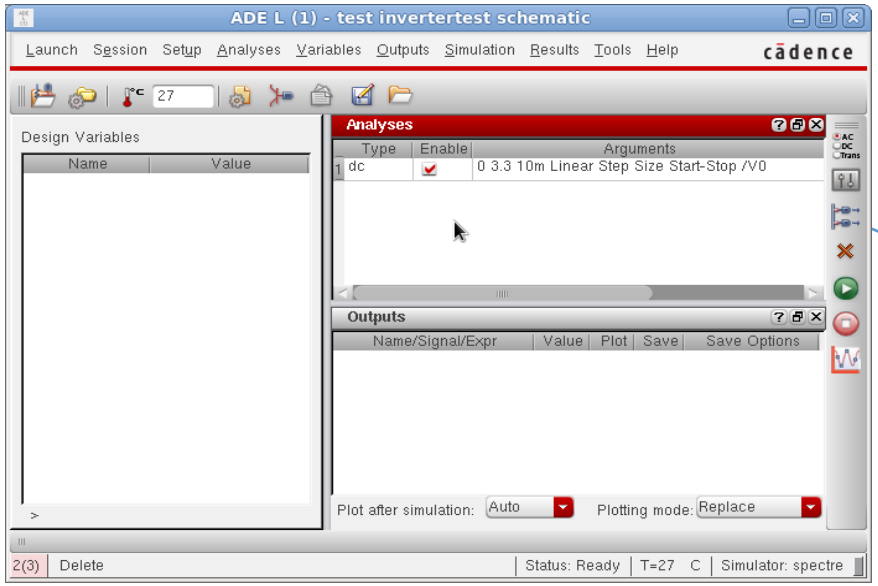
From Schematic

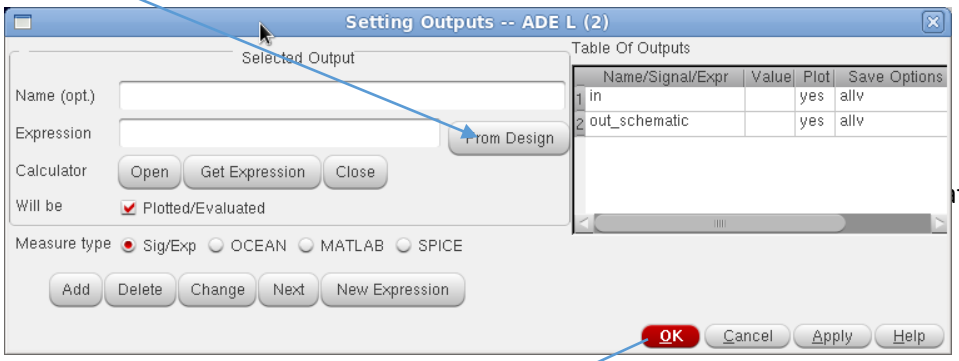
automatic, linear, logarithmic

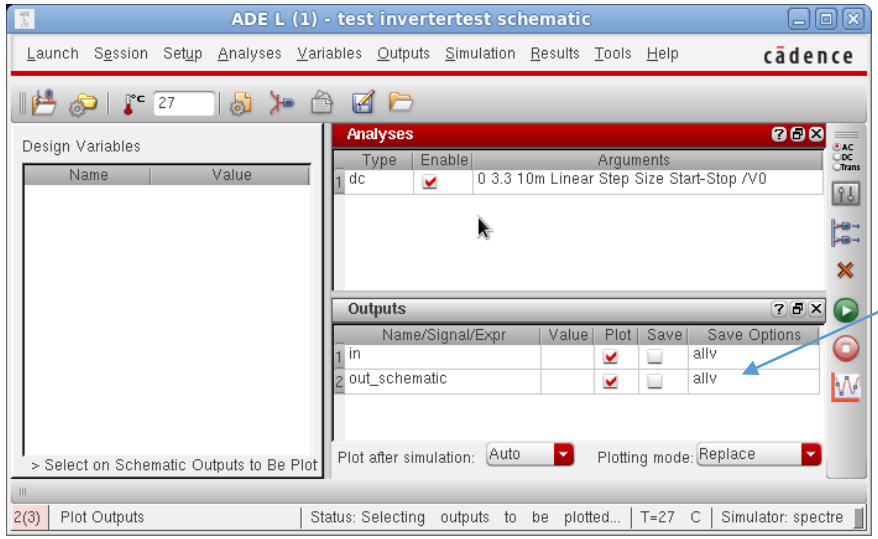


Create/Edit analyses
Design Variables
Simulation Outputs
Delete selected analyses
Run enabled analyses
Stop
Plot

Simulation ADE-XL/L Choose Outputs

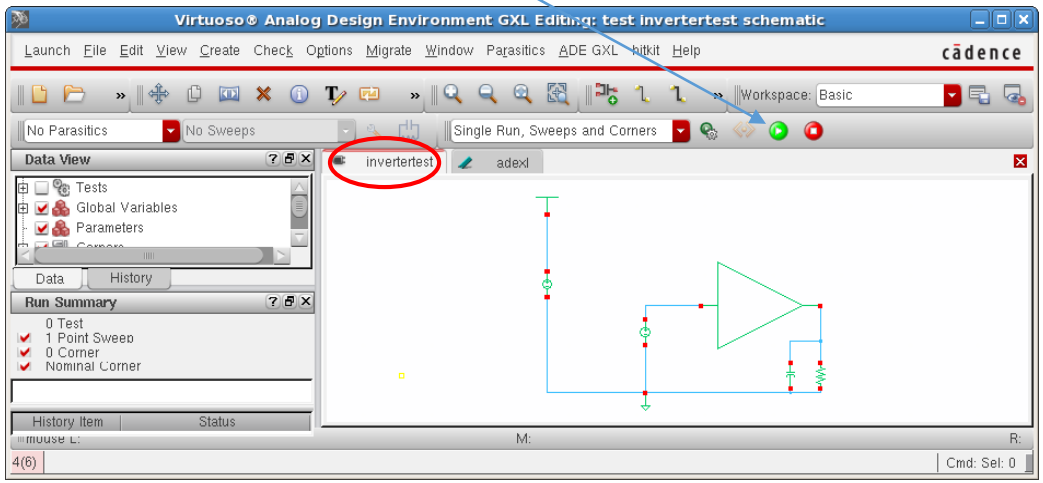






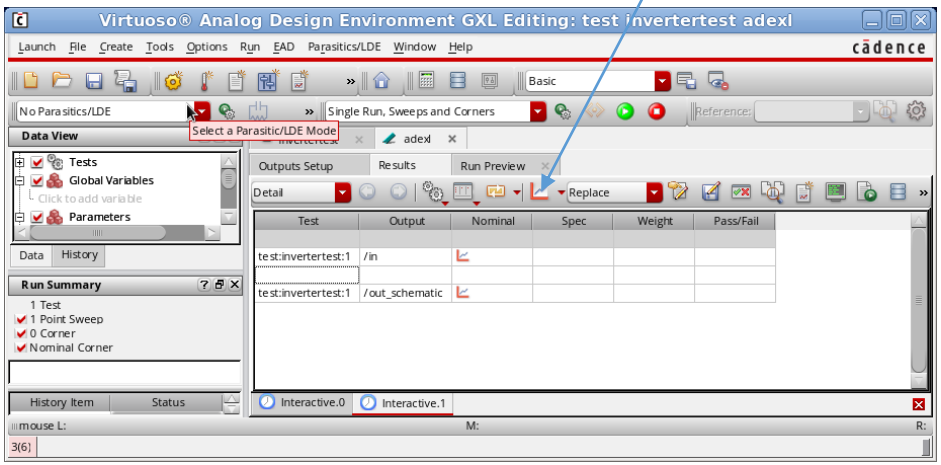
Simulation RUN (in ADE-GXL)

Run Simulation

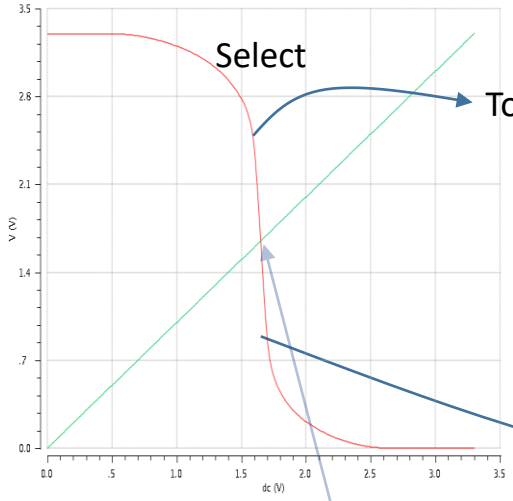


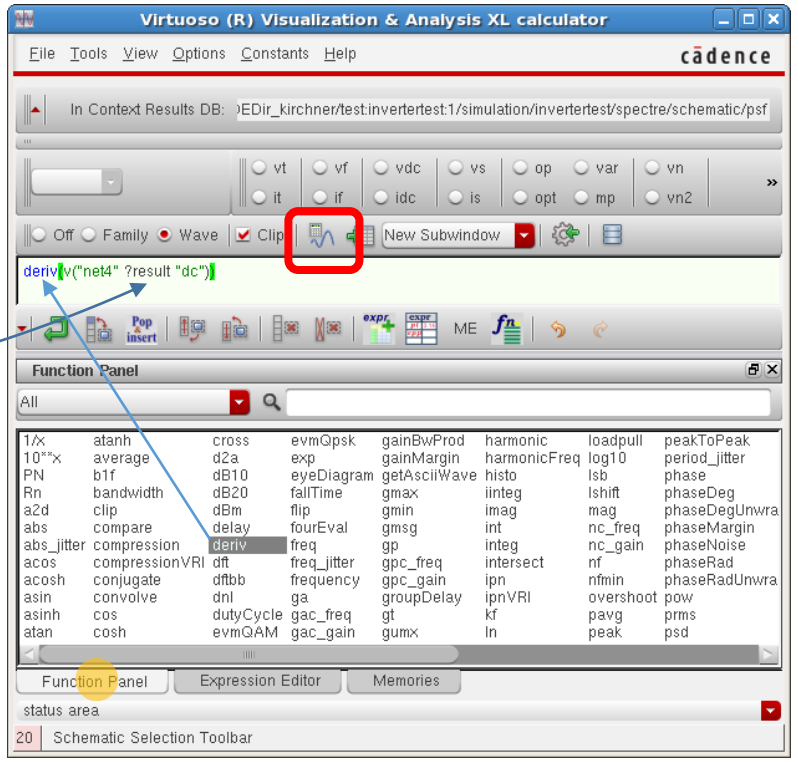
Common Errors stopping execution of simulation:
Design changed and not saved.
Unexpected/unassigned variables due to input errors mostly for component values.
Example: Using "Meg" instaed of "M" for "Mega..
-> Creates a variable "eg"

Plot outputs

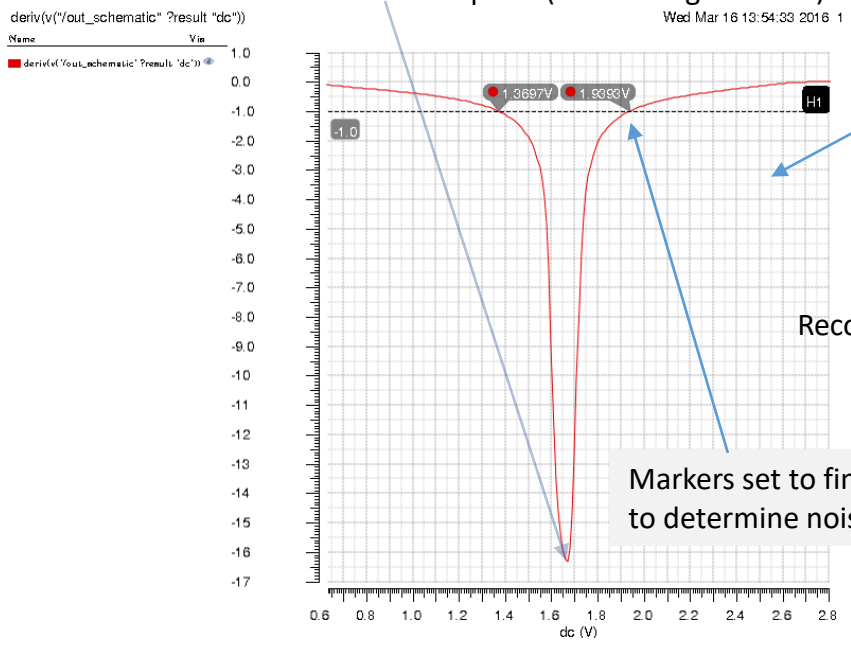


Simulation ADE-L Evaluate Results



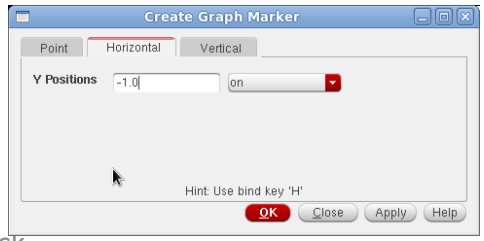


Inflexion point (max. abs. gain value)



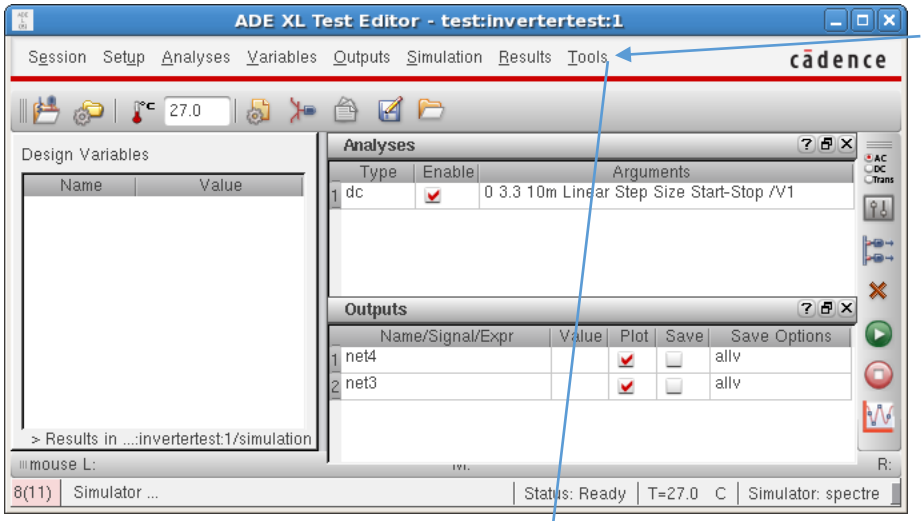
Recommendation: Move derivation plot to new subwindow (RM-> Move to)

In Visualization&Anlaysis Window -> Marker -> Create Marker

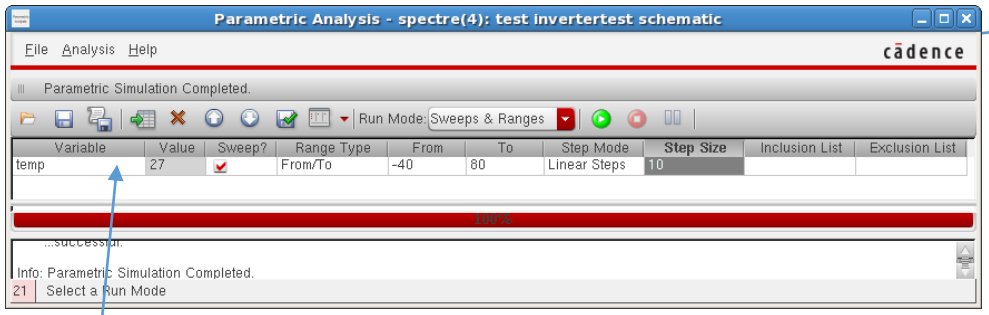


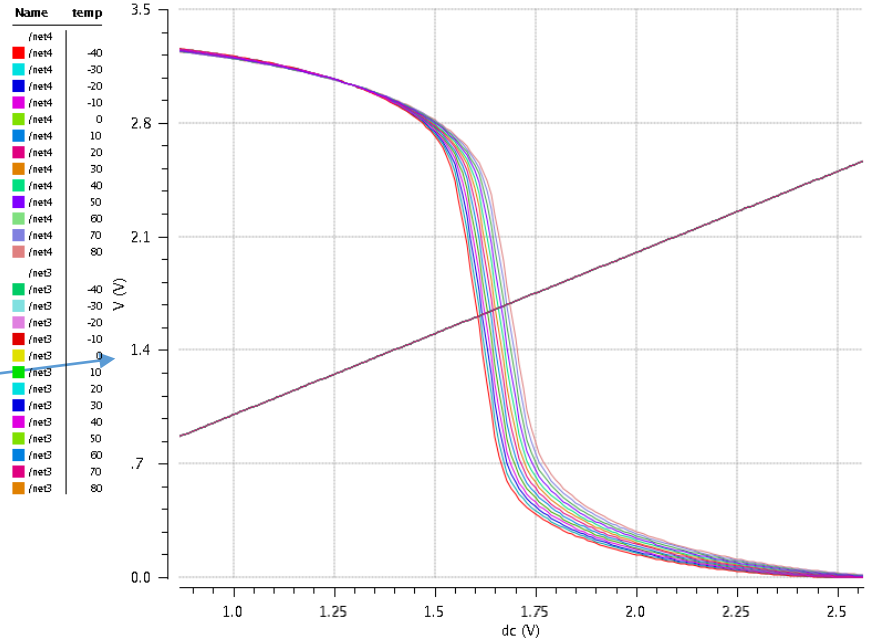
Markers set to find the -1 gain to determine noise margins.

Simulation Parametric Analysis – Temperature (Built in)



Tools -> Parametric Analysis

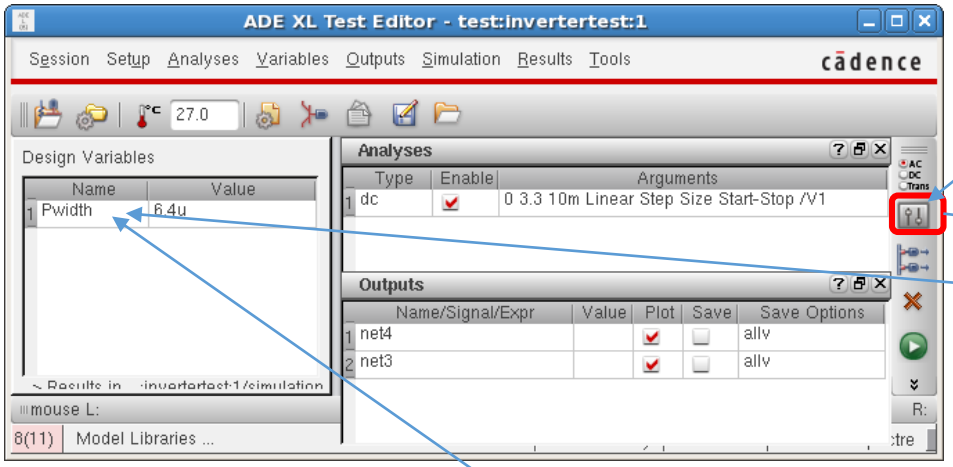




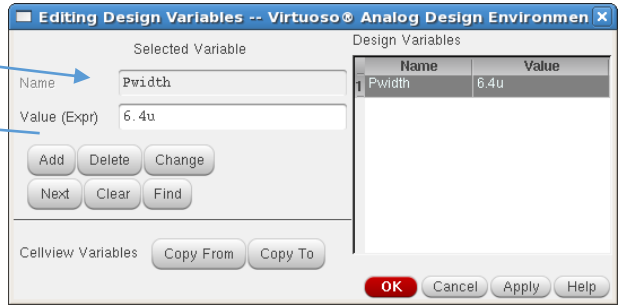
Select "temp" (There is nothing more when you start)!
Try the other entries! Here: -40°C to 80°C in 10° steps)

Simulation Parametric Analysis – Global Variables

As an example we replace the fixed width of the PMOS transistor by a parameter "Pwidth"

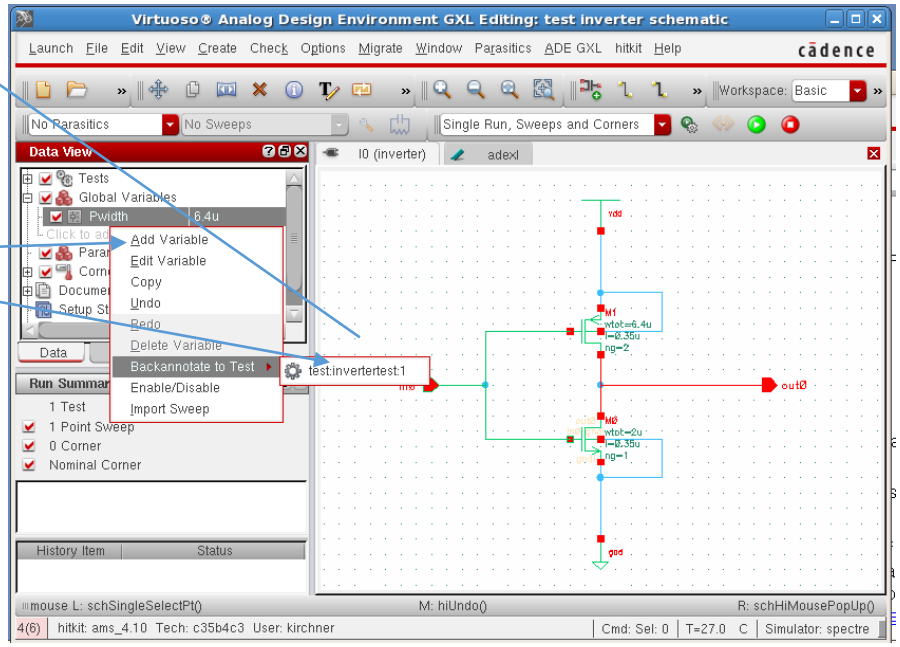


Start here to create a global variable

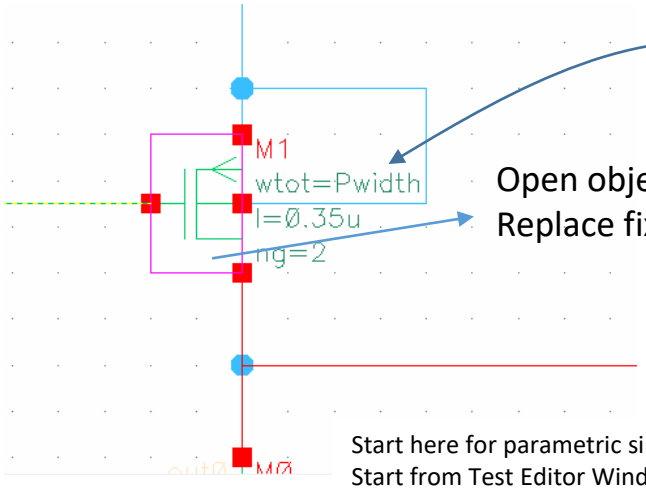


If there is only the testbench schematic open, select inverter and press "E" (descend edit) to open the inverter schematic!

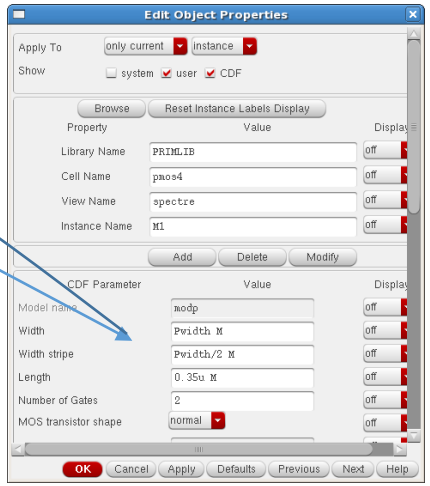
Or start here to create a global variable.
It must be exported/backannotated to appear in test.



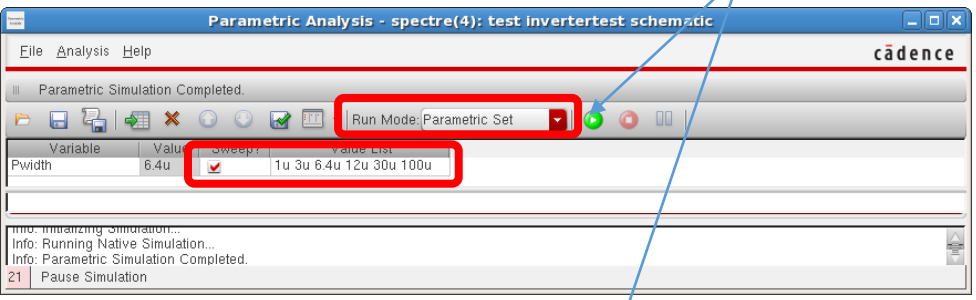
Simulation Parametric Analysis – Global Variables

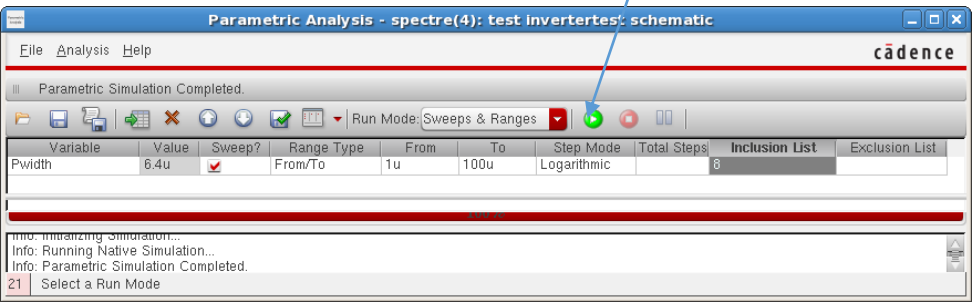


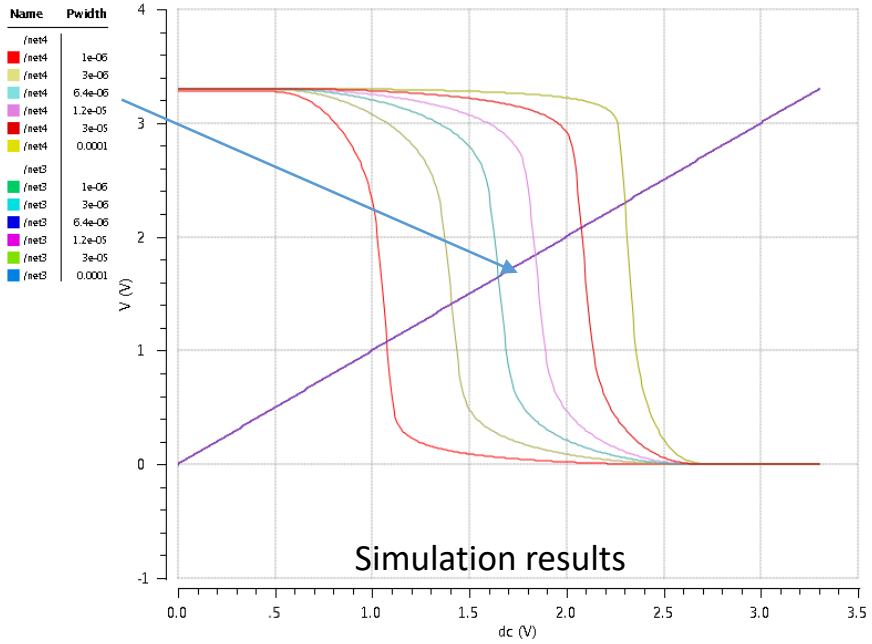
Open object parameters (q)!
Replace fixed value by parameter!



Start here for parametric simulation!
Start from Test Editor Window runs without parametric variation (Default values used).







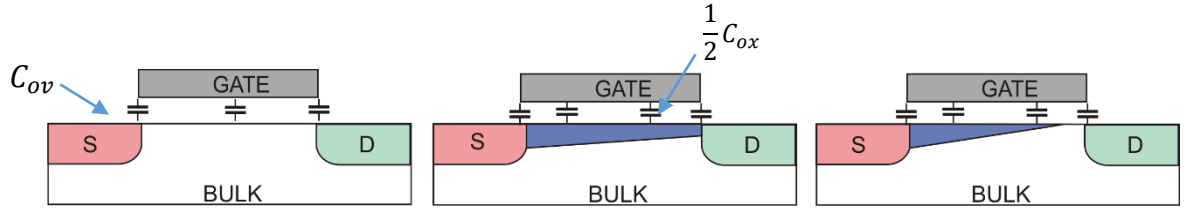
CMOS Inverter Capacitances and Delay

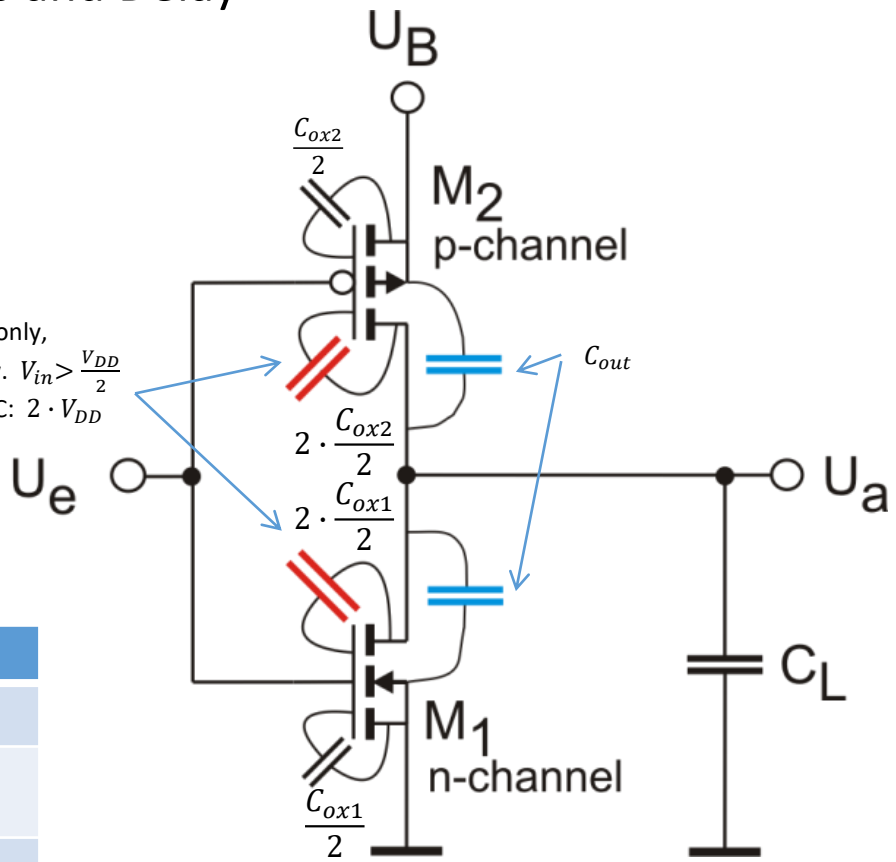
$$C_{in} = \frac{3}{2}(C_{ox1} + C_{0x2})$$

Miller-Capacitor
When will it work? -> only,
if $V_{in} > V_{SP}$, bzw. $V_{in} > \frac{V_{DD}}{2}$
Voltage change over C: $2 \cdot V_{DD}$

Reale Verhältnisse wesentlich komplizierter:
Gate Capacitances zu Drain,Source, Channel, Bulk -> additional $C_{Overlap}$
C_{in} nonlinear:

Region	C_{GB}	C_{GS}	C_{GD}	C_{in}
off	C_{ox}	0	0	$C_{ox} + 2 \cdot C_{ov}$
NPO	0	$\frac{1}{2} \cdot C_{ox}$	$\frac{1}{2} \cdot C_{ox}$	$C_{ox} + 2 \cdot C_{ov}$
PO	0	-> $\frac{2}{3} \cdot C_{ox}$	-> 0	$\frac{2}{3} \cdot C_{ox} + 2 \cdot C_{ov}$

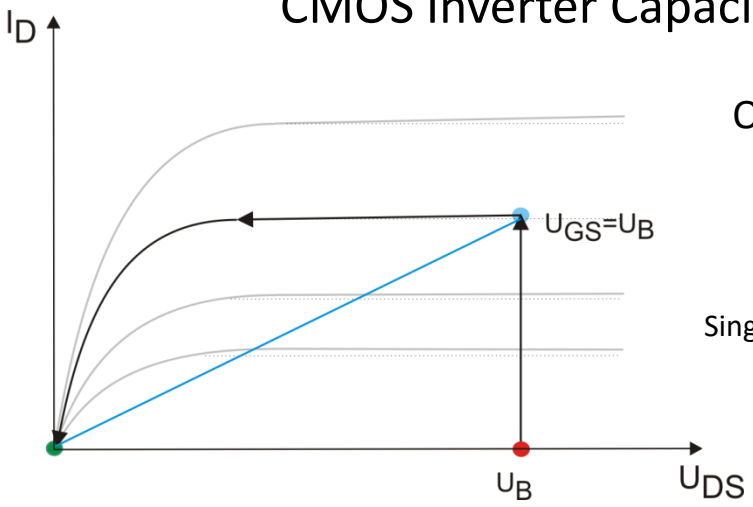




$$C_{out} \approx (C_{ox1} + C_{0x2})$$

Originally the junction capacitance between drain and bulk
In the range of C_{ox} if source and bulk are interconnected
Nonlinear $\sim \frac{1}{\sqrt{V}}$

CMOS Inverter Capacitances, Output Resistance and Delay



Output resistance of FET for charge reversal

Single transistor at V_{DD} with input voltage at V_{DD}

$$I_D = \frac{\beta_n}{2}(V_{DD} - V_{thn})^2 = \frac{KPN}{2}\frac{W}{L}(V_{DD} - V_{thn})^2 = \frac{170\,\mu A}{2\,V^2}\cdot\frac{1\mu m}{0.35\mu m}\cdot(3.3V - 0.5V)^2 = 0.68\,mA$$

$$R_n = R_p = \frac{V_{DD}}{I_D} = \frac{3.3V}{0.68mA} = 4.85\,k\Omega$$

Kapazität und Zeitkonstante -> Delay time (50%-Schwelle)

$$C_{in} = \frac{3}{2}W \cdot L \cdot C'_{ox}$$

$$C_{out} = W \cdot L \cdot C'_{ox}$$

$$C_{in} = 4.5\,\frac{fF}{\mu m^2}\cdot\frac{3}{2}(1 + 3.2)\,\mu m^2 = 28.35\ \text{fF}$$

$$C_{out} = 4.5\,\frac{fF}{\mu m^2}\cdot(1 + 3.2)\,\mu m^2 = 18.9\ \text{fF}$$

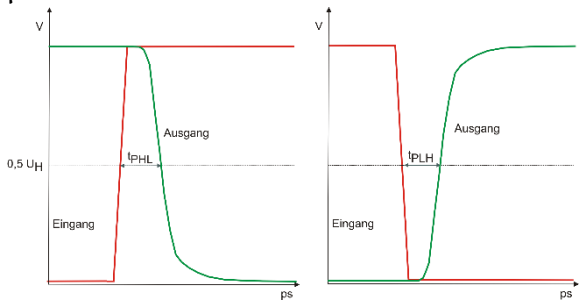
next gate

(+ wire capacitances)

$$t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot \left(C_{inn} + C_{inp} + C_{outn} + C_{outp}\right)$$

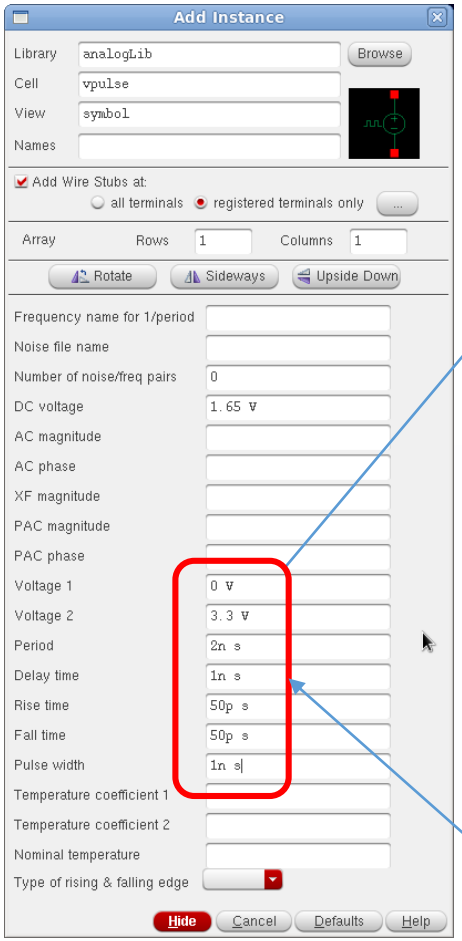
$$t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot C'_{ox} \cdot \frac{5}{2}\left(W_n L_n + W_p L_p\right)$$

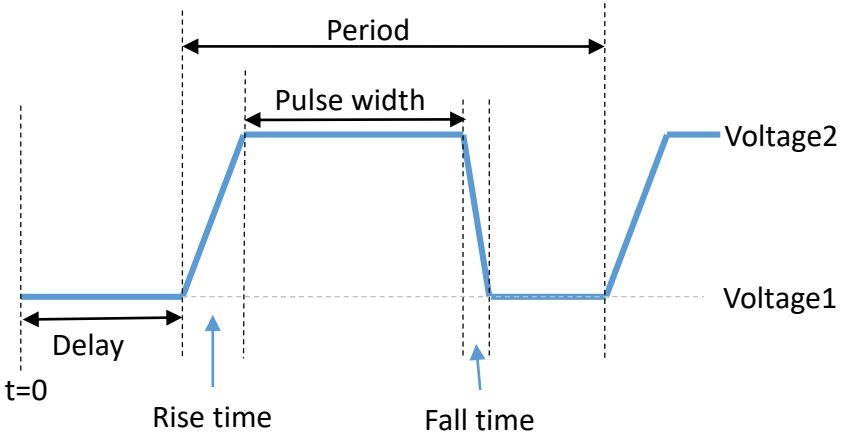
$$t_{pHL} = t_{pLH} = 0.7 \cdot 4.85k\Omega \cdot 4.5\,\frac{fF}{\mu m^2}\cdot\frac{5}{2}(1 + 3.2\,)\mu m^2 = 160\ \text{ps}$$

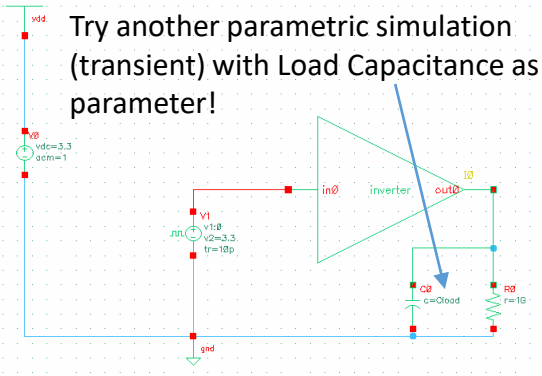


Simulation Transient Analysis

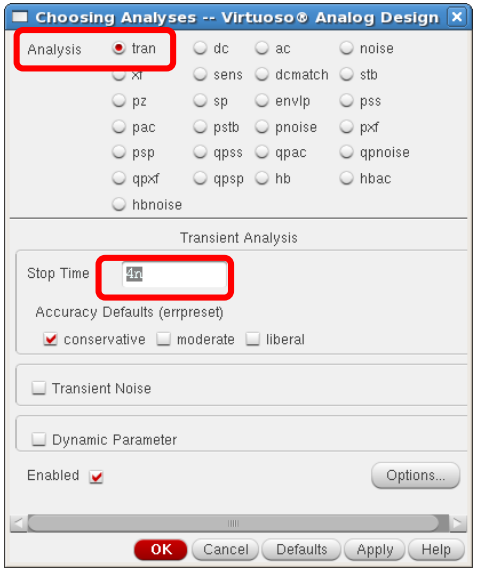
Replace the vdc-source by a vpulse-source. (It would be possible to use this from the scratch even for dc-simulation!)



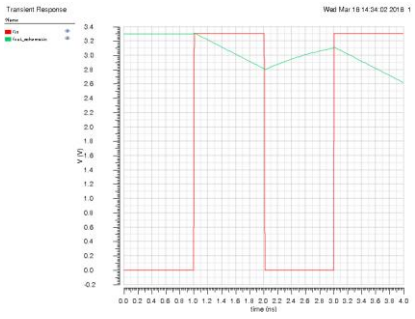




How to find proper time values?

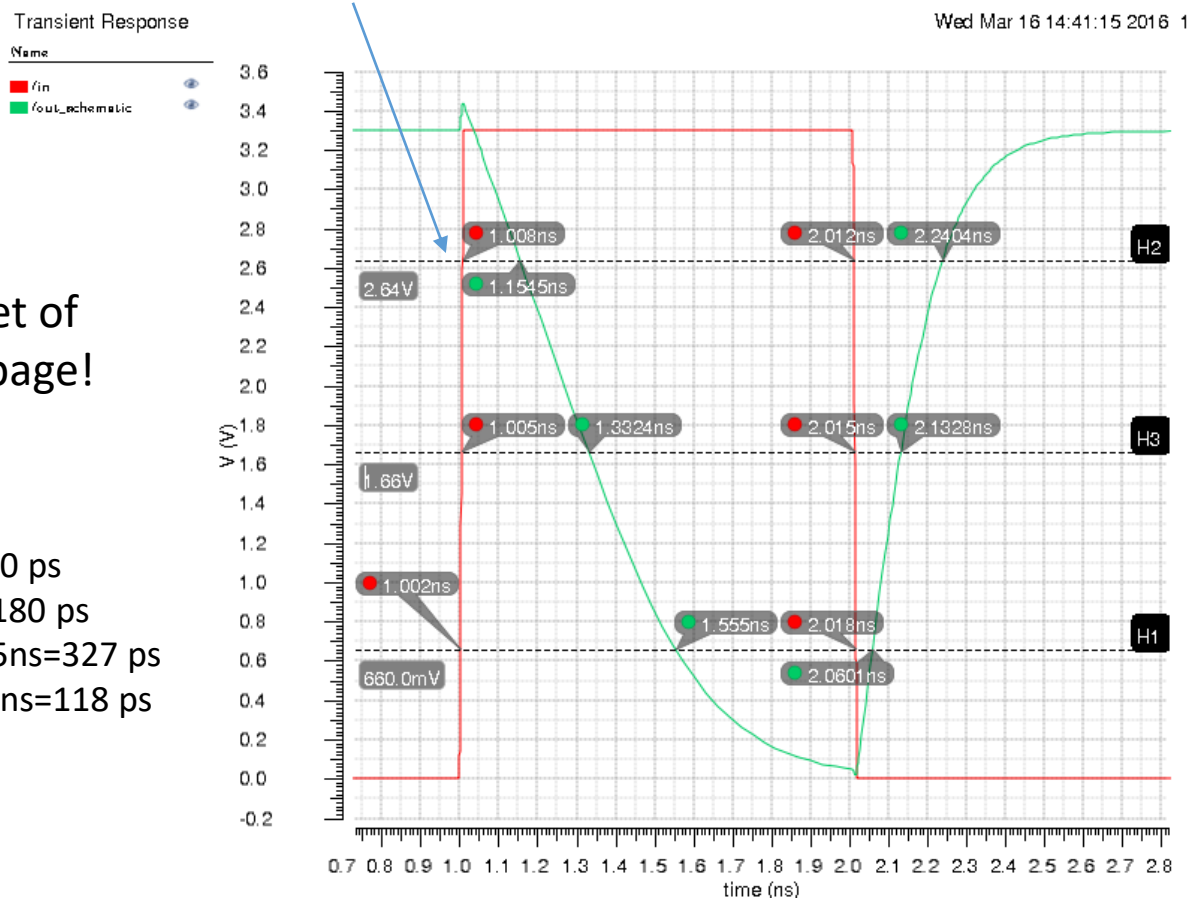


Simulation Transient Analysis



Oops!, looks strange …
1pF load is too much for our small gate

Zur Anzeige der Schnittpunkte: RM auf Markerlinie-> Intercepts -> On

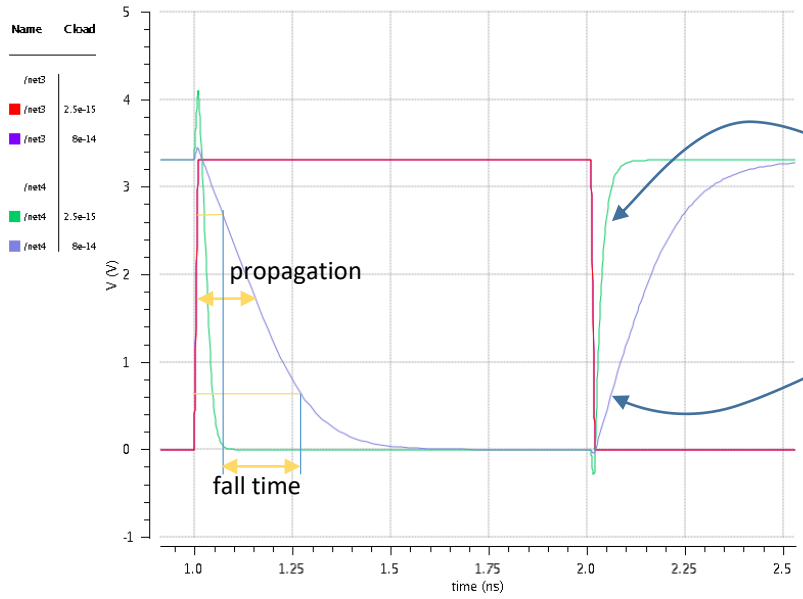


Changed load to 80 fF
Compare with data sheet of ams standard cell next page!

falltime: 1.555ns-1.1545ns=400 ps
risetime: 2.2404ns-2.0601ns=180 ps
delay(inp rise): 1.3324ns-1.005ns=327 ps
delay(inp fall): 2.1328ns-2.015ns=118 ps

Simulation Transient Analysis

Try another parametric simulation with
Load Capacitance as a parameter!
Compare results with a given cell from AMS!



NANGATE INV0 www.ams.com

Databook Build Date: Wednesday Jun 18 17:26 2014
Copyright © 2004-2013 Nangate Inc.
Conditions for characterization library **c35_CORELIB_TYP**, corner **c35_CORELIB_TYP_typical**: Vdd= **3.30**V, Tj= **25.0** deg. C .
Output transition is defined from **20%** to **80%** (rising) and from **80%** to **20%** (falling) output voltage.
Propagation delay is measured from **50%** (input rise) or **50%** (input fall) to **50%** (output rise) or **50%** (output fall).

Cell Area	36.400 um^2
Equation	Q = "!A"
Type	Combinational
Input	A
Output	Q

State Table	
A	Q
L	H
H	L

Propagation Delay [ns]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	0.05	0.53	-0.20	1.07
	rise	0.08	0.94	0.86	2.24

Output Transition [ns]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	0.05	0.71	0.56	1.48
	rise	0.10	1.39	0.54	1.87

Capacitance [fF]	
A	3.8210

Leakage [pW]
0.21

Dynamic Power Consumption [nW/MHz]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	5.98	6.28	160.14	131.01
	rise	34.83	35.09	256.12	205.46

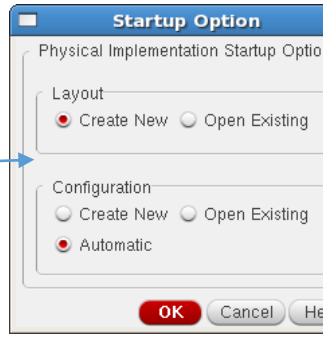
Uups!, explain the negative value!

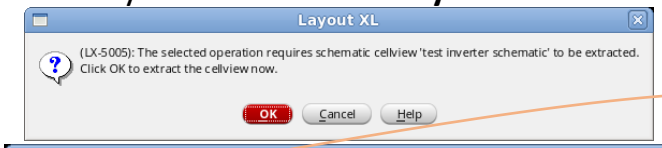
Layout Start and Generate from Schematic

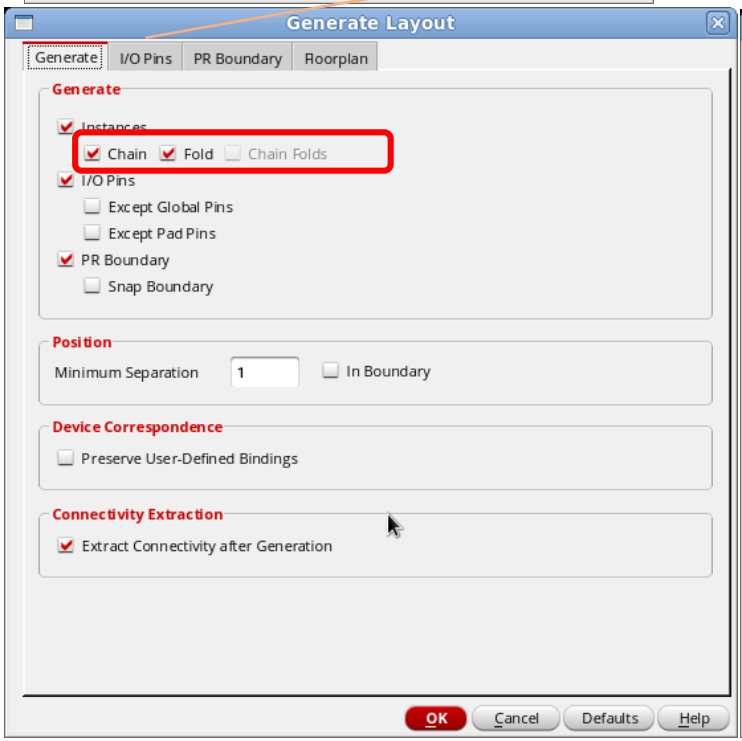
Replace all the global variables in the design with fixed values.
Global variables have their scope in simulation only.
Global Variables in the testbench are not affected, because they will not be involved in the layout.

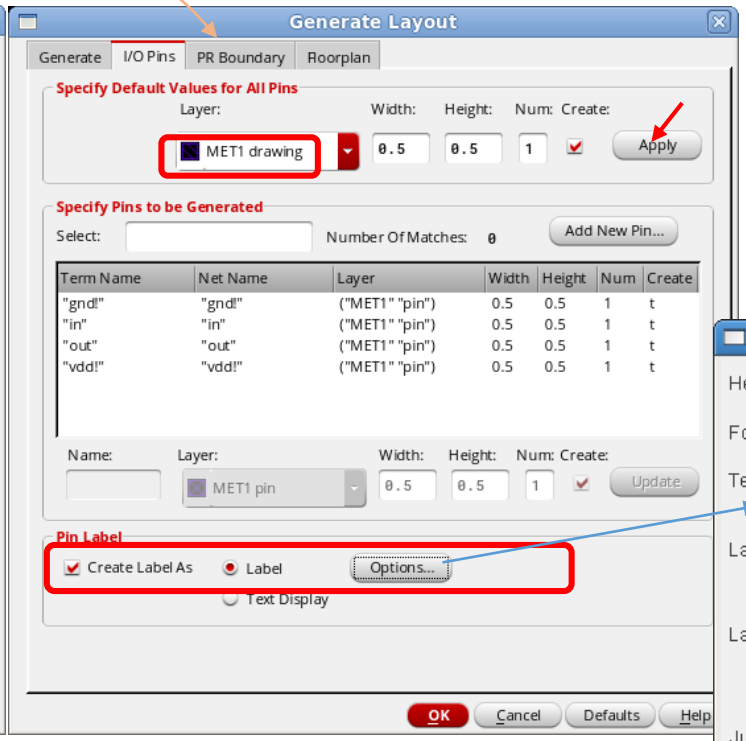
Fold the PMOS (2 gates)

In Schematic Editor: **Launch -> Layout XL**
In Layout XL: **Connectivity -> Generate ->All From Source**







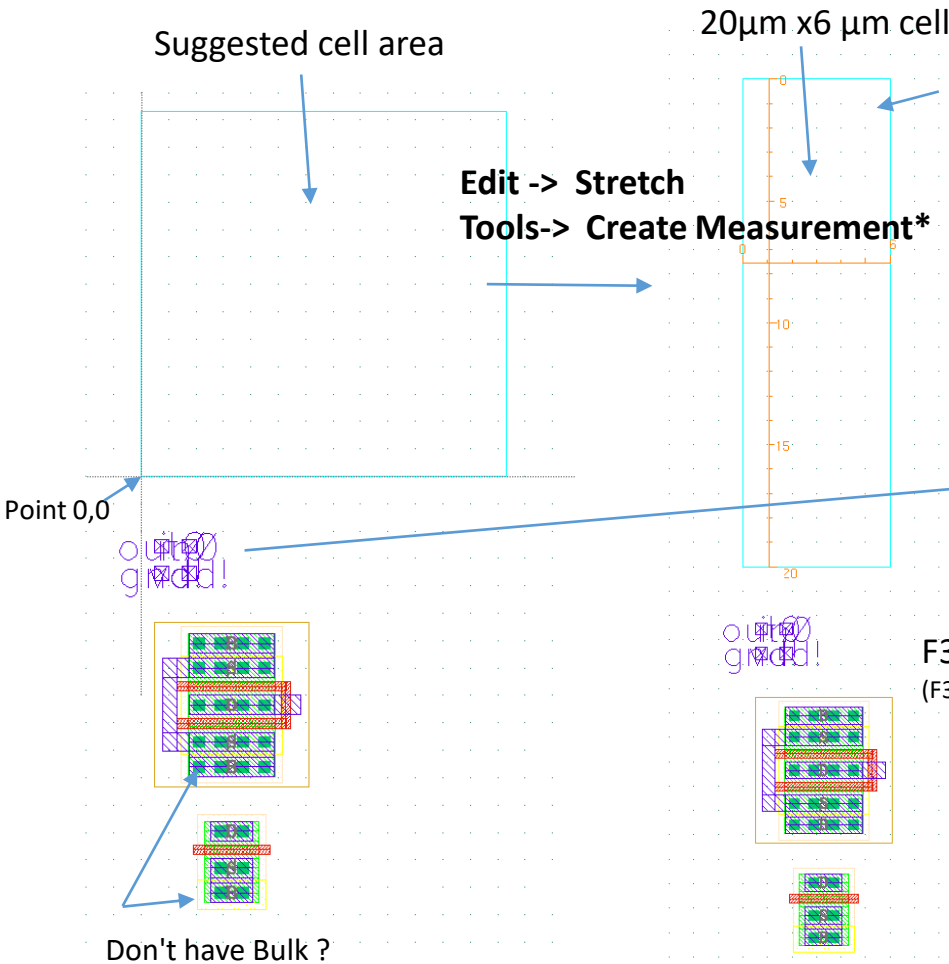


Text is used to recognize ports correctly.

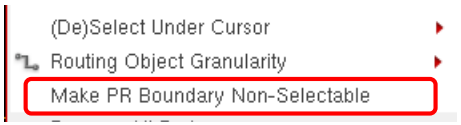
Generates a layout with all instances placed outside a rectangle (estimated cell boundary)

Layout Floorplaning

To see all layers: Options -> Display -> Display Levels -> Set "stop" to 32 (Shift-f) Save to ~/.cdsenv



RM ->



Tools -> Clear All Measurements*m
Create -> Shape -> Rectangle

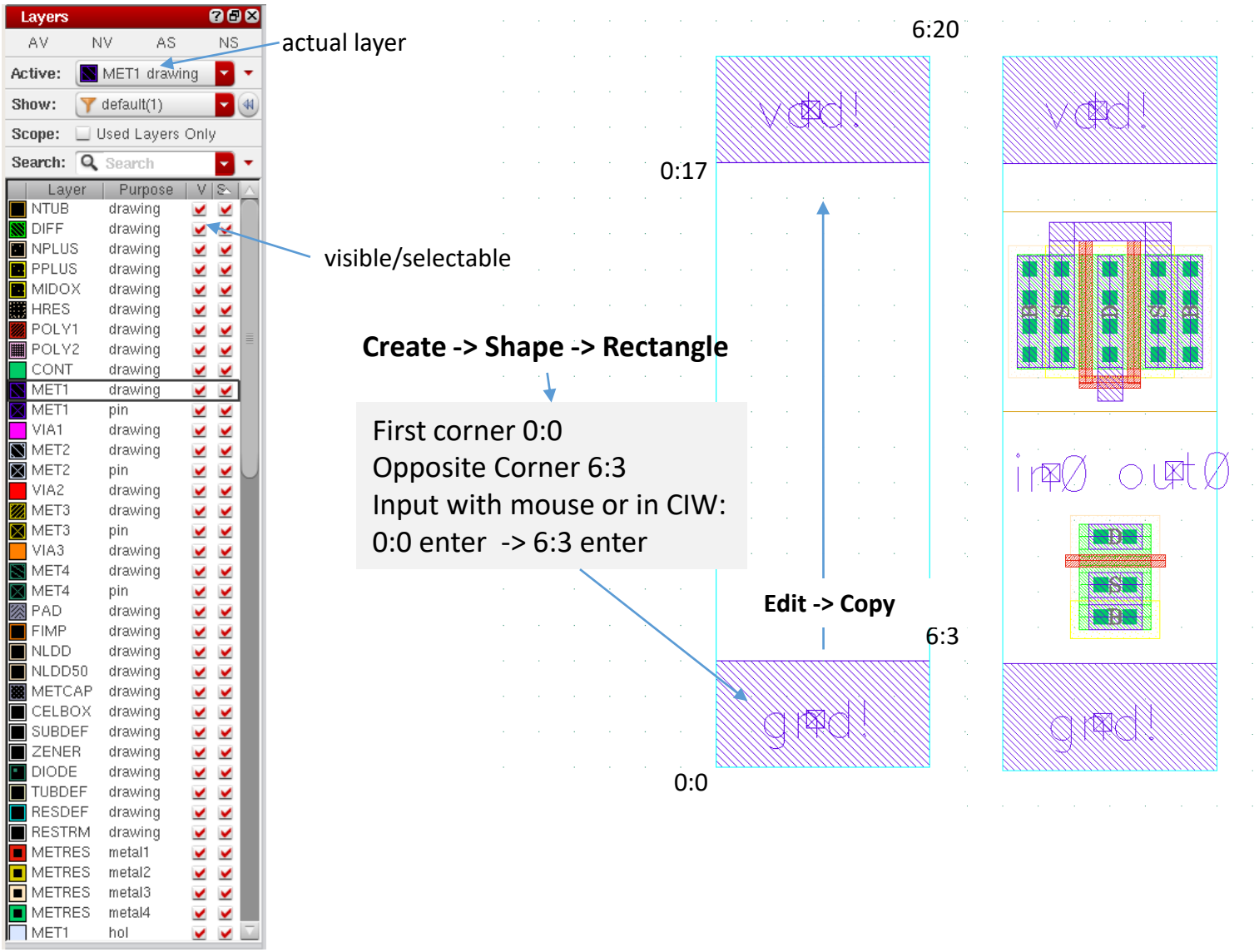
When moving pins include all parts.
Best practice: Snap to the little "+"!

F3 opens move options (e.g. orthogonal, all angels etc.)
(F3 opens options for all commands)

***Ruler** in older versions

Don't have Bulk ?
Delete both transistors in layout.
Open schematic and change transistor property there (add substrate contact).
In Layout XL use Connectivity -> Update Components and Nets.

Layout Edit


Layers
AV
NV
AS
NS
Active:
MET1 drawing
Show:
default(1)
Scope:
Used Layers Only
Search:
Search
Layer
Purpose
V
S
NTUB drawing
DIFF drawing
NPLUS drawing
PPLUS drawing
MIDOX drawing
HRES drawing
POLY1 drawing
POLY2 drawing
CONT drawing
MET1 drawing
MET1 pin
VIA1 drawing
MET2 drawing
MET2 pin
VIA2 drawing
MET3 drawing
MET3 pin
VIA3 drawing
MET4 drawing
MET4 pin
PAD drawing
FIMP drawing
NLDD drawing
NLDD50 drawing
METCAP drawing
CELBOX drawing
SUBDEF drawing
ZENER drawing
DIODE drawing
TUBDEF drawing
RESDEF drawing
RESTRM drawing
METRES metal1
METRES metal2
METRES metal3
METRES metal4
MET1 hol
actual layer
visible/selectable
Create -> Shape -> Rectangle
First corner 0:0
Opposite Corner 6:3
Input with mouse or in CIW:
0:0 enter -> 6:3 enter
Edit -> Copy
6:20
0:17
6:3
0:0
vdd!
gnd!
in
out
vdd!
gnd!

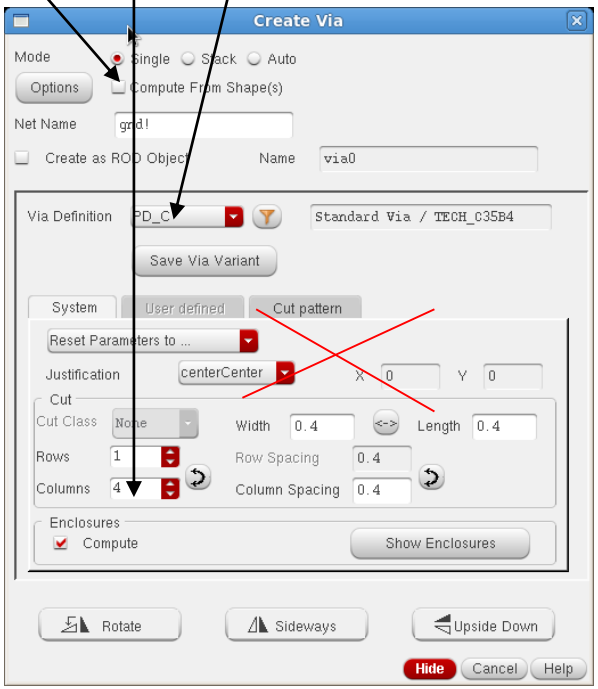
Layout - VIAs

Creating VIAs:

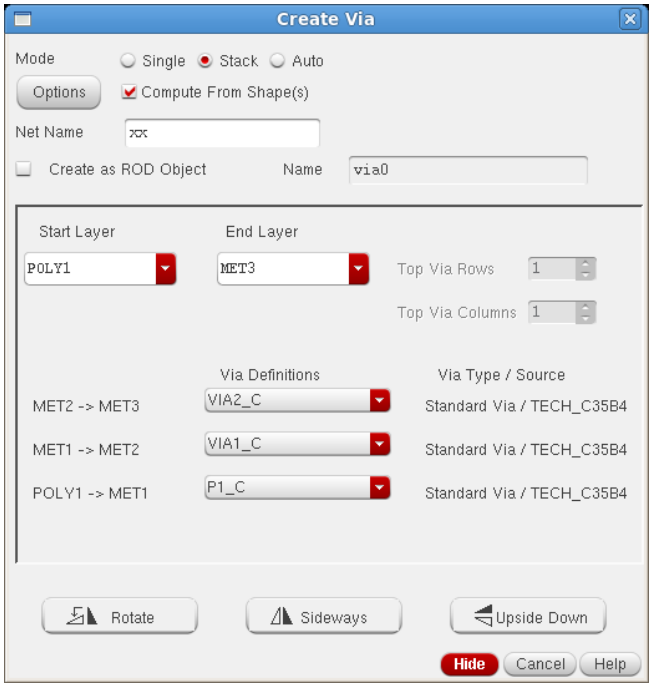
PD_C : p-Substrat-Metal1
ND_C : n-Well-Metal1
P1_C : Poly1-Metal1
P2_C : Poly2-Metal1
VIA1_C : Metal1-Metal2
VIA2_C : Metal2-Metal3
VIA3_C : Metal3-Metal4

Make them for the power stripes before routing of wires.

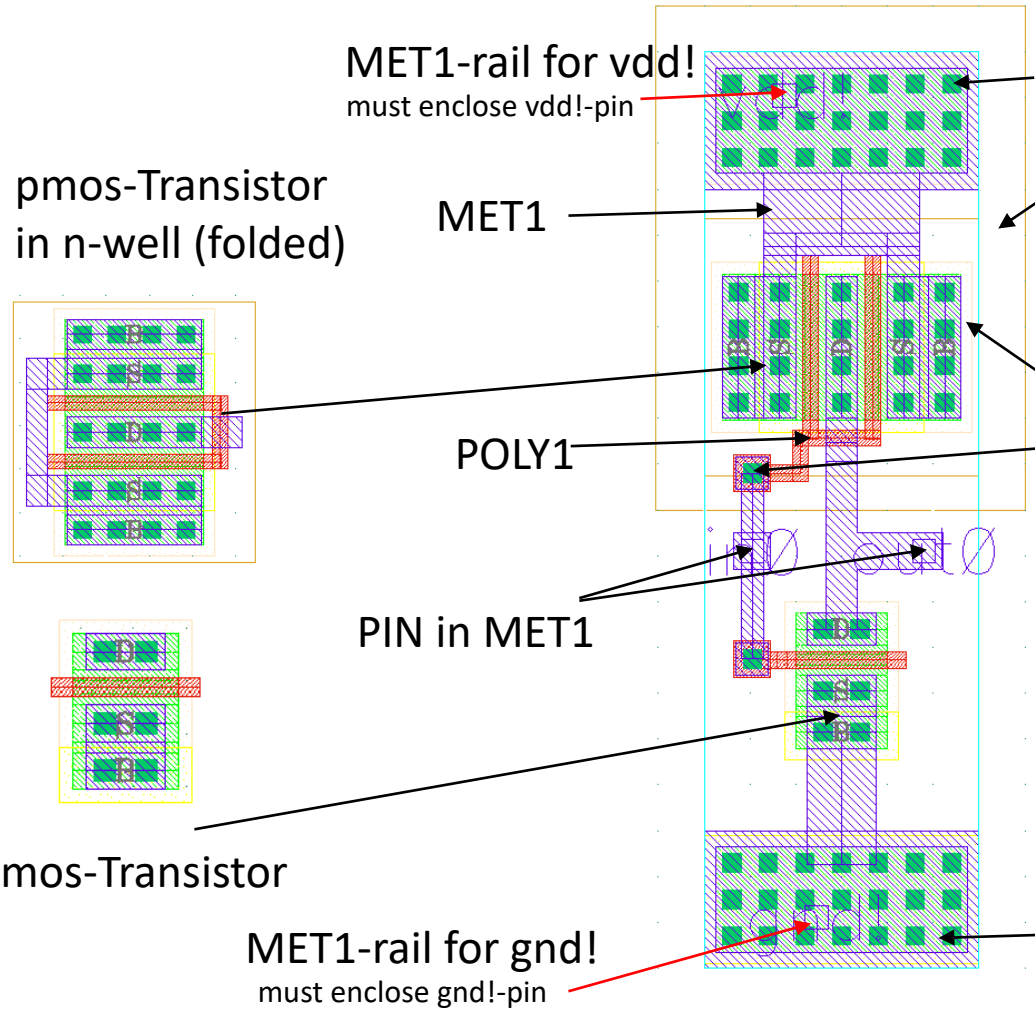
Layout of single contact predefined. Do not change!
Number and alignment variable. Using "**Compute from Shape(s)**" fills area with appropriate number of contacts.



Stacked VIAs connecting more than two layers available:



Cell Layout



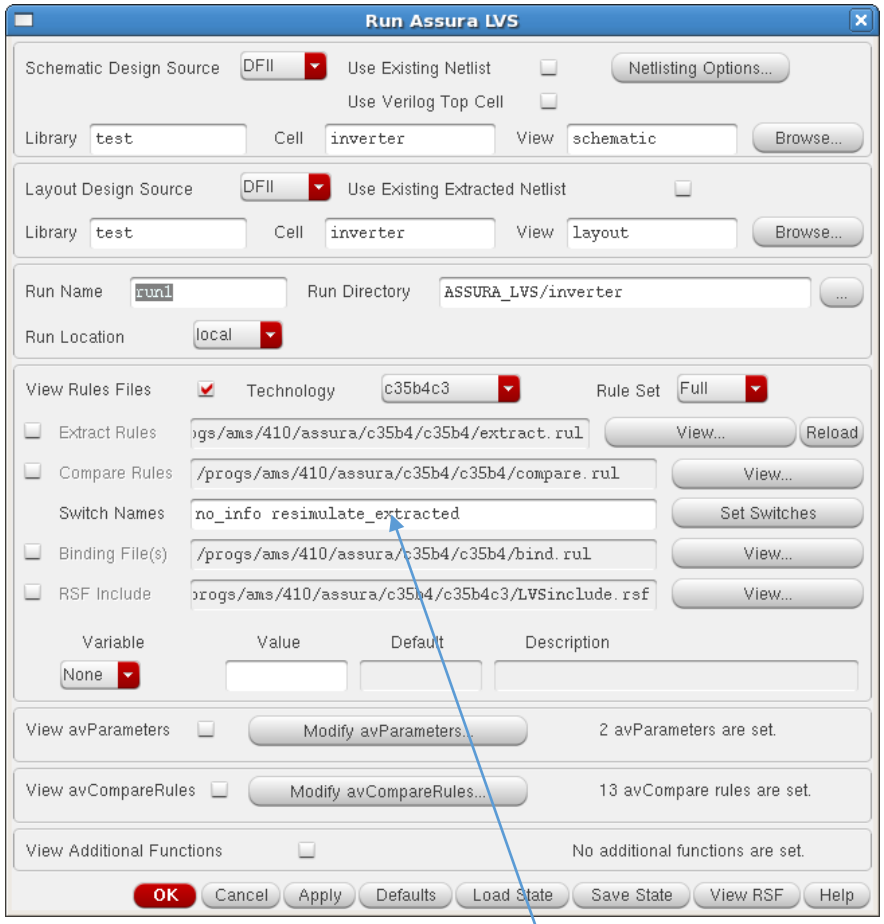
To consider (design rules):
Poly1: width ≥ 0.35µ, space ≥ 0.45µ
Metal1: width ≥ 0.5µ, space ≥ 0.45µ
Metal2: width ≥ 0.6µ, space ≥ 0.5µ

gnd! -> Exclamation mark: global signal

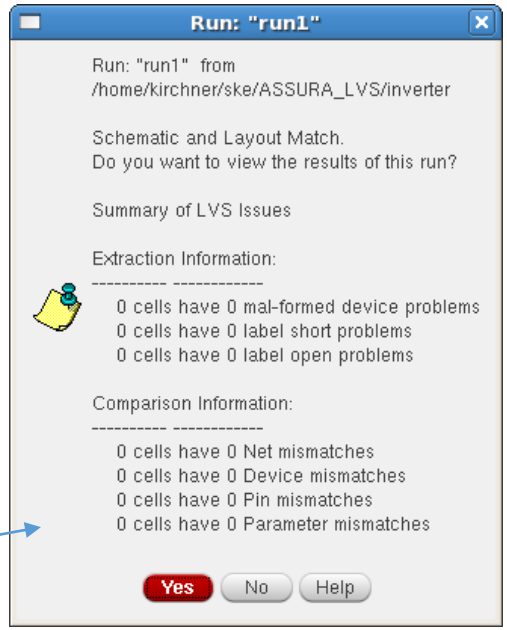
Cadence Layout - LVS

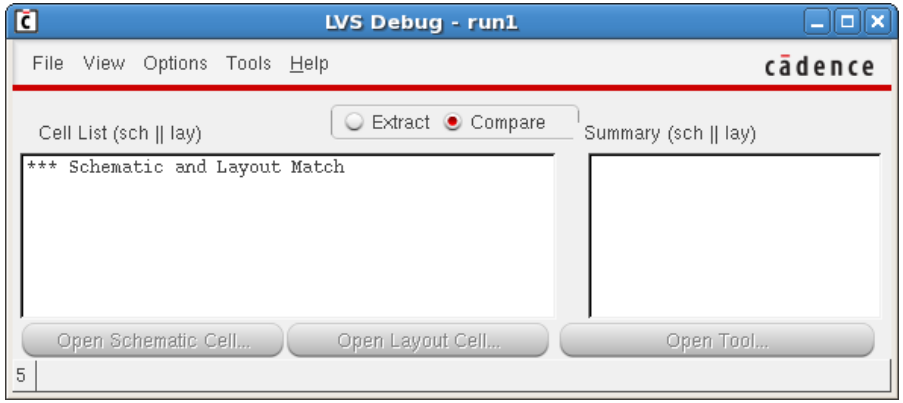
Compare Layout Versus Schematic

Assura -> Run LVS



wait!



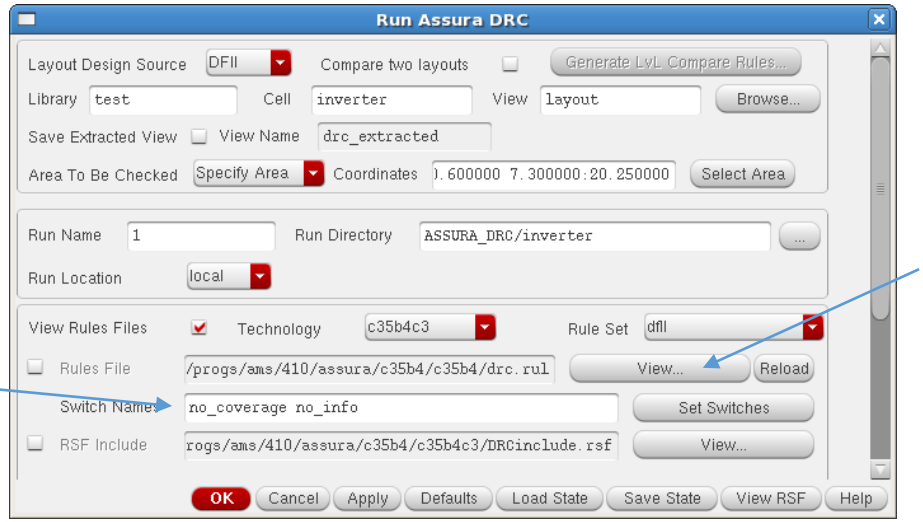


That's what we want to see!

Necessary for QRC parasitic extraction

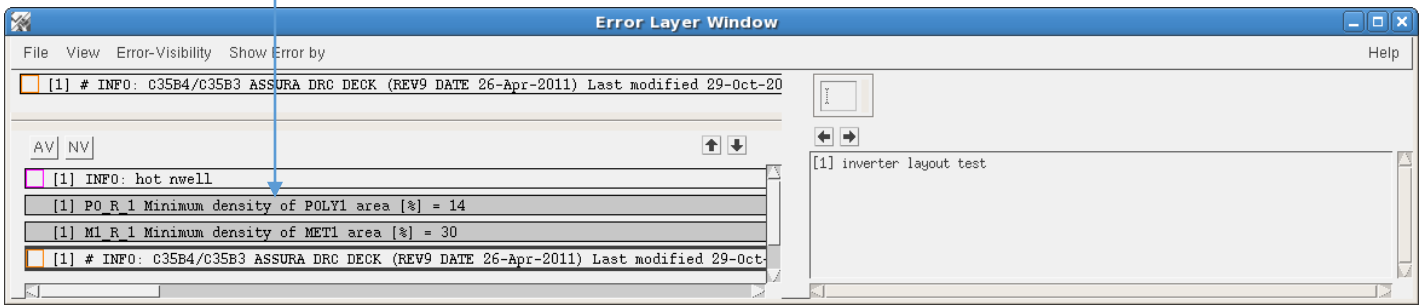
Cadence Layout - DRC

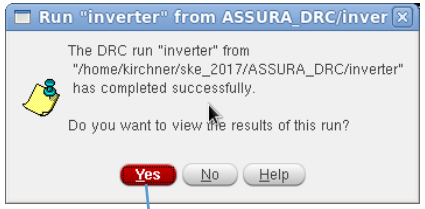
Assura -> Run DRC

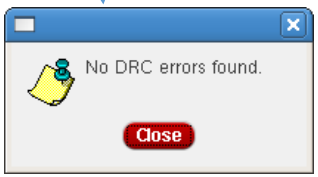


Set these switches to avoid some messages (see below!). What does "Coverage" mean?

Here you may open the rule set file for information. Contains all the rules like distances, overlap, min. width et cetera.







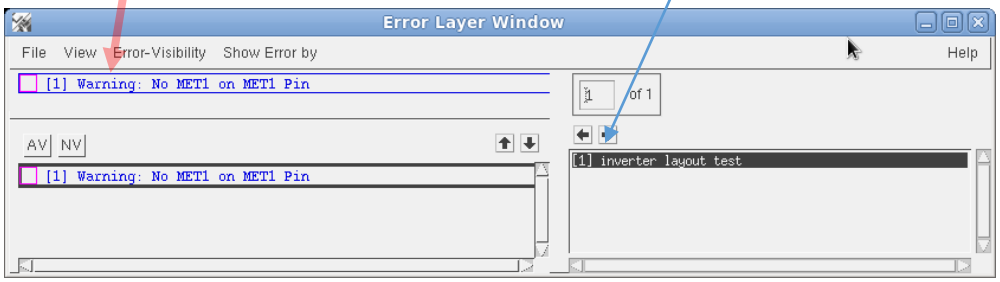
That's what we would like to see!

Cadence Layout – DRC with Errors remaining

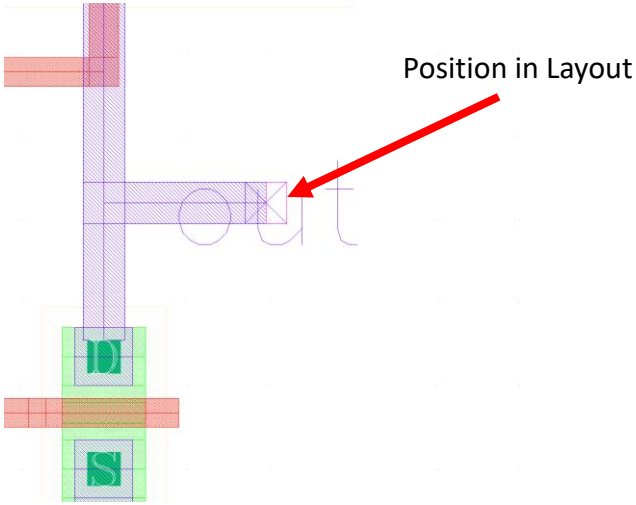
Example for an Error Message:
Here: Pin is not fully covered by metal

Violated Rule

Browse Errors (if multiple)

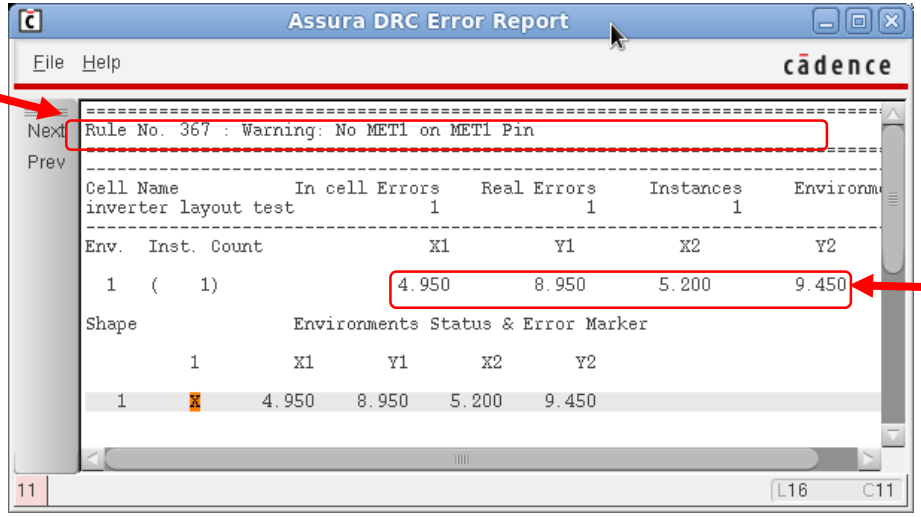


Position in Layout



View -> Error Report

Violated Rule

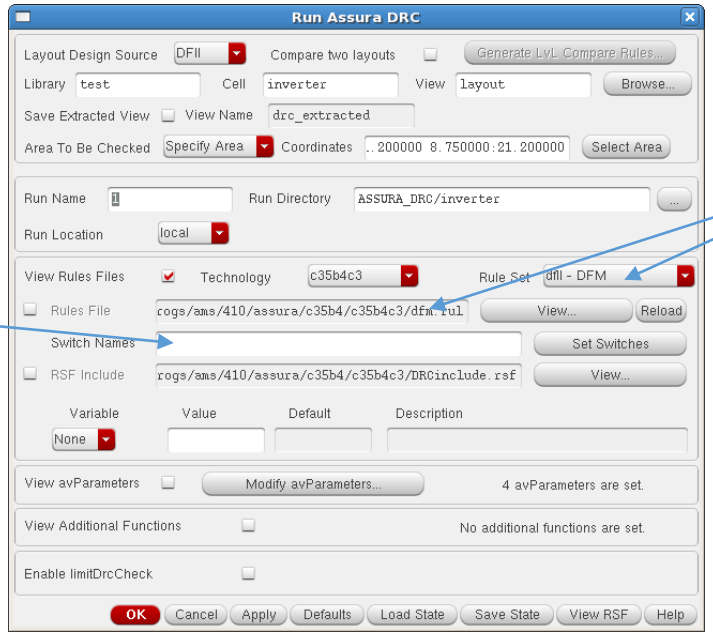


Position in Layout

Solutions:
Extend wire to the right or
add a rectangle in MET1 covering the Pin

Cadence Layout - DFM

Assura -> Run DRC

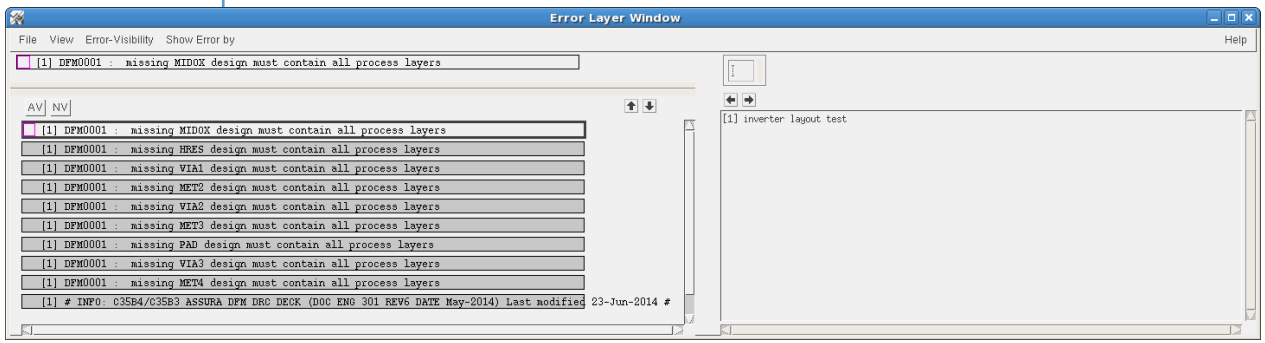


Extended ruleset:
Rules for manufacturing ->

Coverage of all but upper metal layer et cetera.

no switches!

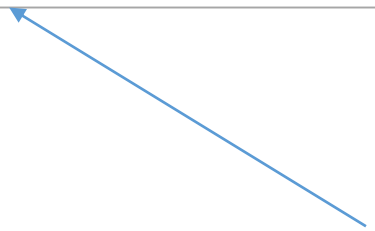
Errors because we did not use some layers.
Interesting for a top layout.



Cadence Layout - ERC

Electrical rule check is included in DRC.
There is no separate rule check in the ams-HITkit.

Starting ERC with Assura -> Run ERC opens a form similar to DRC with no technology selected and either rule files.



Up to now no verification for this.
Separate ERC-usage found nowhere.

Cadence Layout – QRC – Parametric Extraction

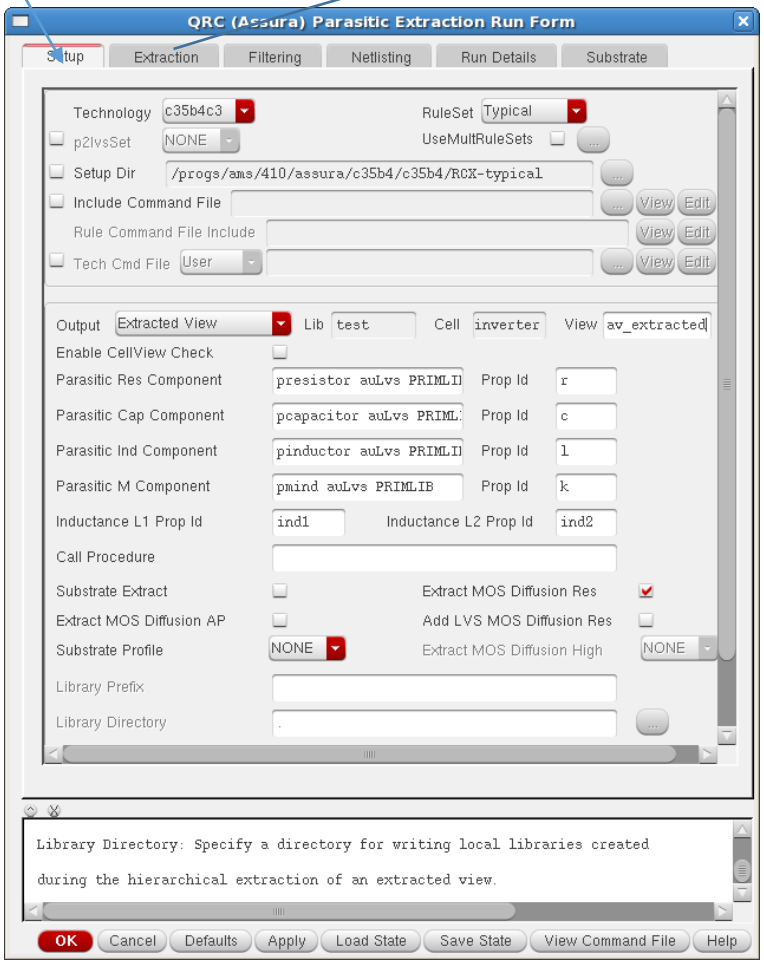
QRC -> Run Assura Quantus -QRC

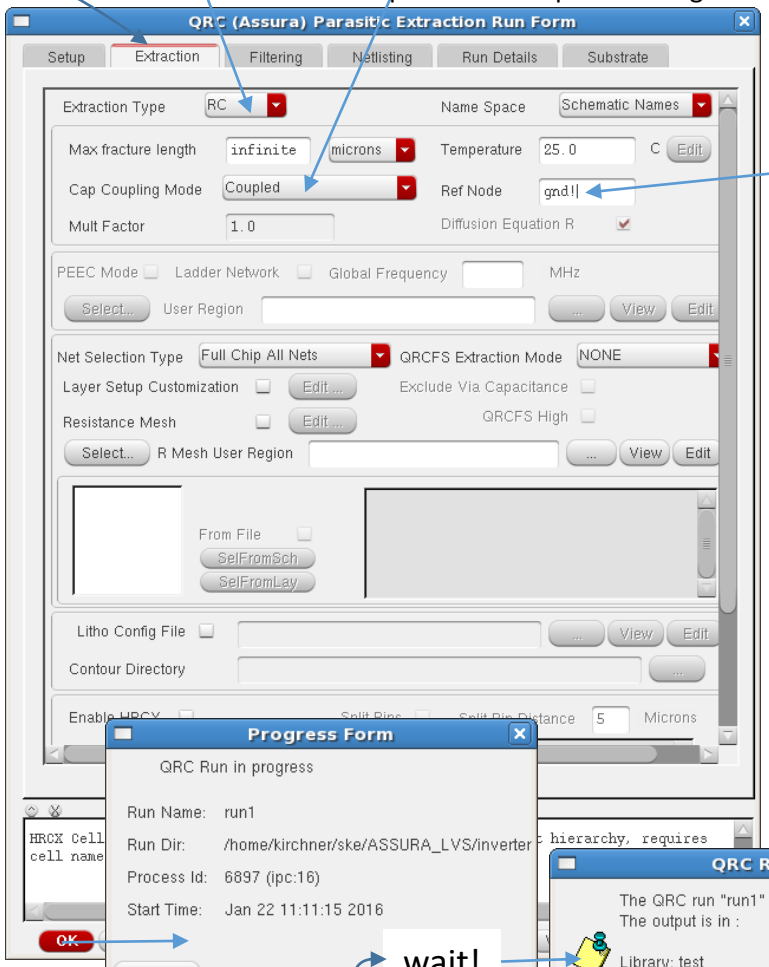
no changes

RC

Coupled C: net to net (signals)
Decoupled C: net to power and ground only

use gnd! or vcc!

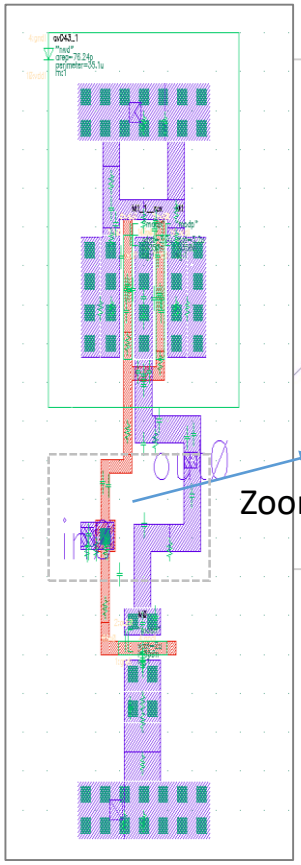




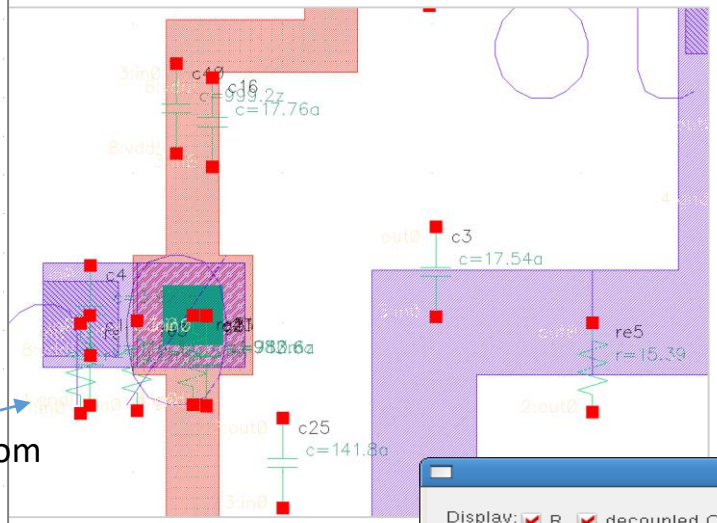
Cadence – QRC – Extracted view

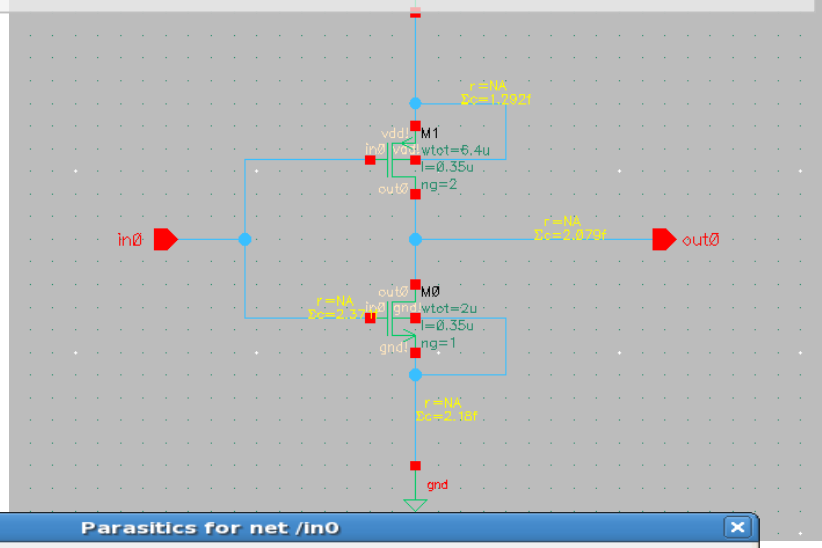
Open View "av_extracted" in Library Manager

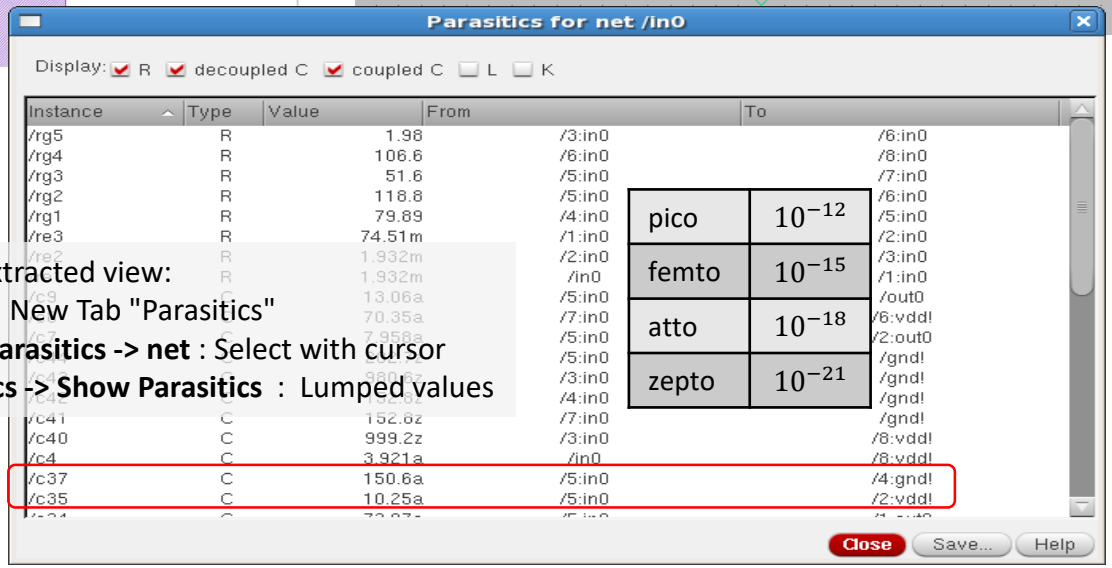
Launch -> Plugins ->Parasitics : New Tab "Parasitics"
Parasitics -> Setup Parasitics (gnd! and vdd! as reference nodes)



Zoom







pico	10^{-12}
femto	10^{-15}
atto	10^{-18}
zepto	10^{-21}

In Schematic or av_extracted view:
Launch -> Parasitics : New Tab "Parasitics"
Parasitics -> Report Parasitics -> net : Select with cursor
In Schematic **Parasitics -> Show Parasitics** : Lumped values

Try also: net to net
terminal to terminal (r)

Viewing parasitics may be interesting.
More important is their use in postlayout simulation.
They will be included in simulation netlists.

Cadence – QRC – Post-Layout Simulation (ADE-L/XL)

Open testbench (schematic)
Copy the inverter and its load.
Save as a new testbench.

We need different models for the UUT (inverter)

- Original schematic
- Netlist with extracted parasitics.

In **CIW**:

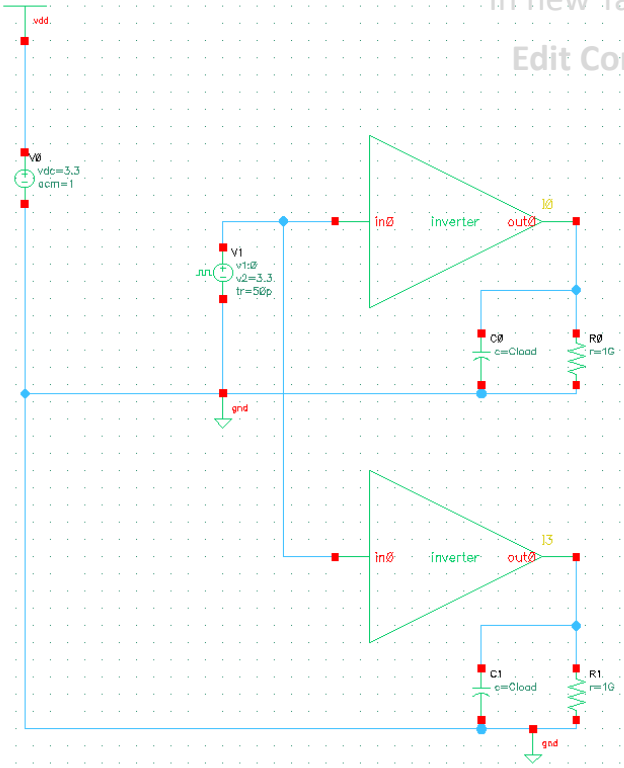
File -> New -> Cellview

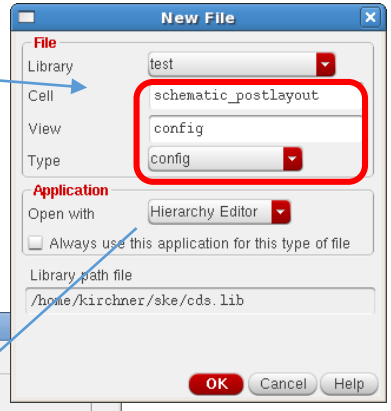
In Schematic Editor:

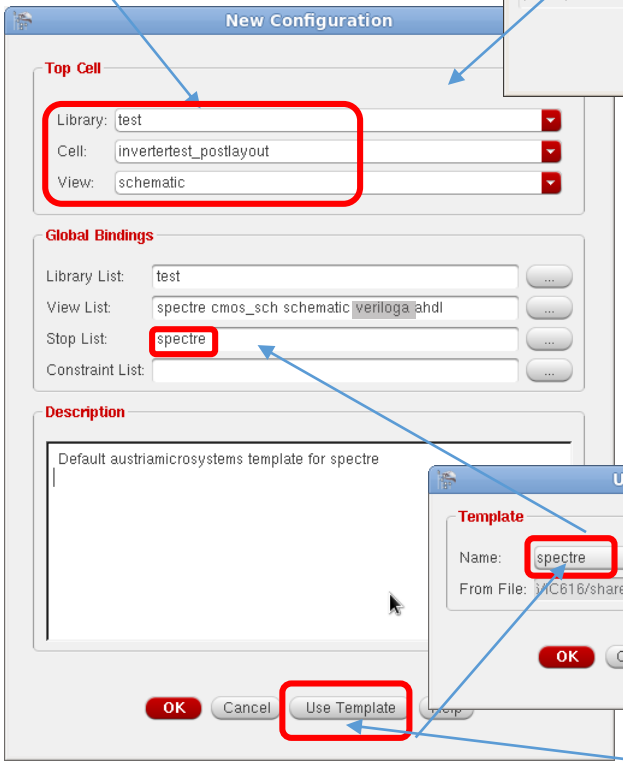
Launch -> Hierachy Editor

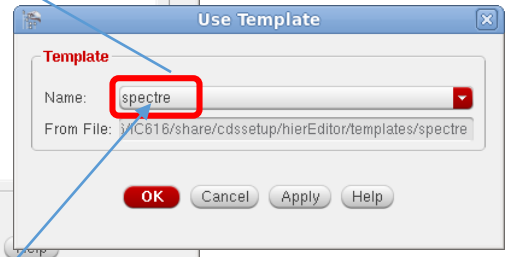
In new Tab "Hierarchy-Editor"

Edit Configuration



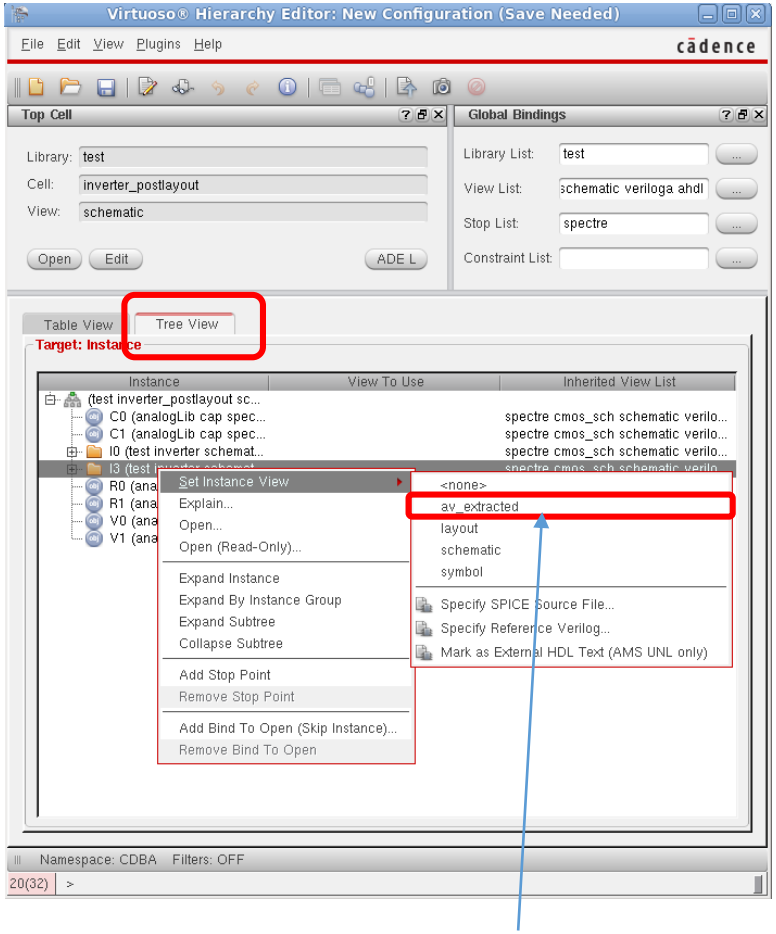


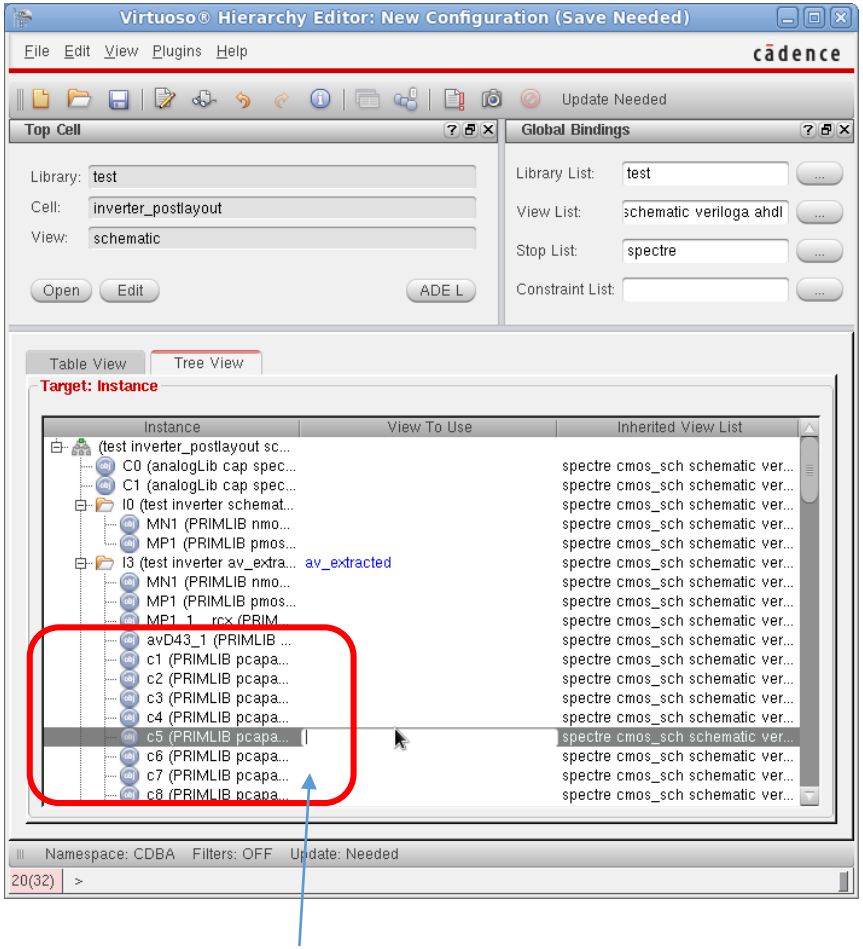




Begin here!

Cadence – Post-Layout Simulation (ADE-L/XL)



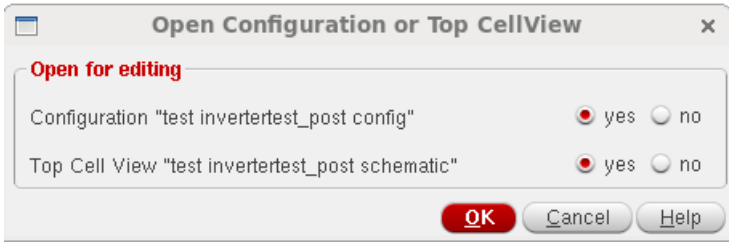


Parasitics

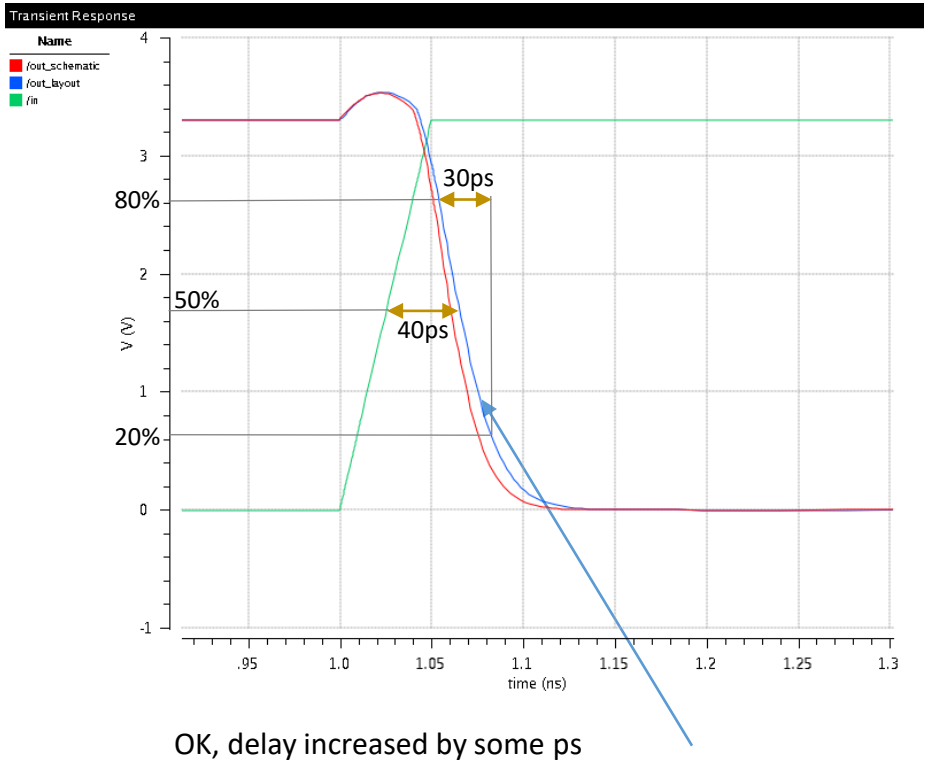
Replace (use RightMouse -> set instance view) schematic by av_extracted

Cadence – Post-Layout Simulation - Result

Open the configuration in Library Manager

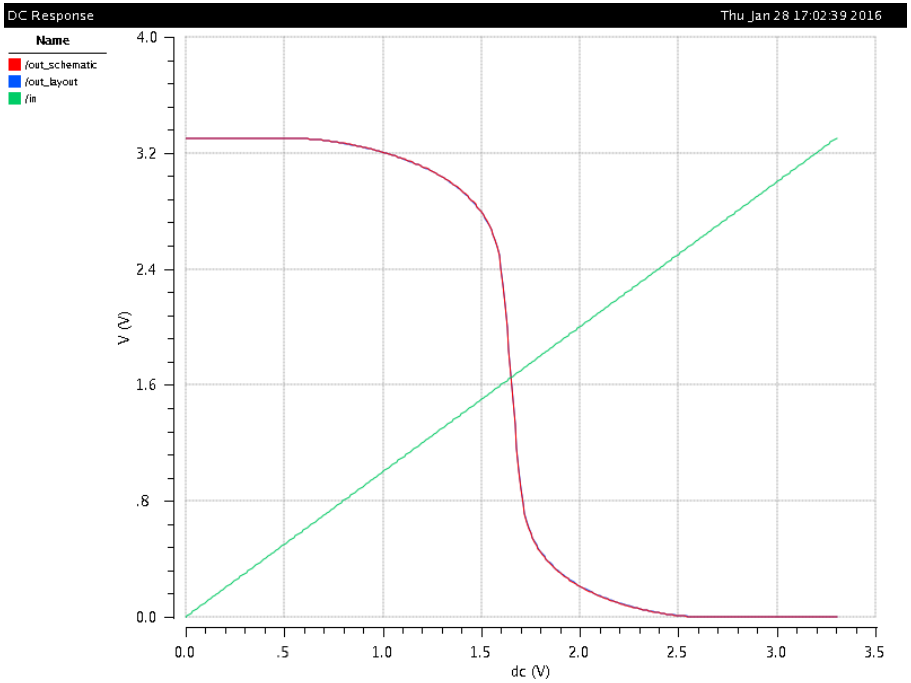


To perform simulation see slides above from "Simulation ADE GXL Start"



OK, delay increased by some ps

Shown for C_{Load}= 4 fF. Less difference for higher load.



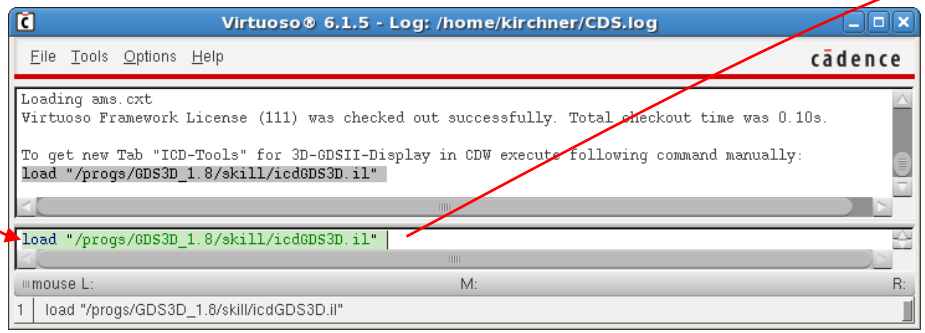
OK, no visible change

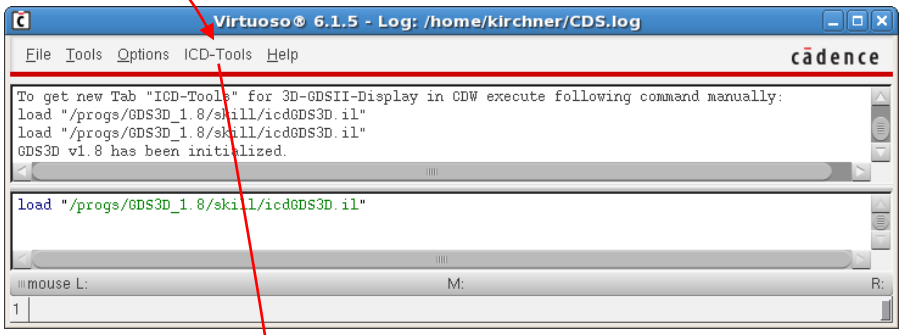
Layout 3D View

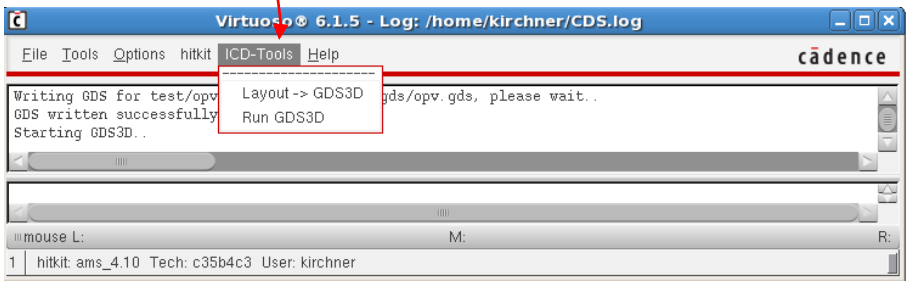
GDS3D from University of Twente, NL

Needs a technology file (layer thickness, pitches). Generated for AMSC35B4 from process parameters.
Needs initialization for Cadence integration, but may be used standalone.

Automatic initialization does not work yet. For manual initialization observe the last output after CIW start.







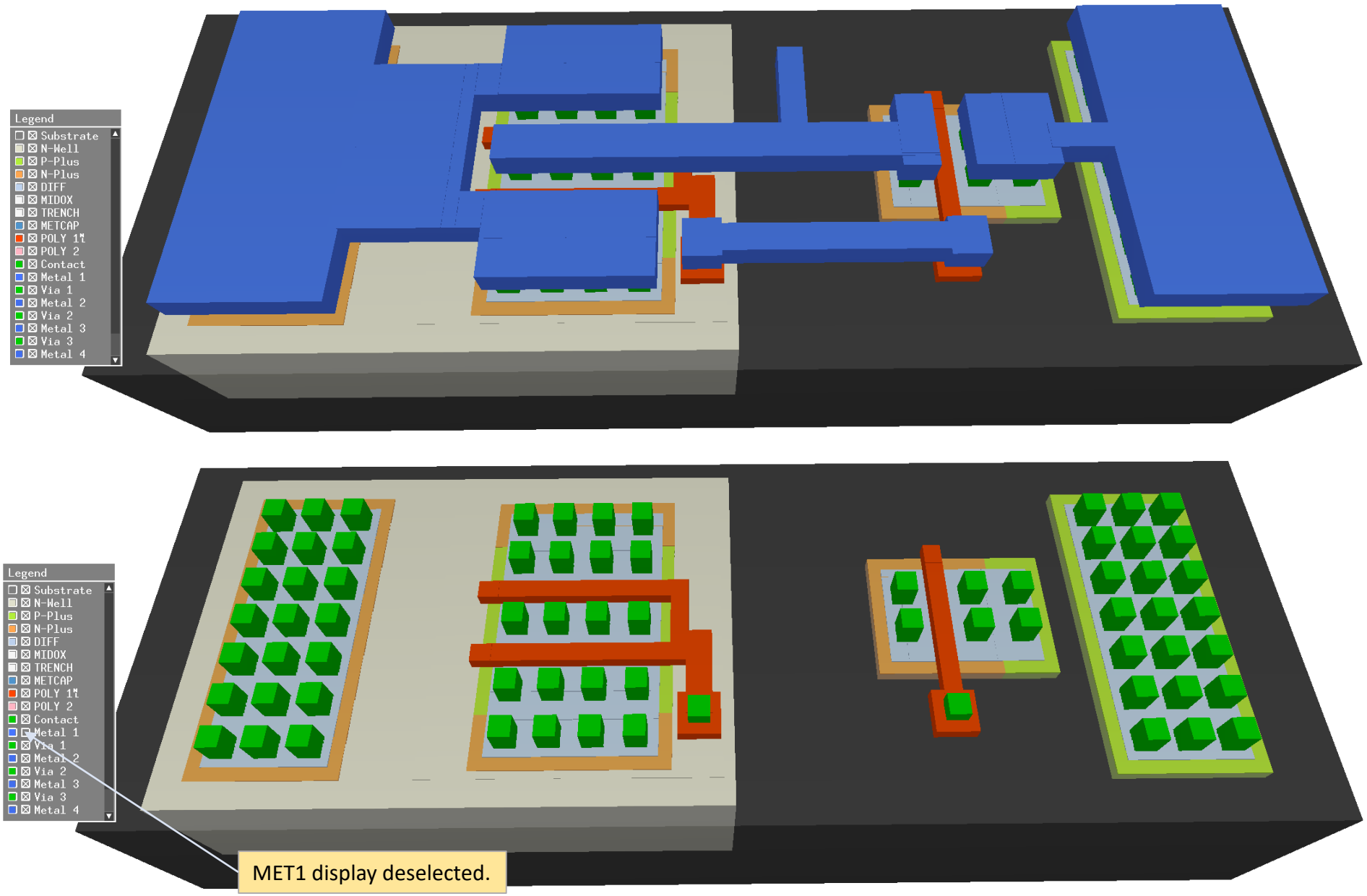
With a layout opened we can make a GDSII-Stream and run the GDS3D tool. ICD - Tools

In the GDS3D-tool use F1 to see the (game like) usage.

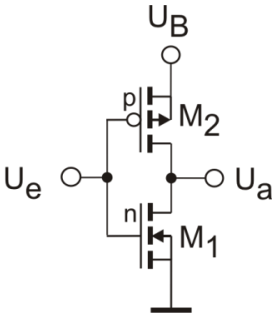
Do not use the normal streamout from CDW (File -> Export -> Stream) because GDS3D uses a separate directory for the gds-File!

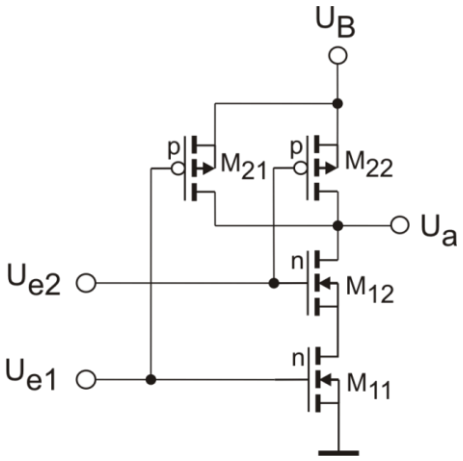
ICD is simply **I**ntegrated **C**ircuit **D**esign group at Twente University)

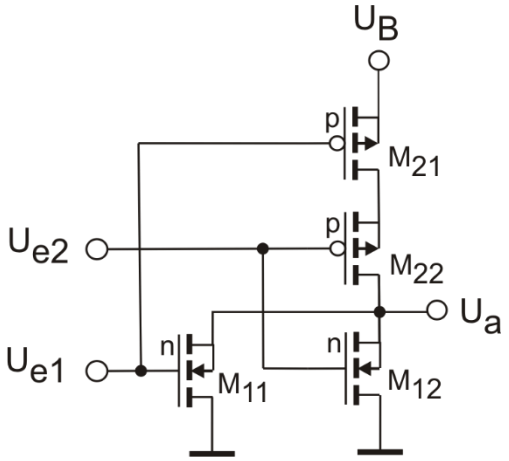
Layout 3D View



Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
Inverter, 2-Input-NAND, 2-Input-NOR







$U_B = 3{,}3V$
$U_{GS0n} = 0{,}48\text{V}$
$U_{SG0p} = 0{,}67V$
$KP_n = 170\ \frac{\mu A}{V^2}$
$KP_p = 58\ \frac{\mu A}{V^2}$

$(d_{ox} = 7{,}6\ nm)$

Calculate the geometry in ($^W/_L$-ratio for p- und n-Transistors) so that you get a good compromise for the switching point and noise margin for the cases:

- Both inputs change at the same moment (connected)
- One input is preassigned to a fixed value so that the second one causes output change. (May be different for both inputs!)

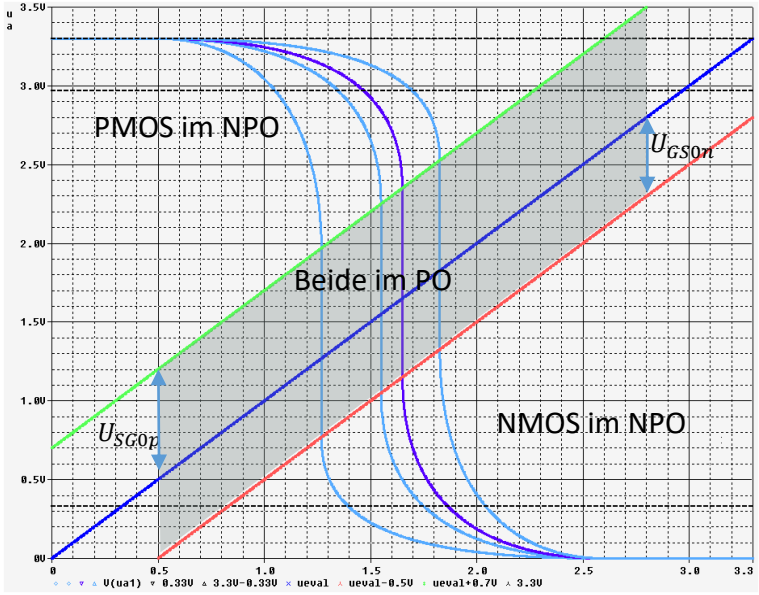
Switching point should be near $\frac{U_B}{2}$ for all cases.

Design (schematic, layout) a 2-Input-NAND or a 2-Input-NOR using short channel length transistors (0.35µ) or long channel length transistors (3.5µm]. Selection of the specific design is done with the tutor.

Cell hight shall be 20 µm.

From Simulation (including postlayout) find out the following values:
Switching points and noise margin for the different cases at the two inputs.
Delay times (50%), falltime, risetime (20%-80%) dependend on load capacitance (4.. 100 fF) and temperature (-40 to 80°C).

Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
Inverter, 2-Input-NAND, 2-Input-NOR



At the switching point both transistor-pairs are in the pinch-off state and passed by the same current :

$$\frac{\beta_n}{2}(U_{eS} - U_{GS0n})^2 = \frac{\beta_p}{2}\left(U_B - U_{eS} - U_{SG0p}\right)^2$$

But: There is a difference in the number of involved switching transistors for the different input cases!

Common Equation for CMOS-Inverter:

$$\frac{\beta_n}{2}(U_{eS} - U_{GS0n})^2 = \frac{\beta_p}{2}\left(U_B - U_{eS} - U_{SG0p}\right)^2$$

Dissolve for U_{eS}:

$$\sqrt{\beta_n}(U_{eS} - U_{GS0n}) = \sqrt{\beta_p}\left(U_B - U_{eS} - U_{SG0p}\right)$$

$$U_{eS} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot U_{GS0n} + U_B - U_{SG0p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Für $U_{eS} = \frac{U_B}{2}$

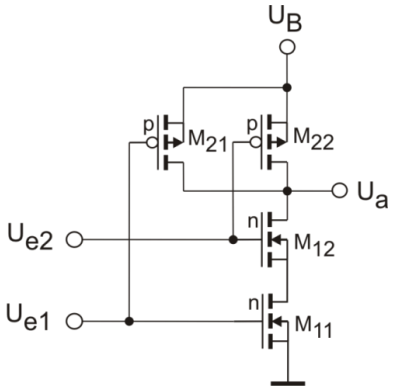
$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}}\right)^2$$

$$\beta = KP \cdot \frac{W}{L}$$

$$mit: \; KPN = 3 \cdot \mathrm{KPP}$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}}\right)^2$$

NAND-Gate



For $U_{eS} = \frac{U_B}{2}$ when both inputs change:

$$\frac{\beta_{nges}}{\beta_{pges}} = \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}}\right)^2$$

$\beta_{nges} = KPN \cdot \frac{1}{2}\left[\frac{W}{L}\right]_n$ One transistor of double length

$\beta_{pges} = KPP \cdot 2\left[\frac{W}{L}\right]_p$ One transistor of double width

$KPN = 3 \cdot \mathrm{KPP}$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{4}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}}\right)^2$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{4}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}}\right)^2 = \frac{4}{3}\left(\frac{1{,}65 - 0{,}7}{1{,}65 - 0{,}5}\right)^2 = 0{,}908$$

$$\frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 1{,}1$$

Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
Inverter, 2-Input-NAND, 2-Input-NOR

$$\frac{\beta_n}{2}(U_{eS} - U_{GS0n})^2 = \frac{\beta_p}{2}(U_B - U_{eS} - U_{SG0p})^2$$

$$\sqrt{\beta_n}(U_{eS} - U_{GS0n}) = \sqrt{\beta_p}(U_B - U_{eS} - U_{SG0p})$$

One p-transistor is and remains off.
One n-Transistor is and remains on.
Only an inverter is switching.

Lower transistor in NAND during switching phase:

$$U_{eS} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot (U_{GS0n} + U_{DS11}) + U_B - U_{SG0p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

See if the values are acceptable with regard to noise margin.
Try to change W/L ratios to find a compromise.

Für $U_{eS} = \frac{U_B}{2}$

$$\beta_{nges} = KPN \cdot \frac{W}{L}$$

$$\beta_{pges} = KPN \cdot \frac{W}{L}$$

$$KPN = 3 \cdot \text{KPP}$$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n} - U_{DS11}}\right)^2$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n} - U_{DS11}}\right)^2$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1{,}65 - 0{,}7}{1{,}65 - 0{,}5 - 0{,}236V}\right)^2 = 0.36 \qquad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 2{,}78$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1{,}65 - 0{,}7}{1{,}65 - 0{,}5}\right)^2 = 0{,}23 \qquad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 4{,}44$$

Interesting, but we can implement one geometry only and must configure a compromise.

Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
Inverter, 2-Input-NAND, 2-Input-NOR

Practical hint to safe time:

Starting from the Inverter schematic:

You may open the inverter schematic as the origin for the new design.

Then create a new schematic cellview (from CDW or Library Manager). **File -> New -> Cellview**

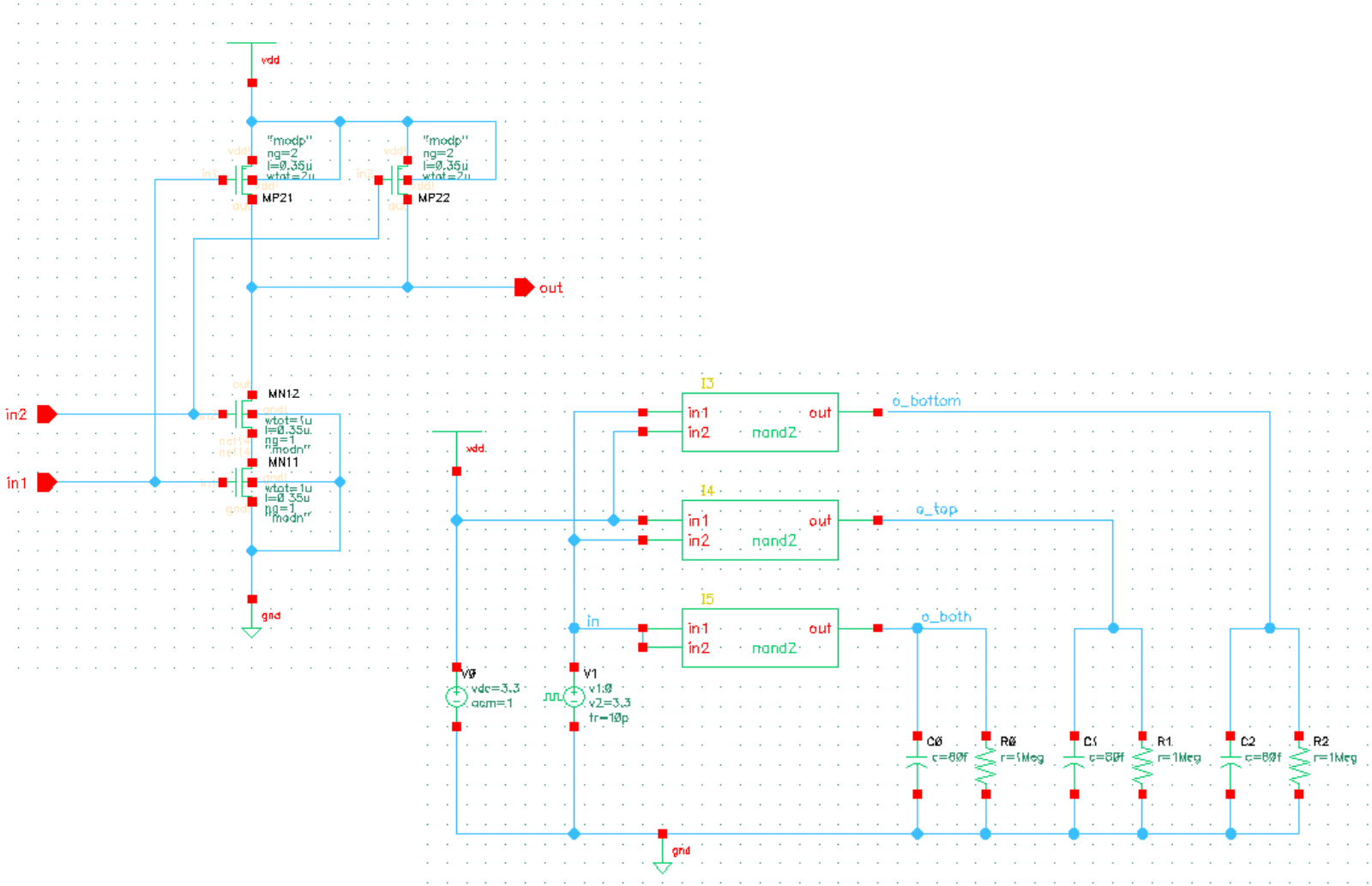
When you have the new empty schematic and the inverter schematic side by side you can copy the inverter circuit or parts of it to the new schematic.

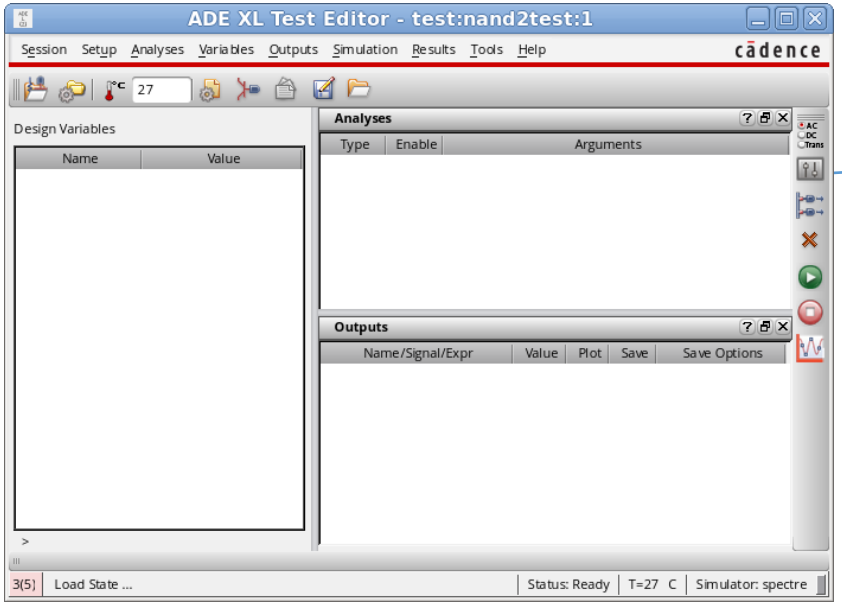
Use copy: "**c**" -> select the desired part using the left mouse button
-> click on the selected part
-> drag to the new place (may be the same schematic window or the new one)

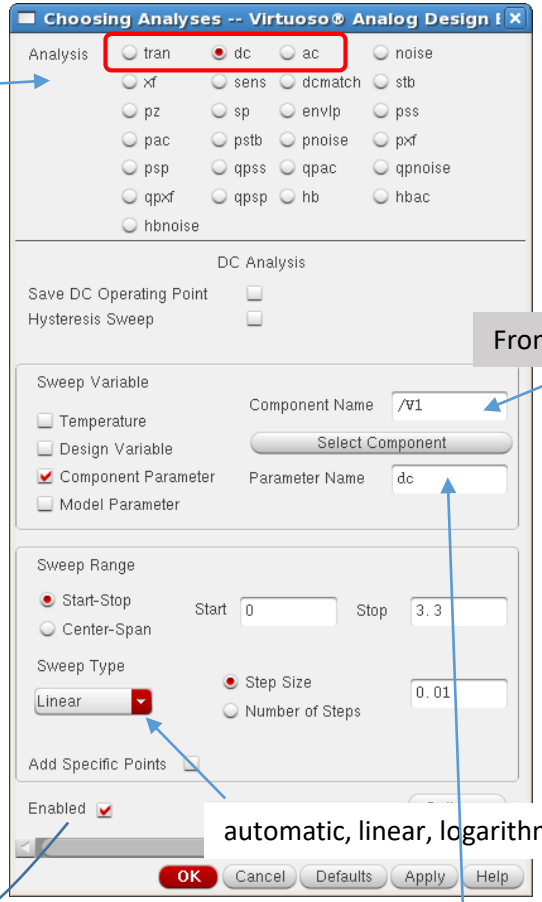
Edit the new schematic to build the NAND or NOR design.

You may proceed in the same manner for the testbench.

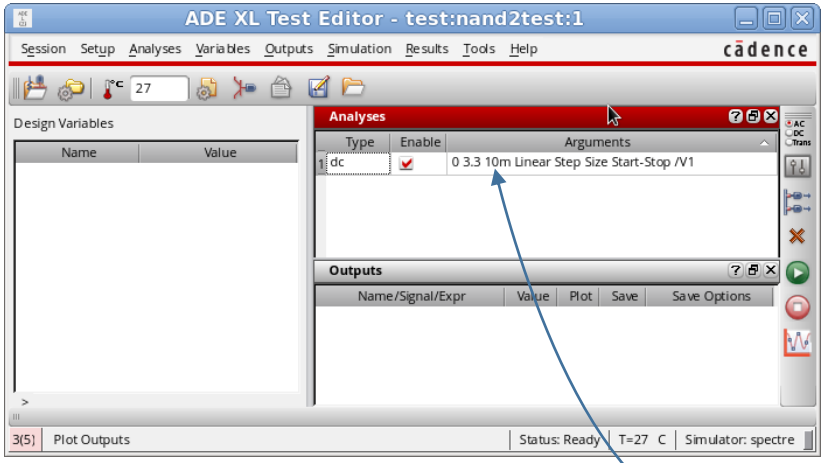
2-input-NAND


vdd
"modp"
ng=2
l=0.35u
wtot=2u
MP21
MP22
out
in2
in1
MN12
MN11
wtot=1u
l=0.35u
ng=1
"modn"
gnd
I3
I4
I5
in1
in2
nand2
o_bottom
o_top
o_both
in
V0
vdc=3.3
acm=1
V1
v1=0
v2=3.3
tr=10p
C0
R0
C1
R1
C2
R2
c=80f
r=1Meg



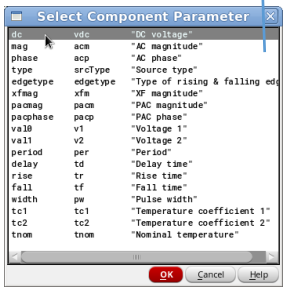


From Schematic

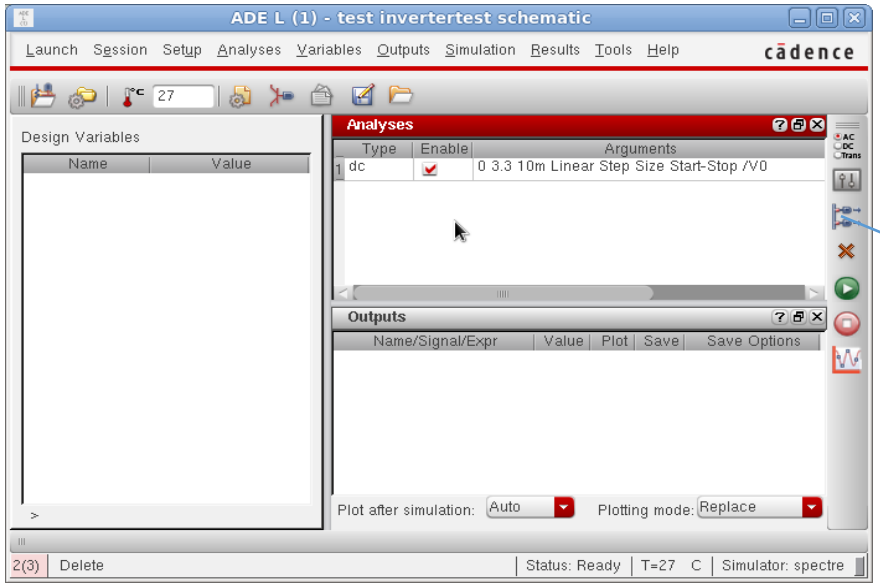


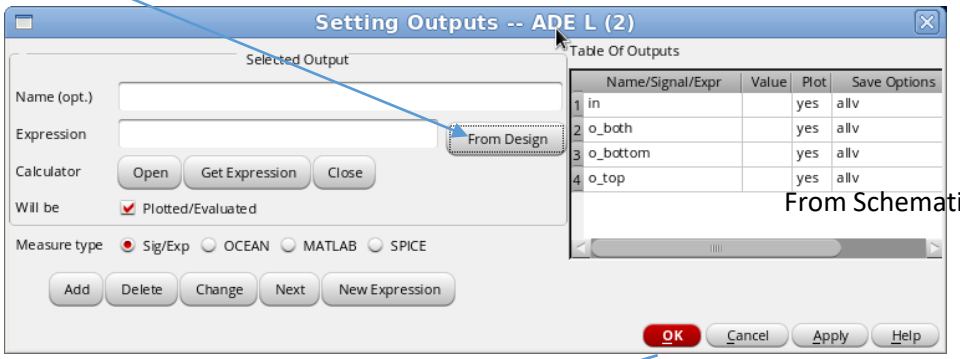
Create/Edit analyses
Design Variables
Simulation Outputs
Delete selected analyses
Run enabled analyses
Stop
Plot

automatic, linear, logarithmic

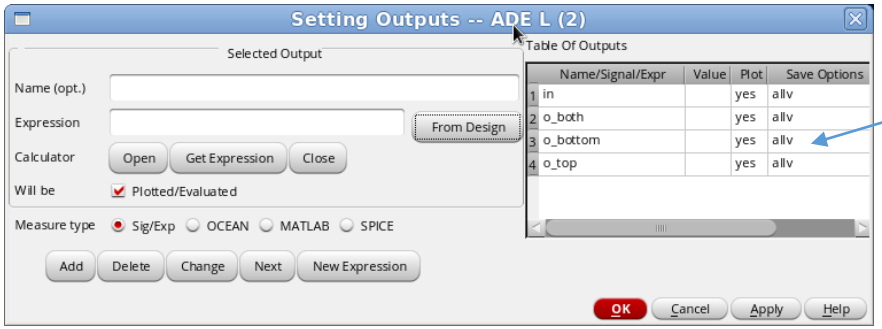


Intranet

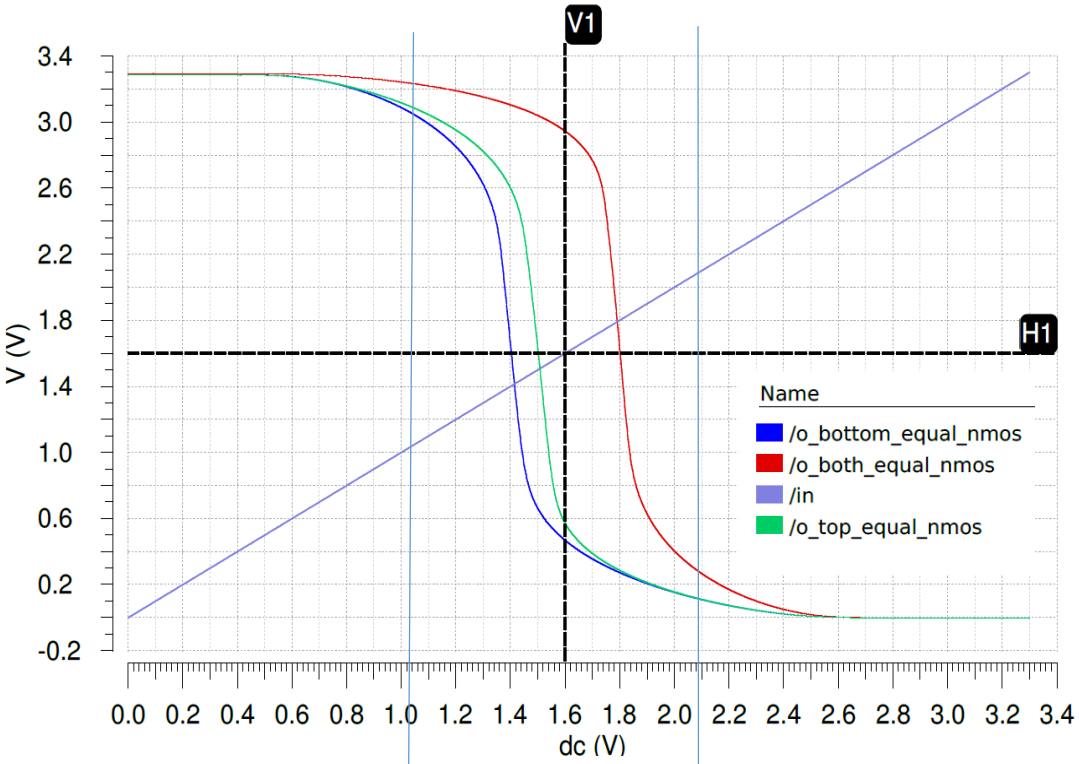




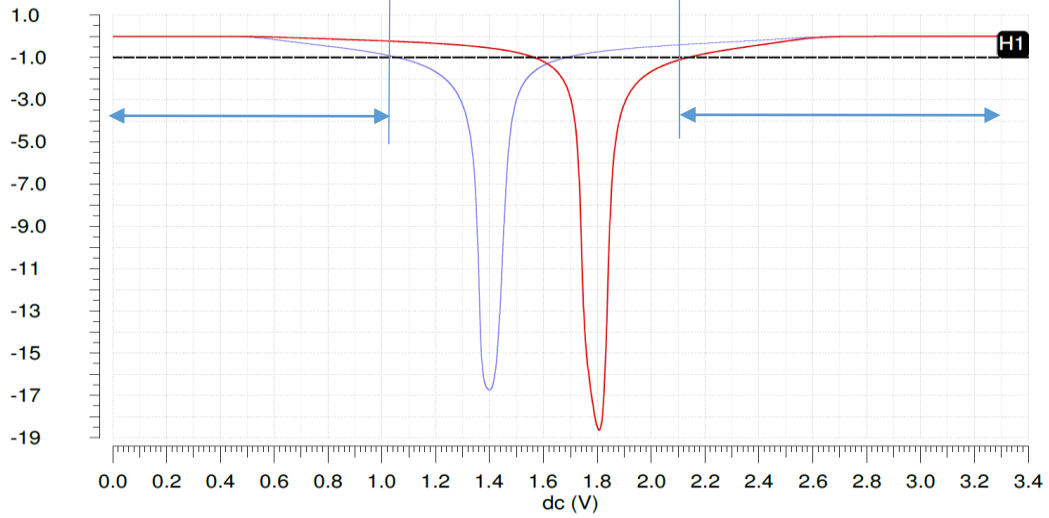
From Schematic



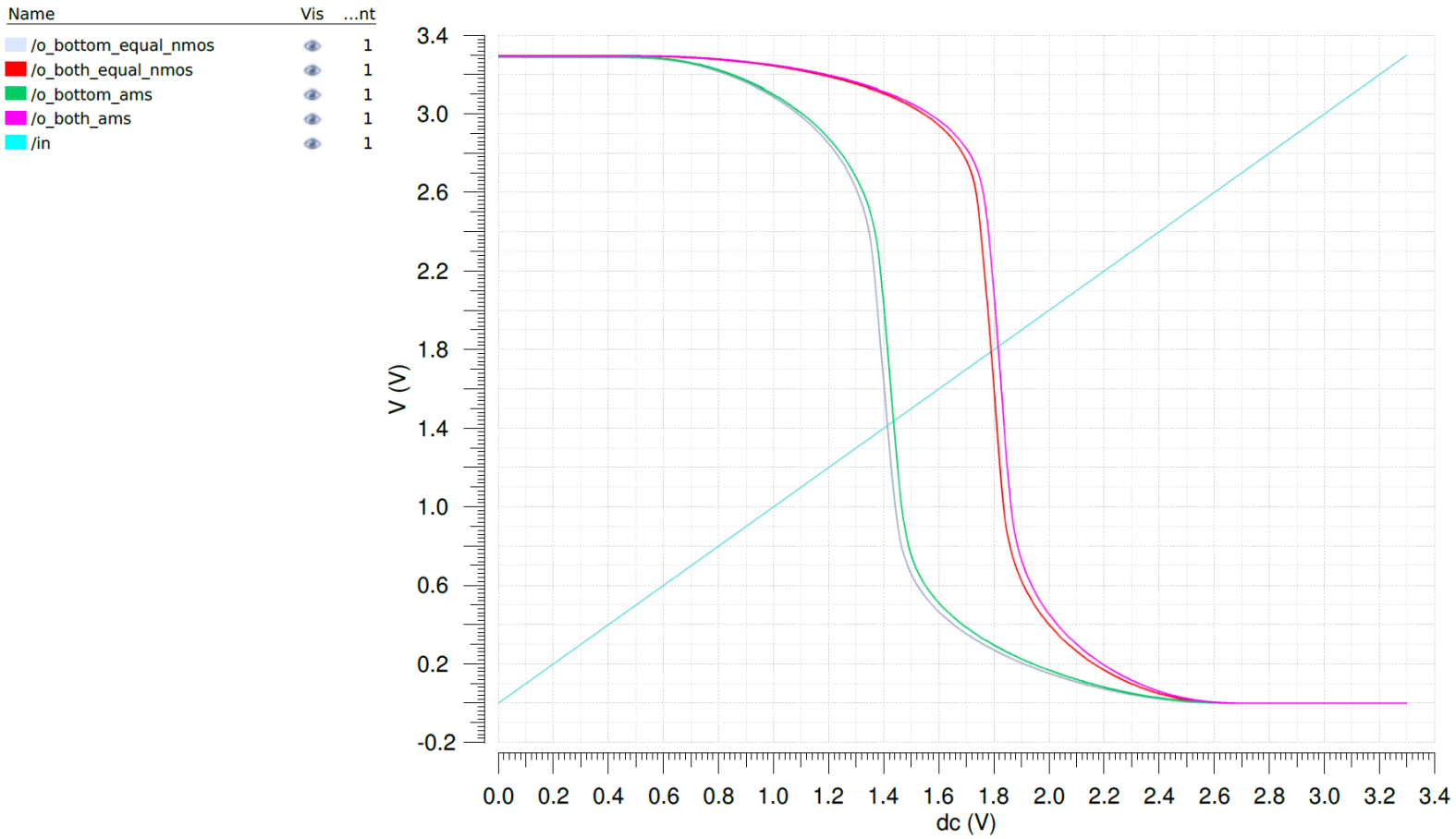
Transfer characteristics and noise margin for 2-Input-CMOS-NAND-Gate



$$\frac{dV_{out}}{dV_{in}}$$

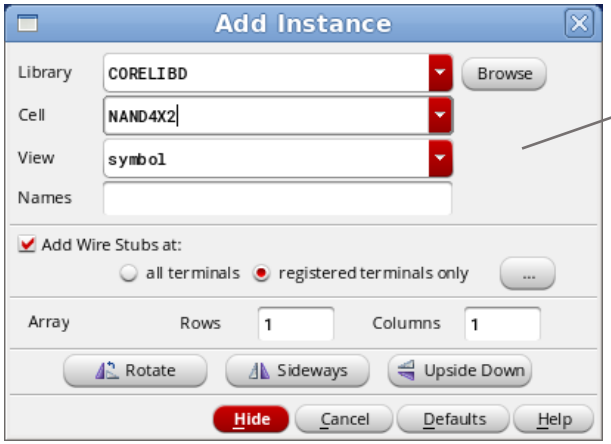


Transfer characteristic for 2-Input-CMOS-NAND-Gates

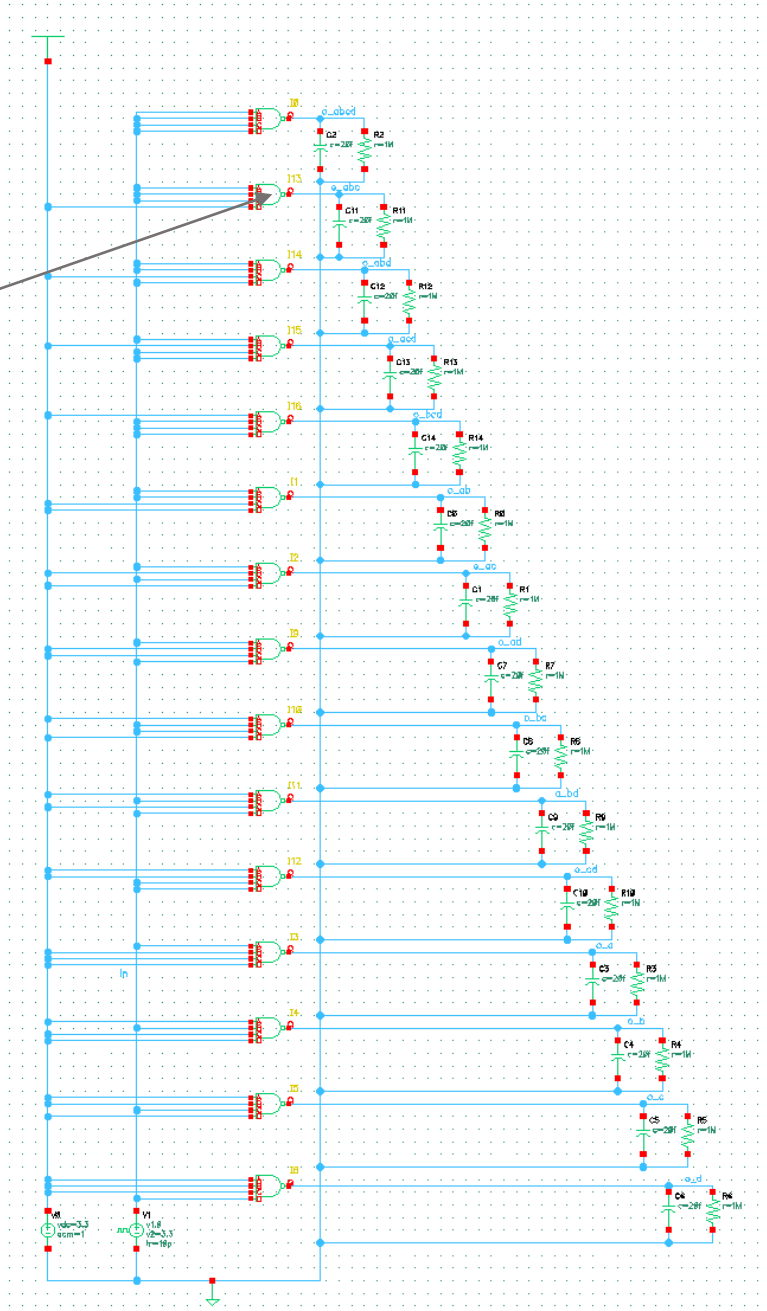


Transfer characteristic of 2-input-NAND-Gates from AMS-0.35µ-library
with $L_{NMOS,PMOS} = 0.35\mu\, W_{NMOS} = 1.325\mu, W_{PMOS} = 2.1\mu$ and self-made gate
with $L_{NMOS,PMOS} = 0.35\mu\, W_{NMOS} = 1.0\mu, W_{PMOS} = 1.6\mu$
(Characteristic for top N-transistor not shown, always beetween bottom and both)

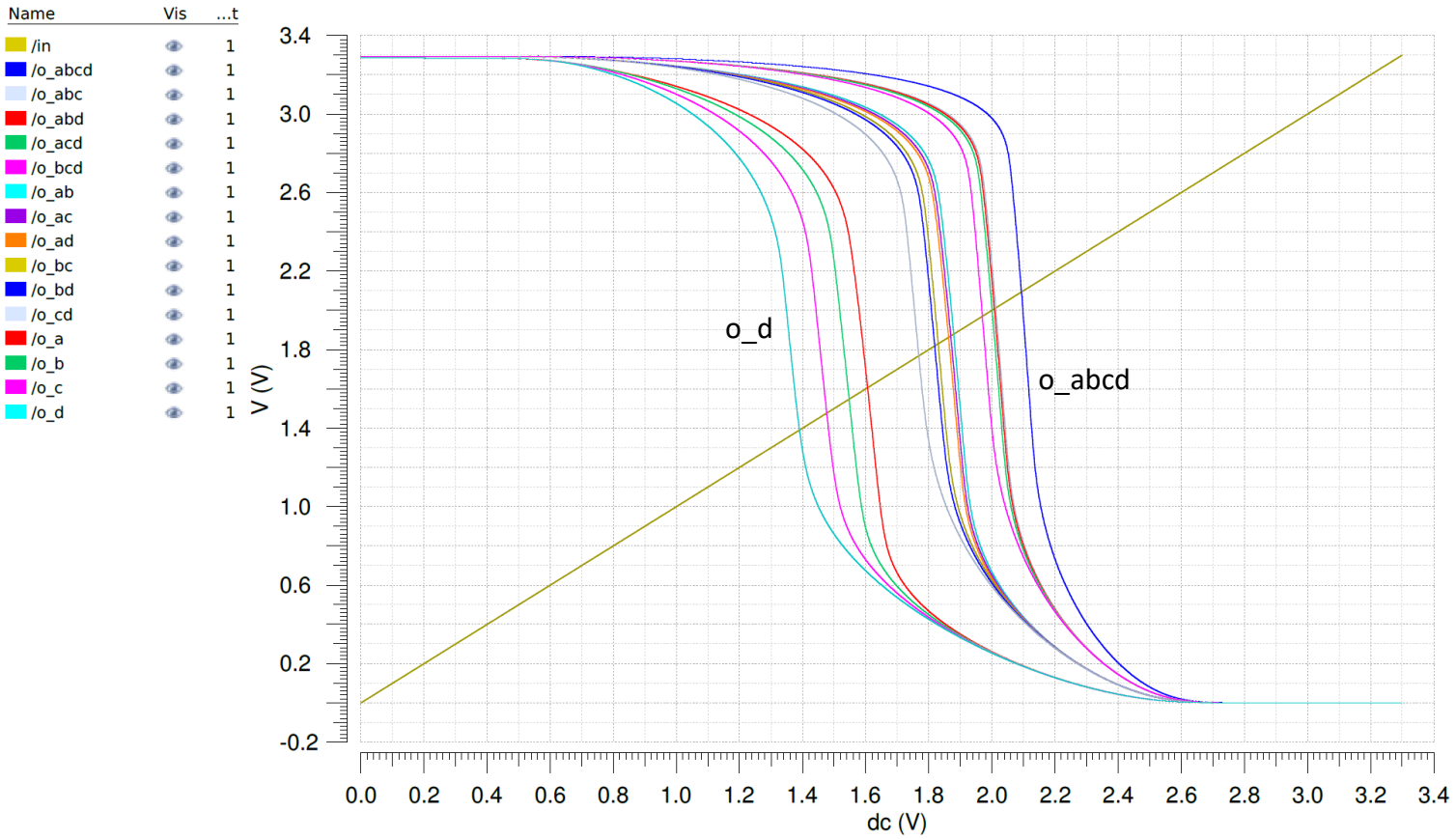
Simulation of 4-input-NAND from 0.35µm library



D-input uses NMOS-transistor nearest to GND, A-input is top NMOS-transistor.



4-Input-NAND-Gate



Transfer characteristic of 4-input-NAND-Gate from AMS-0.35µ-library
with $L_{NMOS,PMOS} = 0.35\mu\, W_{NMOS} = 1.05\mu, W_{PMOS} = 1.4\mu$
Leftmost line for switching lowest (nearest to ground)nmos-transistor only,
rightmost line for all 4 inputs switched simultaneously