

Cadence + AMS-Hitkit

Tutorial for creation of an inverter cell from schematic to layout with CADENCE using AMS-Hitkit and hints for multi-input gates

1. Using the Linux (CentOS) environment
2. Starting CADENCE with AMS-Hitkit
3. Creating a new library
4. Schematic entry
5. Creating a symbol and a testbench
6. Spice-Simulation using ADE XL
 - Analyses selection and setup
 - Using global variables
 - Parametric simulation
7. Starting Layout XL
 - Generate layout from schematic
 - The layer window
 - Wires, vias/contacts, wells
8. Design rule check
9. Layout versus schematic check (LVS)
10. Parasitic extraction (QRC)
11. Simulation of the extracted model (Post-layout simulation)

Some UNIX-commands

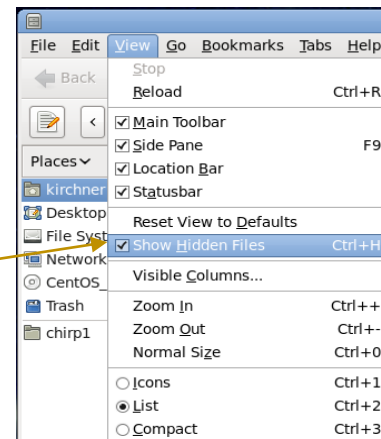
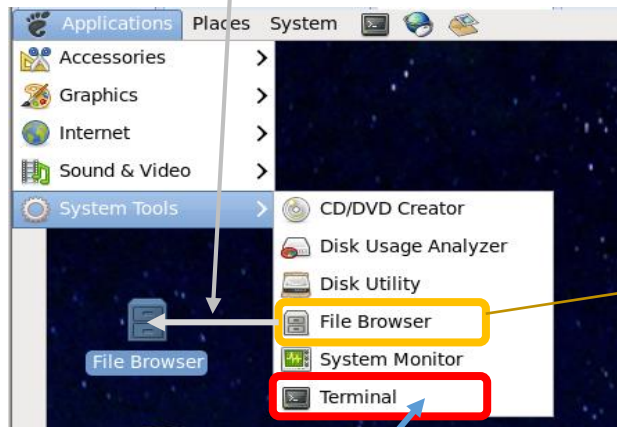
We use CentOS-Linux (Free version "Community Enterprise OS" of RedHat), because Cadence supports RedHat or Suse.
We use the Kornshell (ksh), because it is the standard shell at ITMZ Uni Rostock.

pwd
ls, ls -alsi, ls dir
cd -> cd ~/ske -> cd ./ske
mkdir newdir
cp, cp -r, cp -p
mv
chmod, chmod -R chmod 744 file
grep
use of | for pipeline -> ls | grep pattern
rm, rm -r
rmdir
cat file
man cmd

print working directory
list
change directory
make directory
copy files/directories (recursive, preserve attributes)
move or rename directories
change file mode bits (security) -> -R recursive
filter for pattern
use command output as input for next command
remove/delete
remove directory
show file at standard output
show manual of cmd

Our client computers use the "supported" CentOS 6,
but the server is CentOS 7 (not yet supported to run Cadence)

Move icon to desktop for easy use



Or Right-Mouse on Background and select "Open Terminal"

To save windows images (.png) : Alt-Print

Unix-command to remove Cadence lock files (Close all Cadence programs before!) : `find ~/ -name "*.cdslock" -exec rm {} \;`

AMS-HitKit - Start

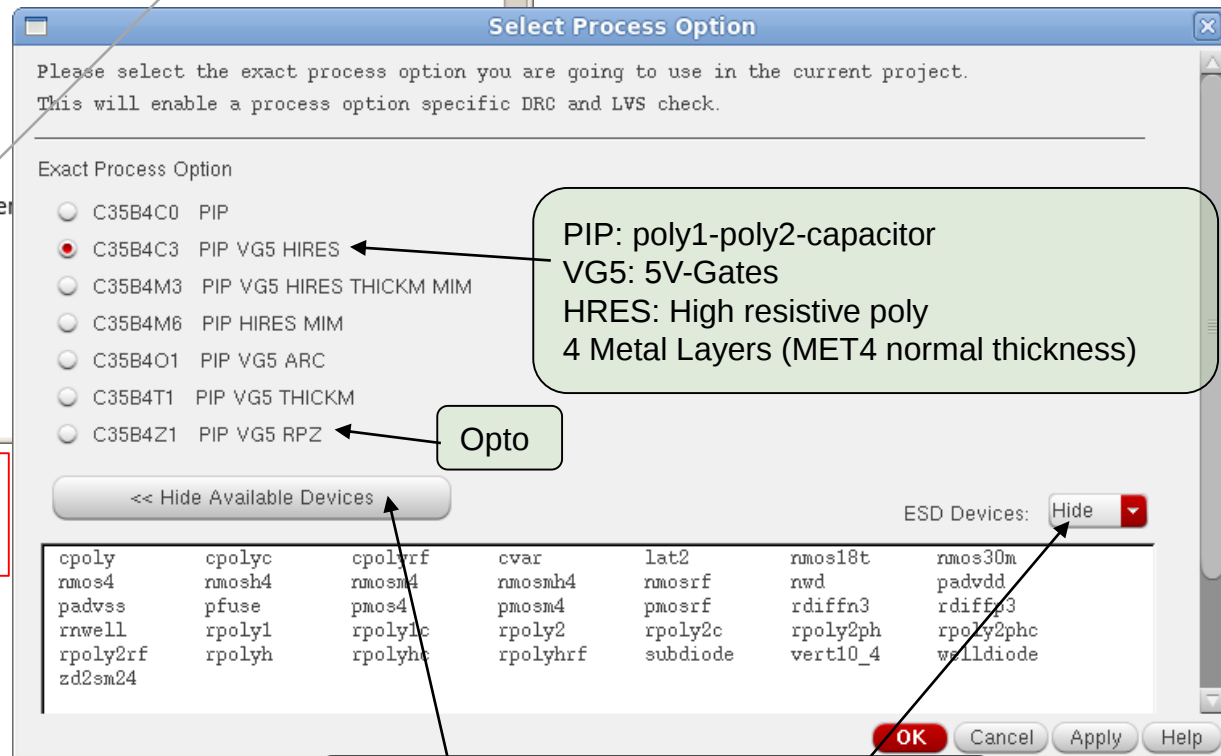
= Starting Cadence Design Framework with Libraries, Rules, Scripts provided for AMS-technology

```
Terminal
File Edit View Search Terminal Help
kirchner@KaterCentOS6: cd
kirchner@KaterCentOS6: pwd
/home/kirchner
kirchner@KaterCentOS6: mkdir myproject
kirchner@KaterCentOS6: cd myproject
kirchner@KaterCentOS6: ams_cds -newtech c35b4 &
[1] 6647
kirchner@KaterCentOS6:
Creating a new .cdsinit file...
Creating a new cds.lib file
Creating a new .simrc file...
Creating a new assura_tech.lib file
Creating a new Calibre cellmap file
Creating a new streamout template file
mv: cannot move './.cadence/dfII/layerSets/cadence/cadence.signature.xml': Permission denied
Creating a new layerSets directory
Creating a new jobpolicy directory
Creating a new .cdsinit_local file...
Creating Hierarchy Editor templates...
[1] 6724
virtuoso : HIT-Kit=ams 4.10 tech=c35b4
kirchner@KaterCentOS6: 
```

First start !
Later use "ams_cds" simply!
(or "ams_cds &" to release the terminal for further use)

Do not use your homedir!
Create a separate project directory!

Make your favourite directory structure
~/ske
~/ske/inverter



PIP: poly1-poly2-capacitor
VG5: 5V-Gates
HIRES: High resistive poly
4 Metal Layers (MET4 normal thickness)

Basic elements, available in this technology
Show additional elements for ESD
ElectroStatic Discharge

You may use one single directory for different designs.

AMS-HitKit - Start



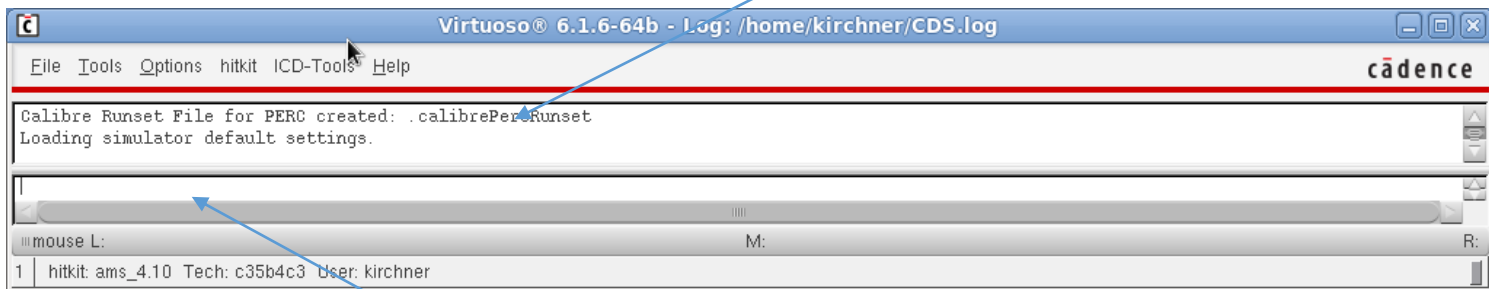
Would stay open as long as ams_cds is running



Window open for some seconds after ams_cds start

Command Interpreter Window - CIW

Messages



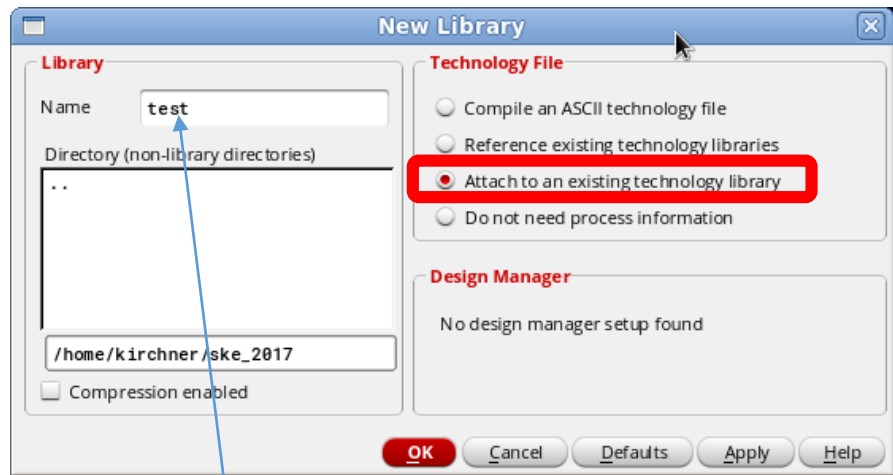
Command Inputs

AMS-HitKit - A new library

Command Interpreter Window - CIW



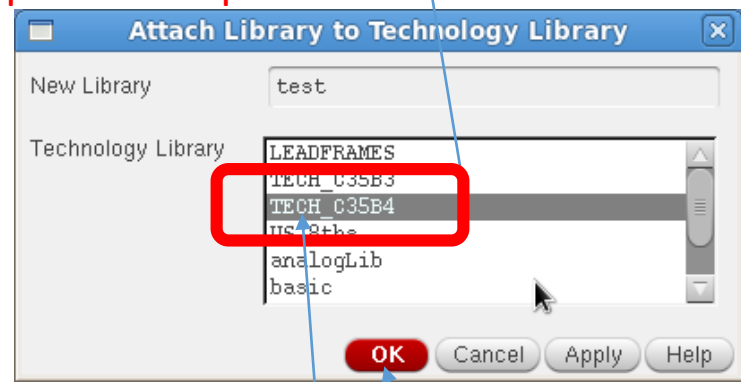
File -> New -> Library



Choose a name for your library!
(You may use one library for different designs.)

Select
"Attach to an existing technology library" -> OK

important step!



We use the 4 metal layer technology here.
Do not press OK before you have selected the TECH-library!

Quit with OK!

AMS-HitKit - A new cellview

Command Interpreter Window CIW

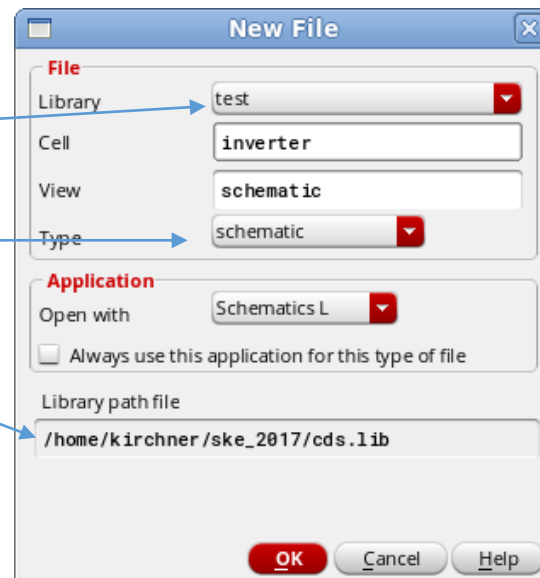


File -> New -> Cellview

Your new library

Start with schematic view

Depends on your project path



Choose a cell name, check "schematic" as cellview -> OK

Quit with OK !

AMS-HitKit Schematic Editor is open

The screenshot displays the AMS-HitKit Schematic Editor environment. The main window is the Schematic Editor, titled "Virtuoso® Schematic Editor XL Editing: test inverter schematic". It features a menu bar with "Launch", "File", "Edit", "View", "Create", "Check", "Options", "Migrate", "Window", "HIT-KIT Utilities", and "Help". Below the menu is a toolbar with various icons for file operations, editing, and simulation. The workspace shows a schematic diagram with components and connections. A text box in the center of the workspace contains the following text:

Normally the background is black, you may (but you should not for normal work) change to white by modifying an entry in your ~/.Xdefaults file:
!Opus.editorBackground: #000000 -> Opus.editorBackground: #ffffff

For printing it is sometimes interesting to have a white background but not all the design colours match white background.

When you have some content it is possible to create images with white background using "File -> Export Image". There opens a form where you can change the background colour. Try it!

The Terminal window shows the following commands and output:

```
kirchner@KaterCent056: cd
kirchner@KaterCent056: pwd
/home/kirchner
kirchner@KaterCent056: mkdir myproject
kirchner@KaterCent056: cd myproject
kirchner@KaterCent056: ams_cds -newtech c35b4 &
[1] 6647
kirchner@KaterCent056:
Creating a new .cdsinit file...
Creating a new cds.lib file...
Creating a new .simrc file...
Creating a new assura_tech.lib file
Creating a new Calibre cellmap file
Creating a new streamout template file
mv: cannot move './.cadence/dfII/layerSets/cadence.signature.xml' to './.cadence/cadence.signature.xml': Permission denied
Creating a new layerSets directory
Creating a new jobpolicy directory
Creating a new .cdsinit local file...
Creating Hierarchy Editor templates...
[1] 6724
virtuoso : HIT-Kit=ams 4.10 tech=c35b4
kirchner@KaterCent056: []
```

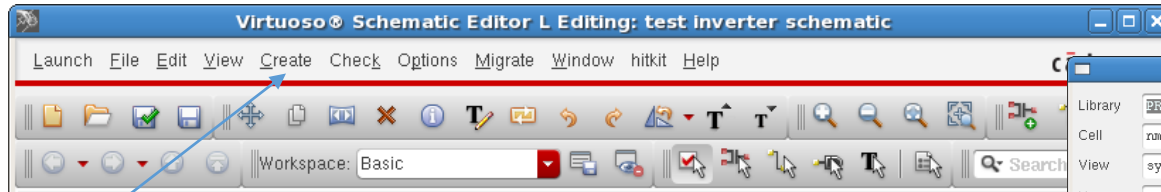
The Library Manager window shows the "WorkArea: /home/kirchner/ske_2017" and contains three panes: "Library", "Cell", and "View". The "Library" pane lists various components, including "test", "ieee", "ncinternal", "ncmodels", "ncutils", "sbaLib", "sdlib", "std", "synopsys", "test", and "vital_memory". The "Cell" pane shows the "inverter" component. The "View" pane shows the "schematic" component. The "Messages" pane at the bottom displays the log file path: "Log file is '/home/kirchner/ske_2017/libManager.log'".

The Log window shows the following text:

```
Virtuoso® 6.1.5-64b - Log: /home/kirchner/CDS.log
File Tools Options HIT-KIT Utilities Help
Loading leToolbox.cxt
Loading hsm.cxt
Loading lx.cxt
Loading lce.cxt
Loading lce.cxt
mouse L: schSingleSelectPt() M: ddsOpenLibManager() R: schHiMousePopUp()
1(4) HIT-Kit: ams_4.10 Tech: c35b4c3 User: kirchner Cmd: Sel: 0
```

Try to have a fixed arrangement for open windows (Terminal, CIW ..)

Schematic entry - Components

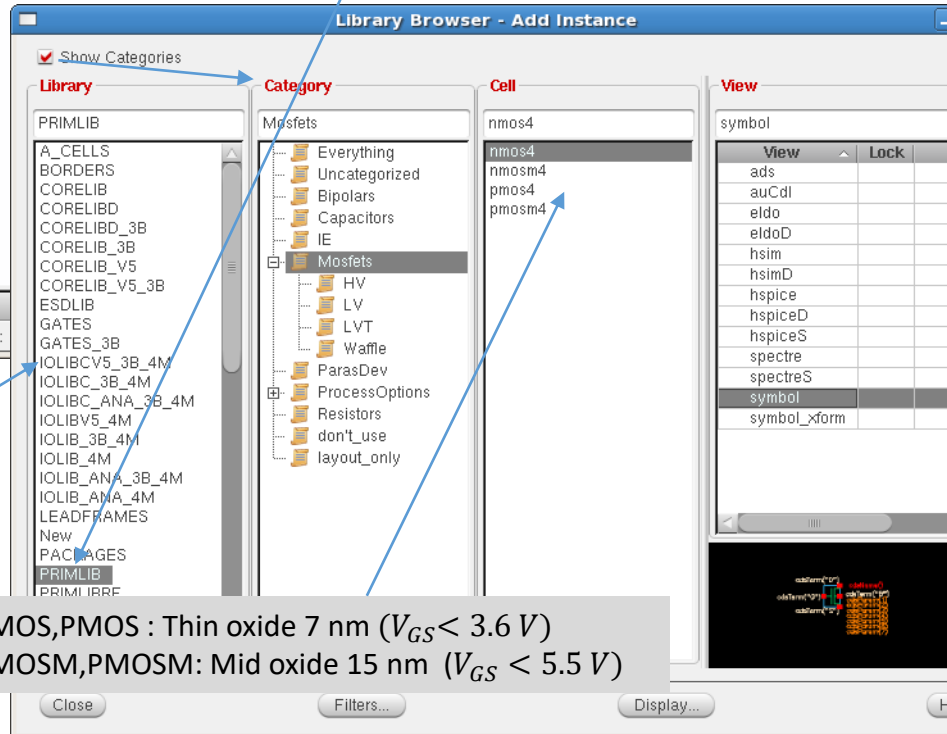


Create -> Instance
(hotkey "i")

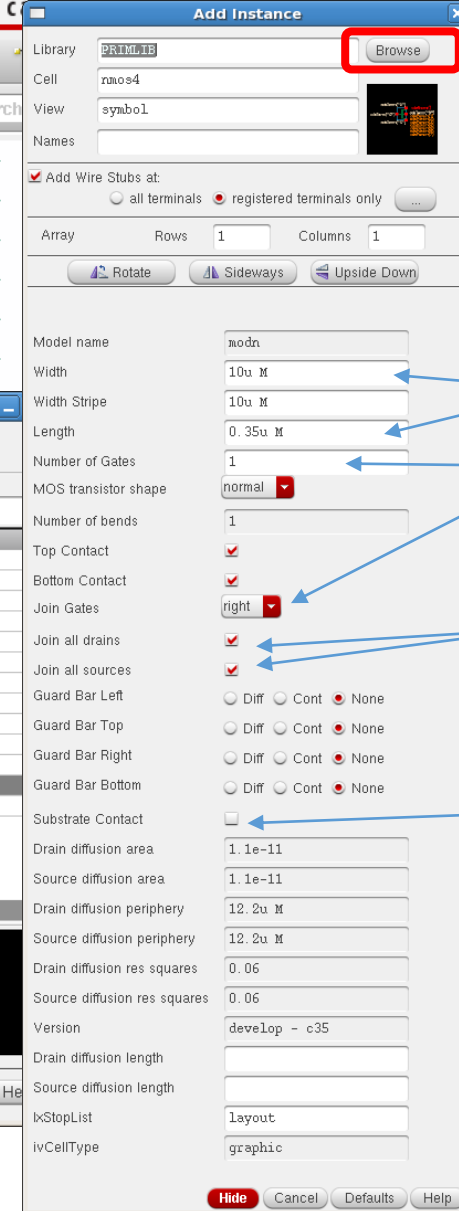
PRIMLIB contains all the
available elements (primitives).

nmos4
MN0
wtot=10u.
l=0.35u
ng=1
modn

Cells



NMOS,PMOS : Thin oxide 7 nm ($V_{GS} < 3.6 V$)
NMOSM,PMOSM: Mid oxide 15 nm ($V_{GS} < 5.5 V$)



Open Library Browser

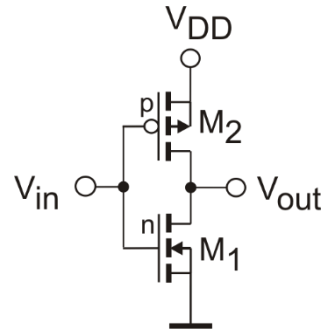
$\frac{W}{L}$
Finger

compact

Substrate contact
in layout

Instance properties
may be changed
in layout-process
later

CMOS Inverter calculation



There is the same current flowing through both transistors. Beide. For ideal switching point is $V_{in} = V_{GSn} = V_{SGp} = V_{out} = V_{DSn} = V_{SDp} = \frac{V_{DD}}{2}$. Because of $|V_{DS}| > |V_{GS} - V_{th}|$ both transistors are in the pinch-off state and we can assume:

$$\frac{\beta_n}{2} (V_{inSP} - V_{thn})^2 = \frac{\beta_p}{2} (V_{DD} - U_{inSP} - U_{thp})^2$$

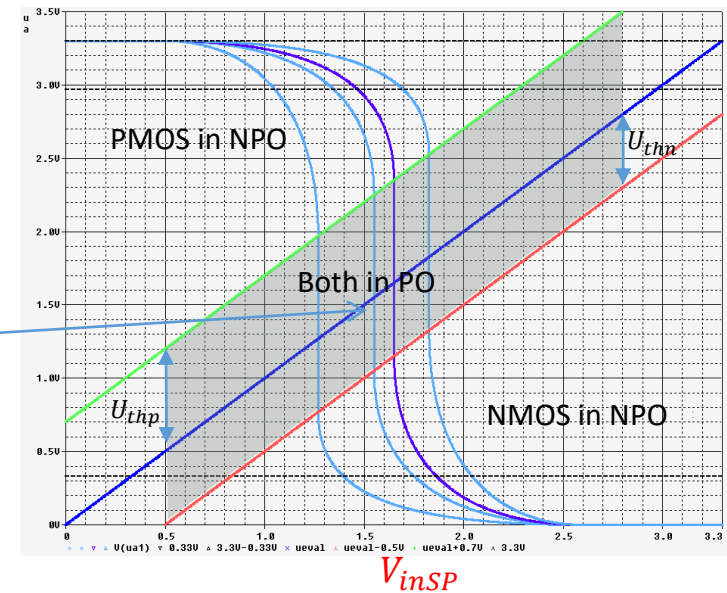
$$V_{thn} = 0.5V, KPN = 170 \frac{\mu A}{V^2}$$

$$V_{thp} = 0.65V, KPP = 58 \frac{\mu A}{V^2}$$

Dissolving for V_{inSP} :

$$\sqrt{\beta_n} (V_{inSP} - V_{thn}) = \sqrt{\beta_p} (V_{DD} - V_{inSP} - V_{thp})$$

$$V_{inSP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{thn} + V_{DD} - V_{thp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$



For desired $V_{inSP} = \frac{V_{DD}}{2}$ we calculate the relation $\frac{\beta_n}{\beta_p}$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}} \right)^2$$

$$\beta = KP \cdot \frac{W}{L}$$

using: $KPN = 3 \cdot KPP$

$$\frac{\left[\frac{W}{L} \right]_n}{\left[\frac{W}{L} \right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}} \right)^2 \approx \frac{1}{3}$$

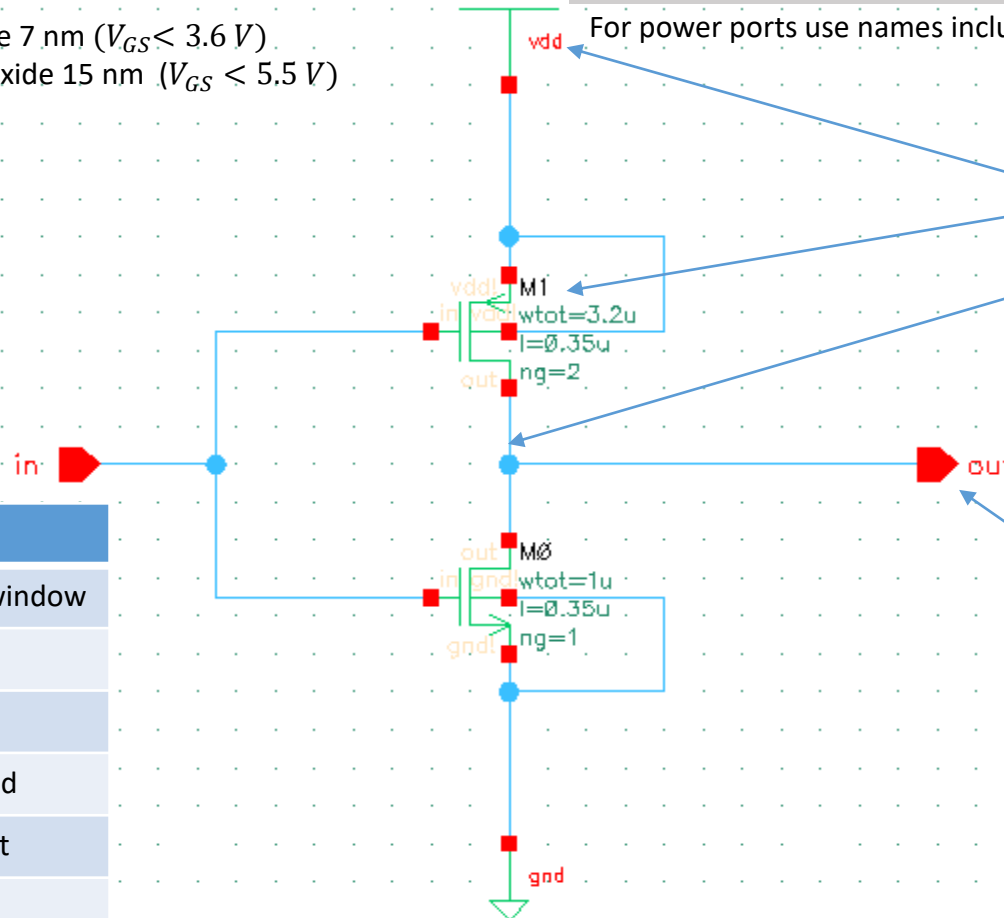
for $|V_{DD}| \gg |V_{thp} - V_{thn}|$

Inverter schematic

NMOS,PMOS : Thin oxide 7 nm ($V_{GS} < 3.6\text{ V}$)
 NMOSM,PMOSM: Mid oxide 15 nm ($V_{GS} < 5.5\text{ V}$)

vdd, gnd etc. from library "analogLib/globals"

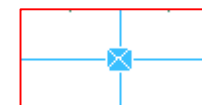
For power ports use names including "vdd" or "vcc"



For ground ports use names including "gnd".
 (Some scripts (ERC) need this naming convention.)

key	function
F3	show option window
u	undo
U	redo
e	descend & read
E	descend & edit
CTRL-e	return
DEL	delete

key	function
i	create instance
w	create wire
M	move
m	stretch (im Layout "S" !)
c	copy
q	object properties
p	add pin
l	add wire name (label)
x	check current cellview
f	fit
]	zoom in
[	zoom out

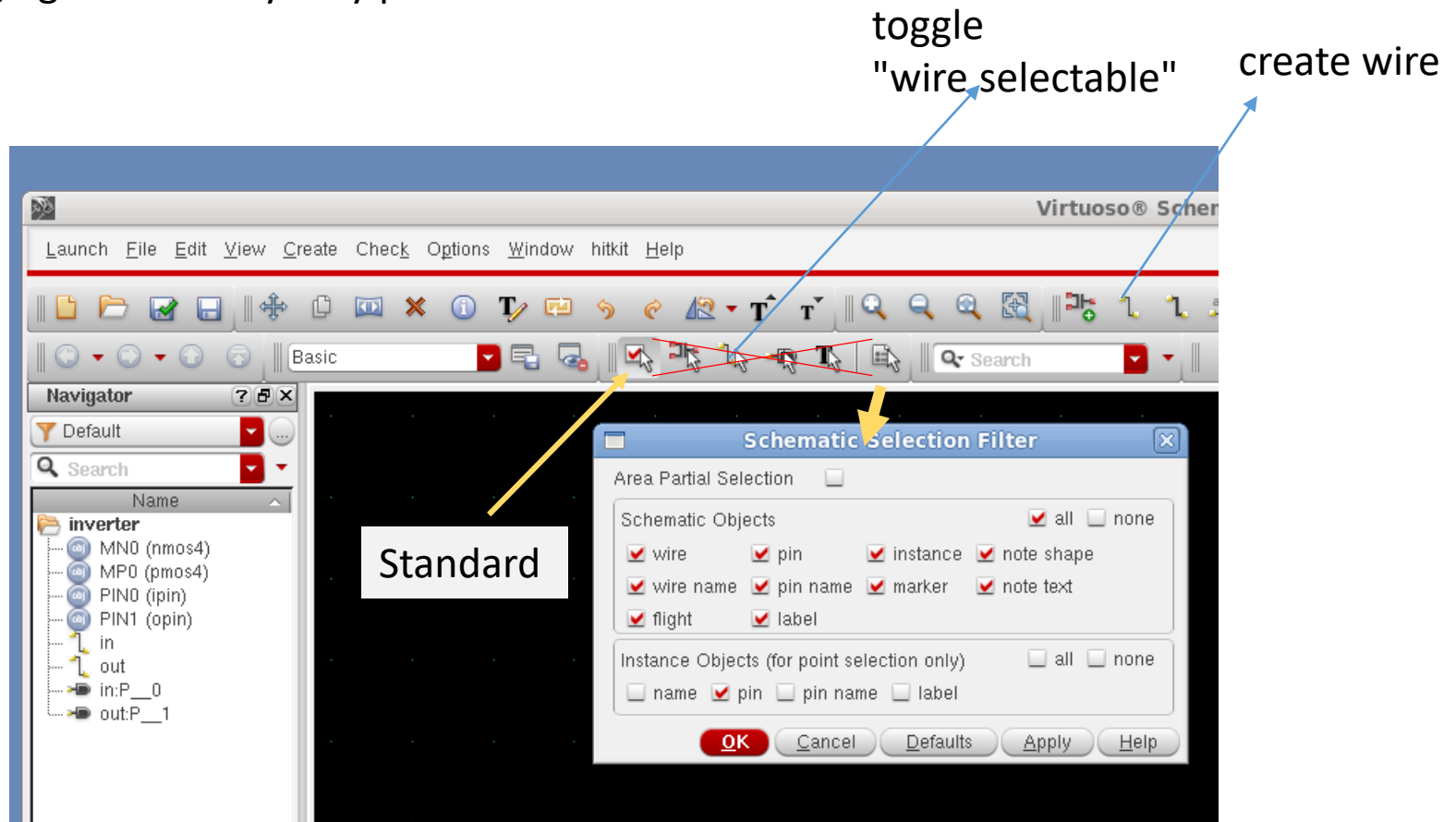


Avoid crossover dots.
 Warnings! May be deselected
 Check-> Rules-> Physical

File -> Check and Save (shft-x)

Schematic Editor: Filter

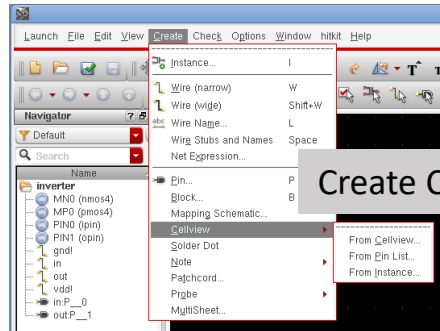
Schematic editor has a filter function for selectable objects!
Changing accidentally may prohibit selection!



Inverter Symbol from Schematic

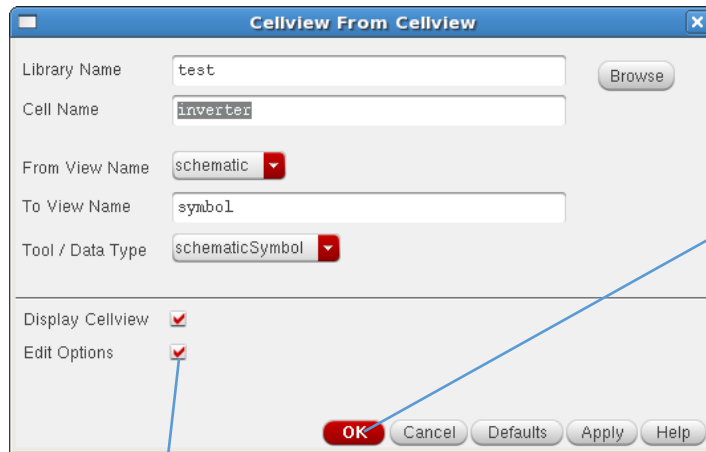
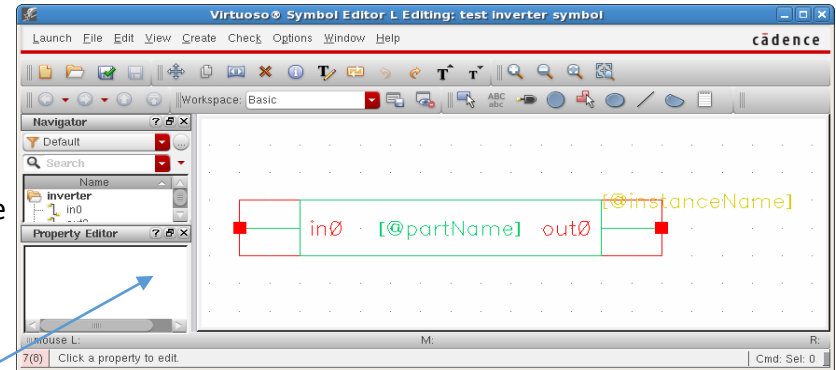
Symbol needed to use our design in higher levels of hierarchy.

First Example is the insertion of the design in a testbench.

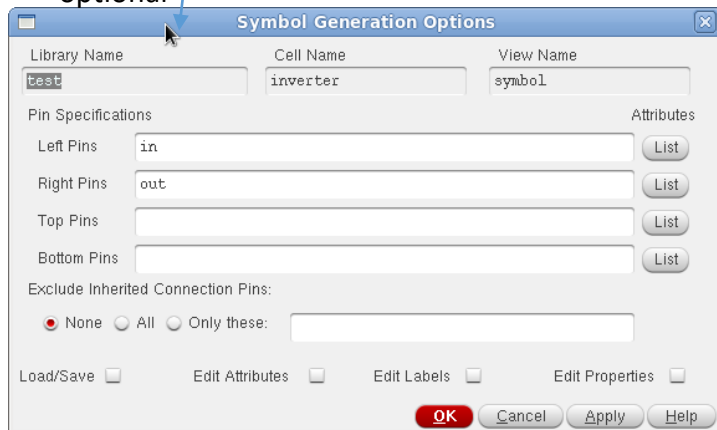


Create Cellview -> From Cellview -> OK

Standard: rectangle



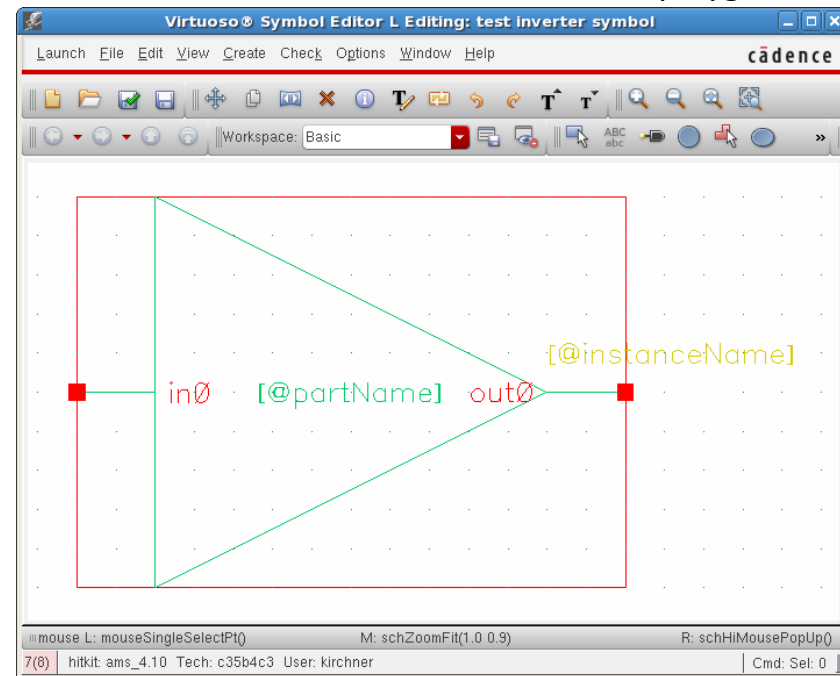
optional



One may change shapes:

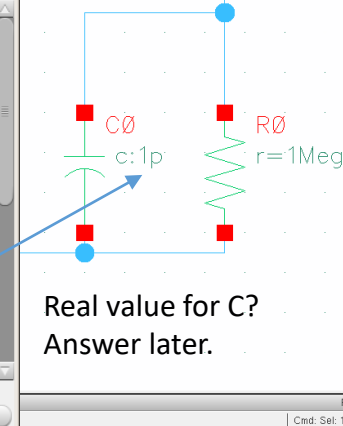
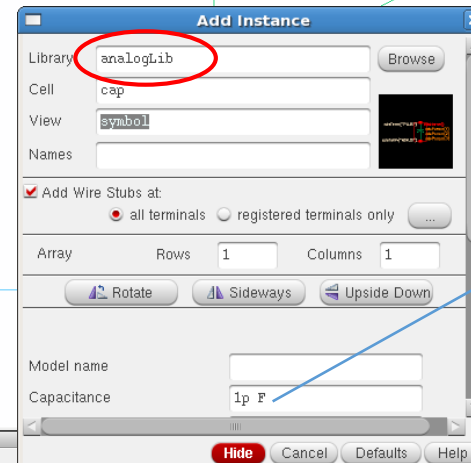
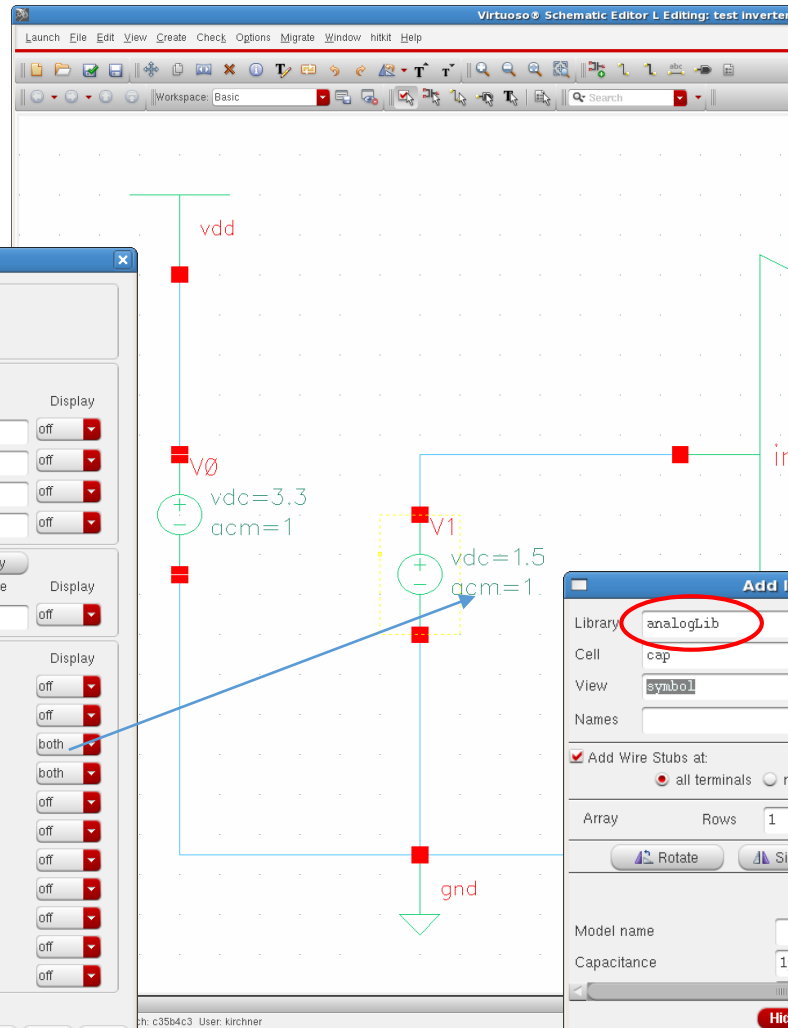
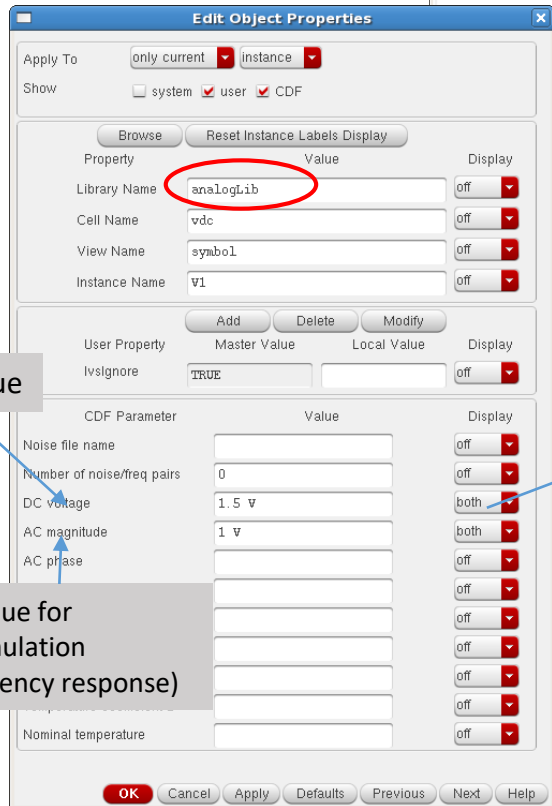
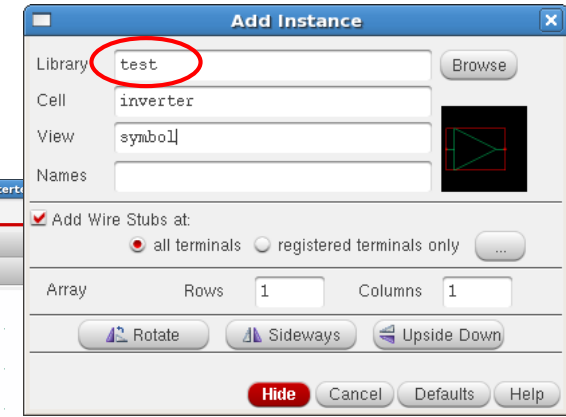
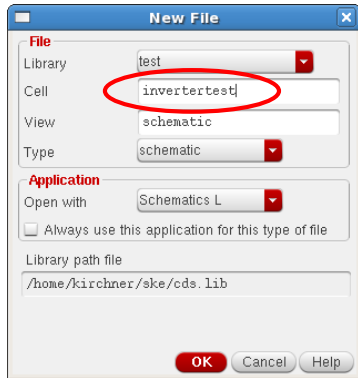
outline (green), selection frame (red)

use: stretch, delete, move, create polygon



Inverter Schematic for Simulation -> Testbench

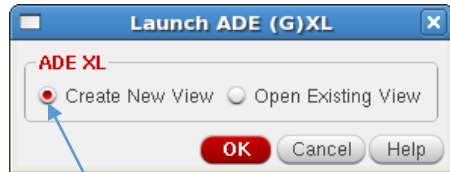
In CIW (or Library Manager): File -> New -> Cellview



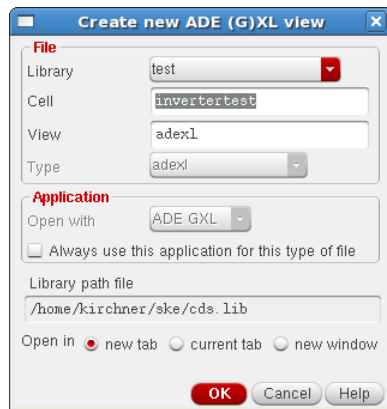
Real value for C?
Answer later.

Simulation ADE GXL Start

From the Schematic Editor -> **Launch** -> **ADE GXL**

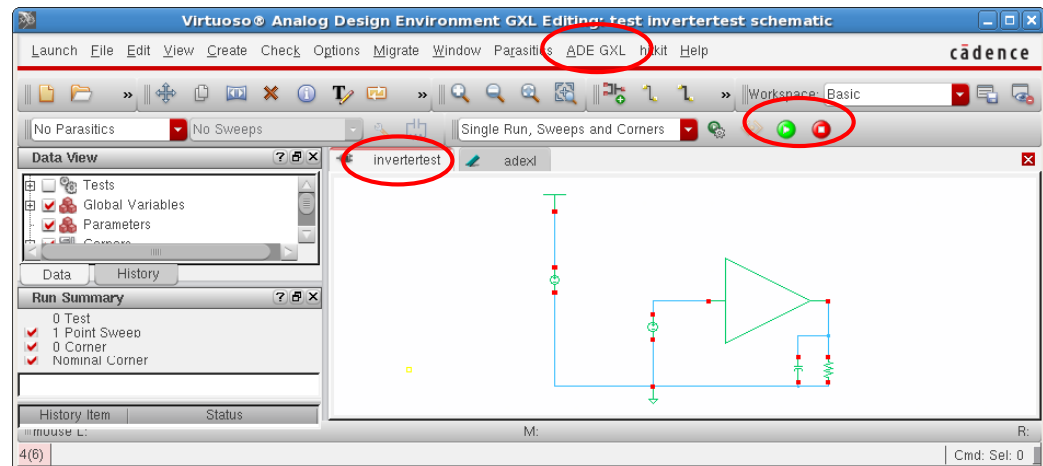
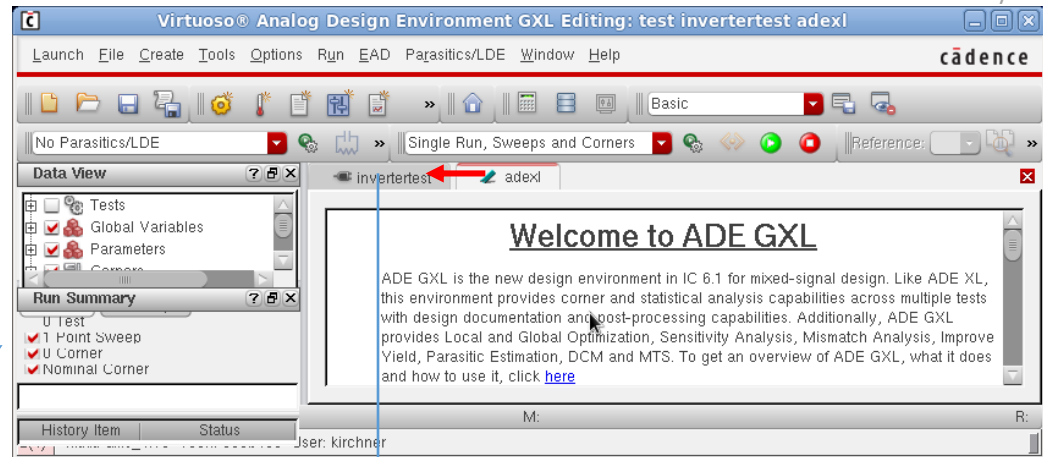


ADE XL creates a new view!

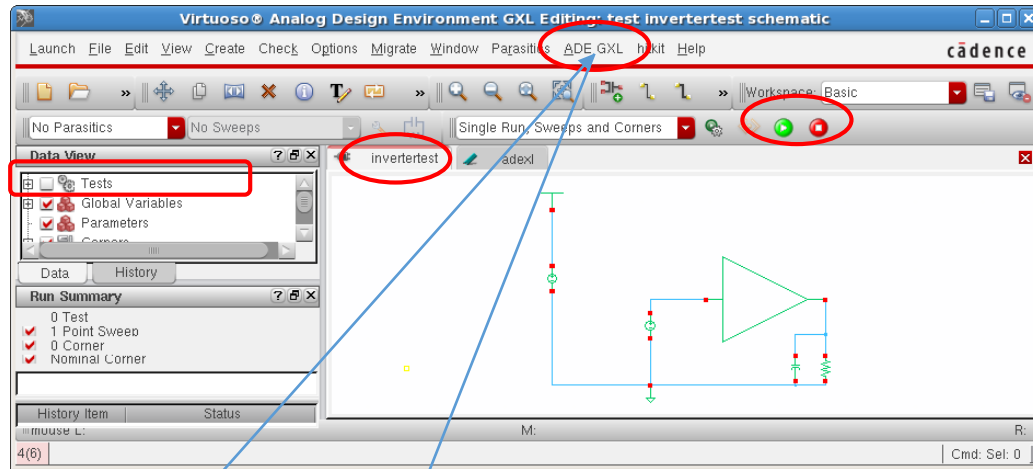


ADE (G)XL usage differs from ADE L
Most tutorials use older ADE L

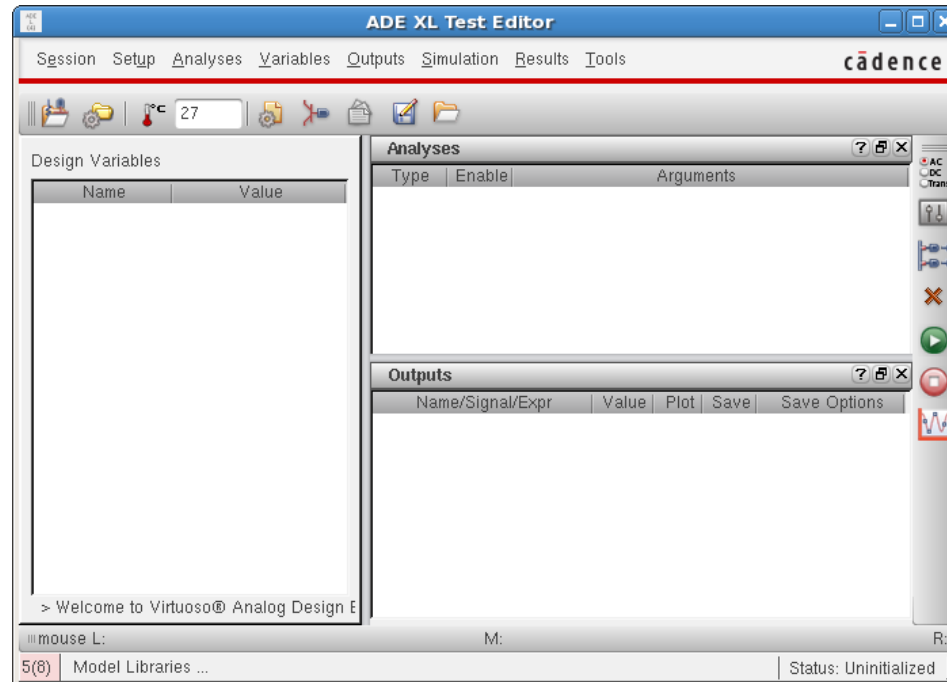
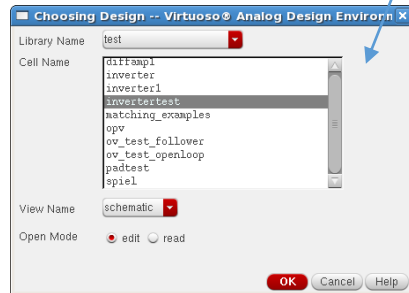
LDE Layout Dependent Effects
EAD Electrically Aware Design



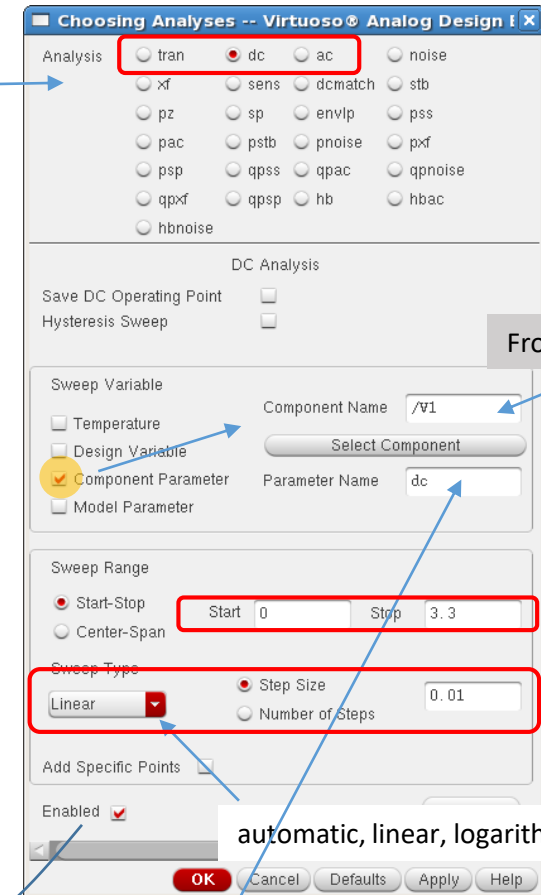
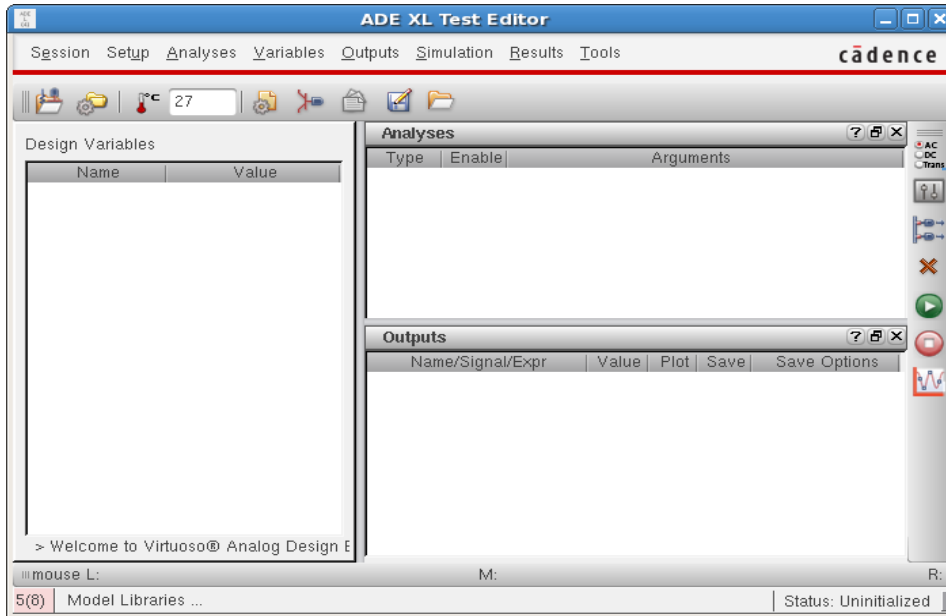
Simulation ADE GXL Create Test



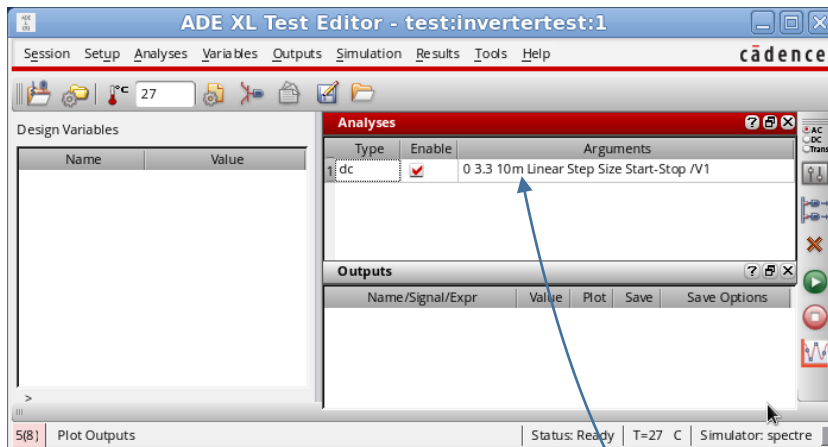
Choose: ADE GXL -> Create -> Test



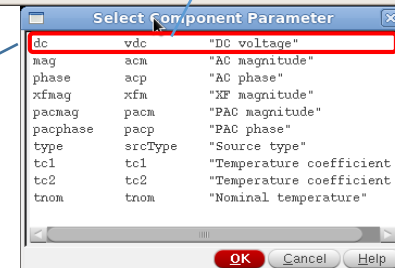
Simulation ADE GXL Create Analyses



From Schematic

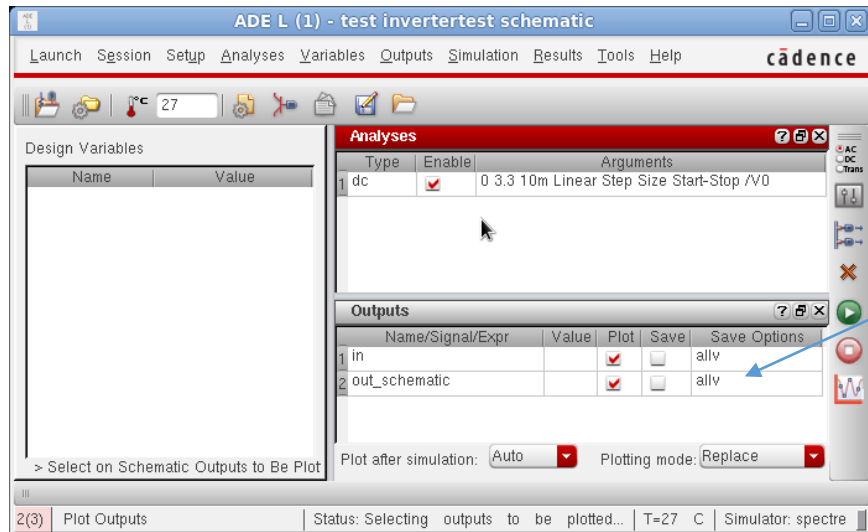
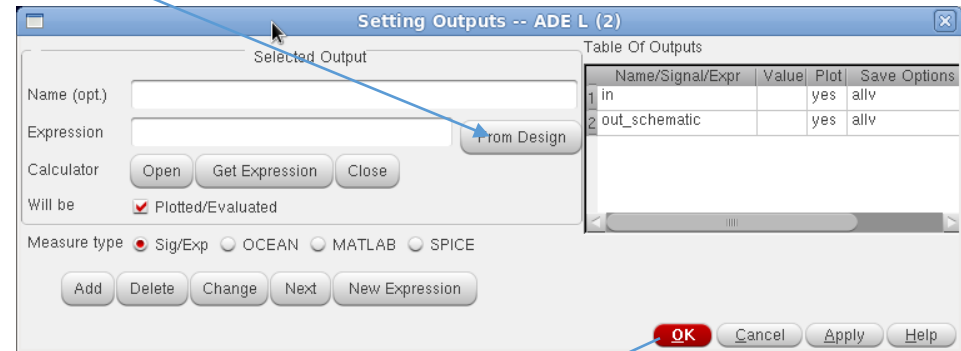
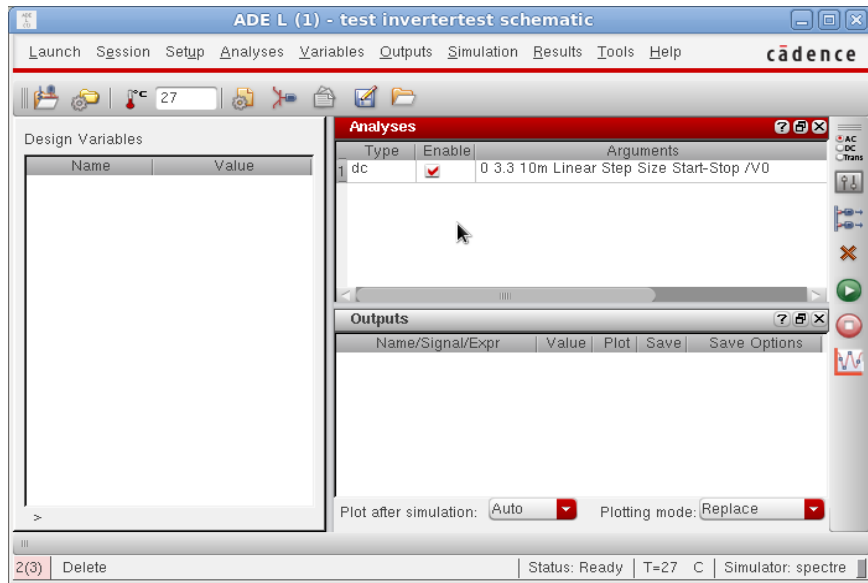


Create/Edit analyses
Design Variables
Simulation Outputs
Delete selected analyses
Run enabled analyses
Stop
Plot



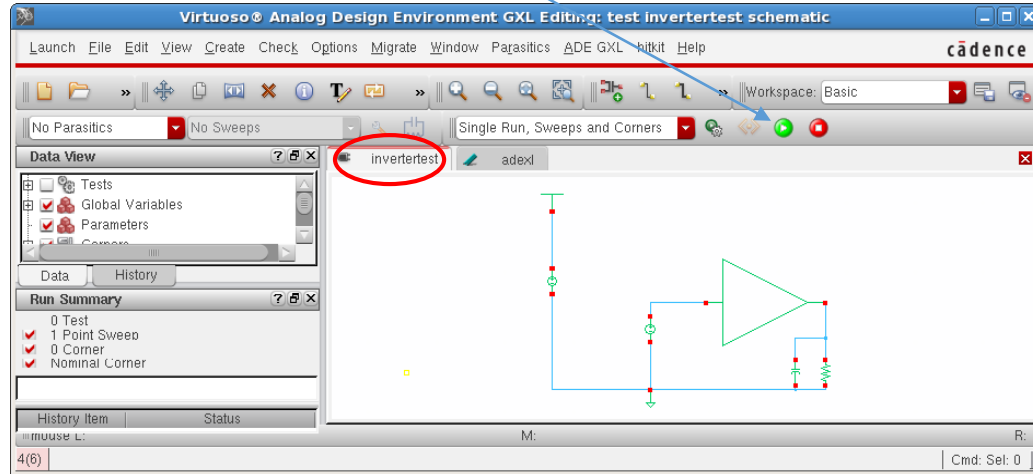
automatic, linear, logarithmic

Simulation ADE-XL/L Choose Outputs



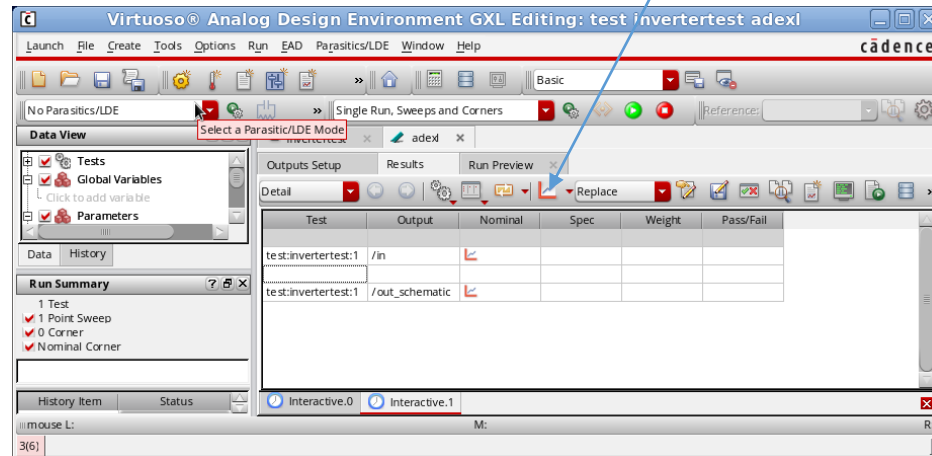
Simulation RUN (in ADE-GXL)

Run Simulation

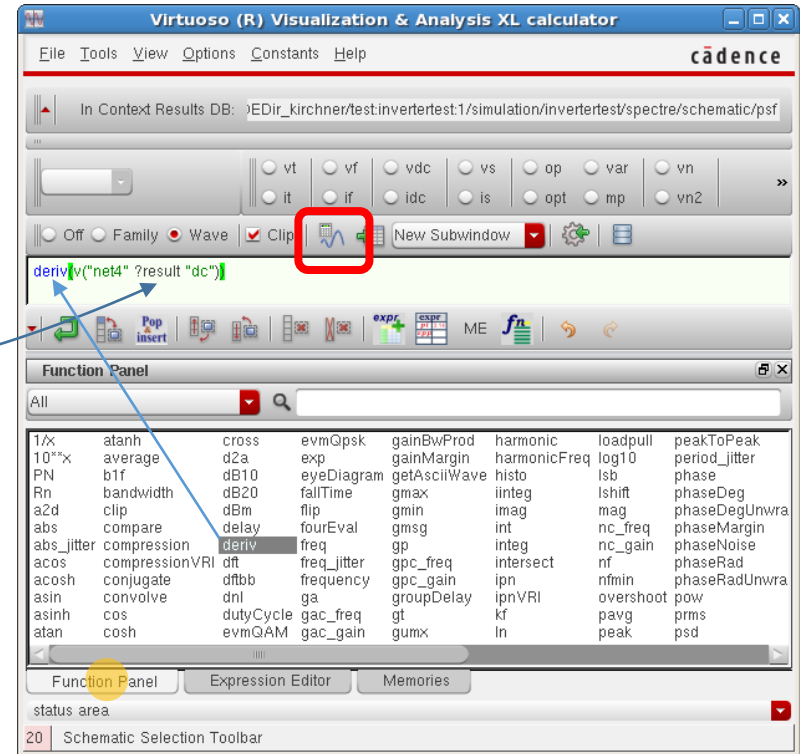
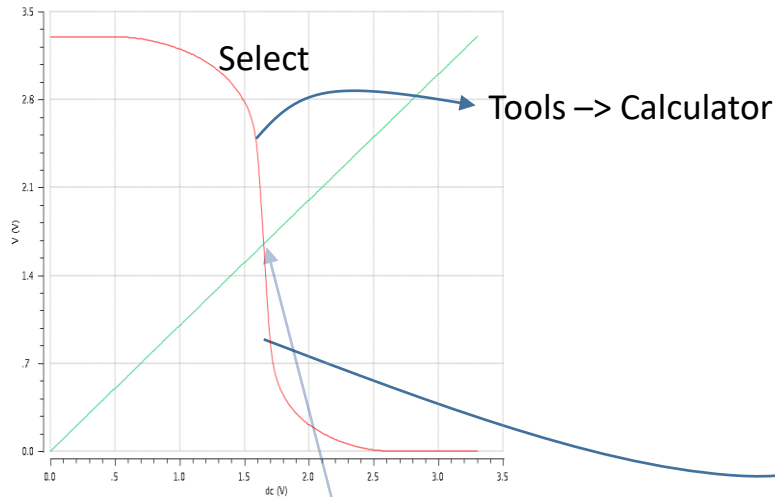


Common Errors stopping execution of simulation:
Design changed and not saved.
Unexpected/unassigned variables due to input errors
mostly for component values.
Example: Using "Meg" instead of "M" for "Mega..
-> Creates a variable "eg"

Plot outputs

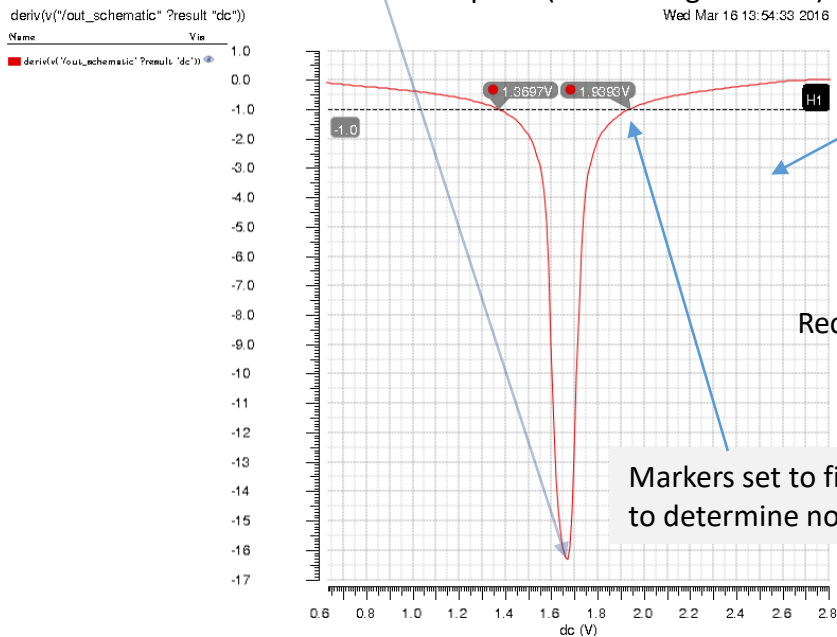


Simulation ADE-L Evaluate Results



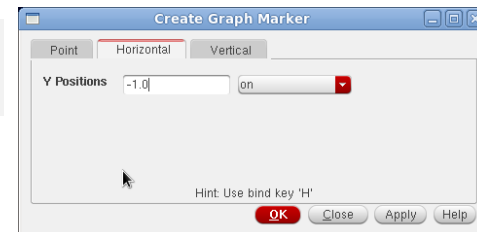
Inflexion point (max. abs. gain value)

Wed Mar 16 13:54:33 2016 1



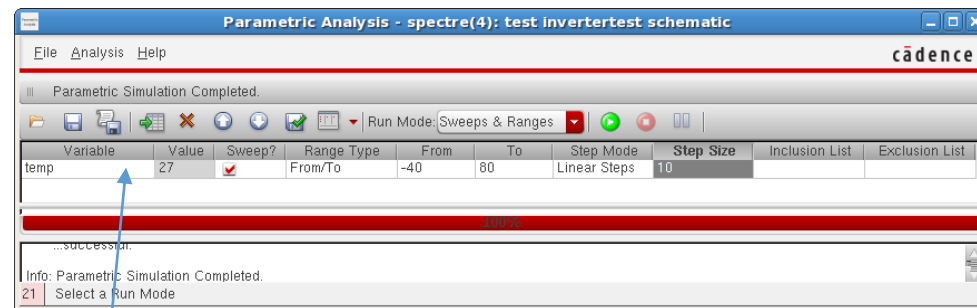
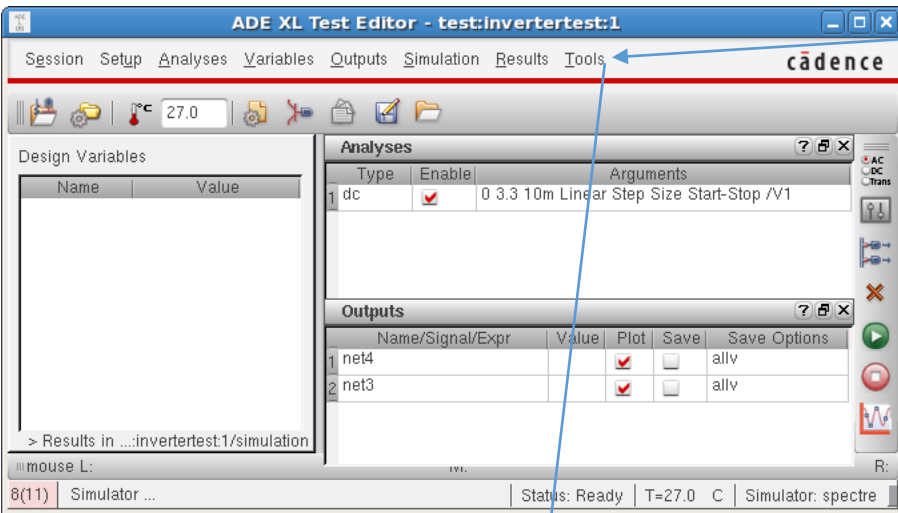
Recommendation: Move derivation plot to new subwindow (RM-> Move to)

In Visualization&Anlaysia Window -> Marker -> Create Marker

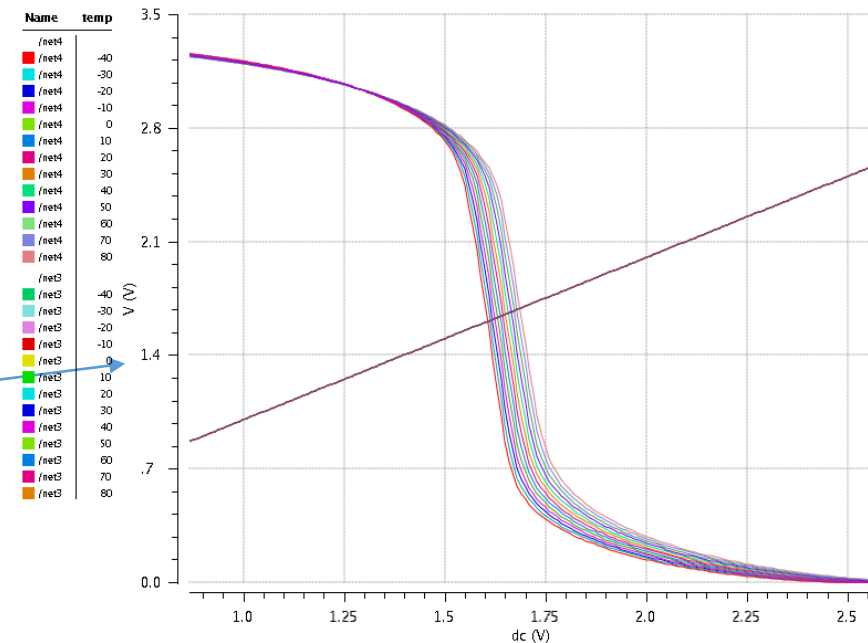


Simulation Parametric Analysis – Temperature (Built in)

Tools -> Parametric Analysis

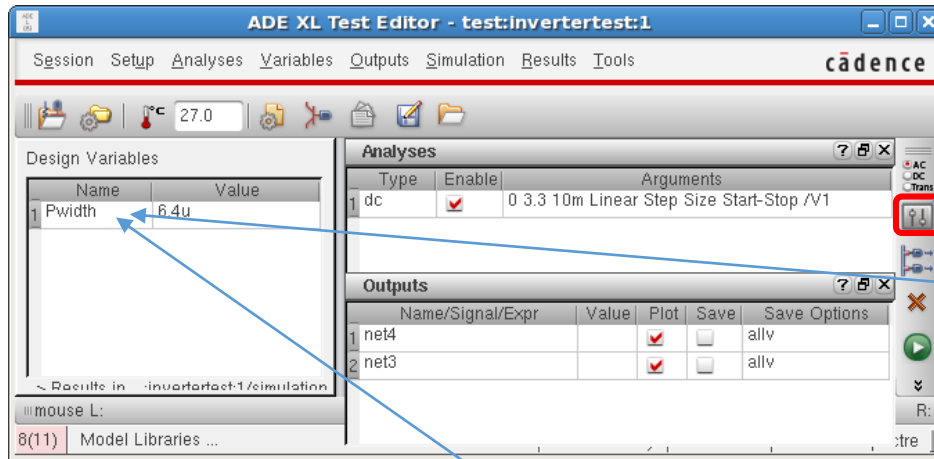


Select "temp" (There is nothing more when you start!)
Try the other entries! Here: -40°C to 80°C in 10° steps)

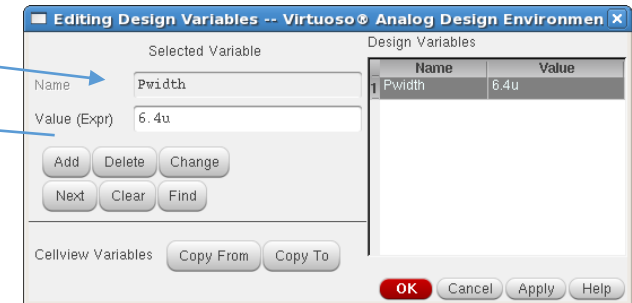


Simulation Parametric Analysis – Global Variables

As an example we replace the fixed width of the PMOS transistor by a parameter "Pwidth"

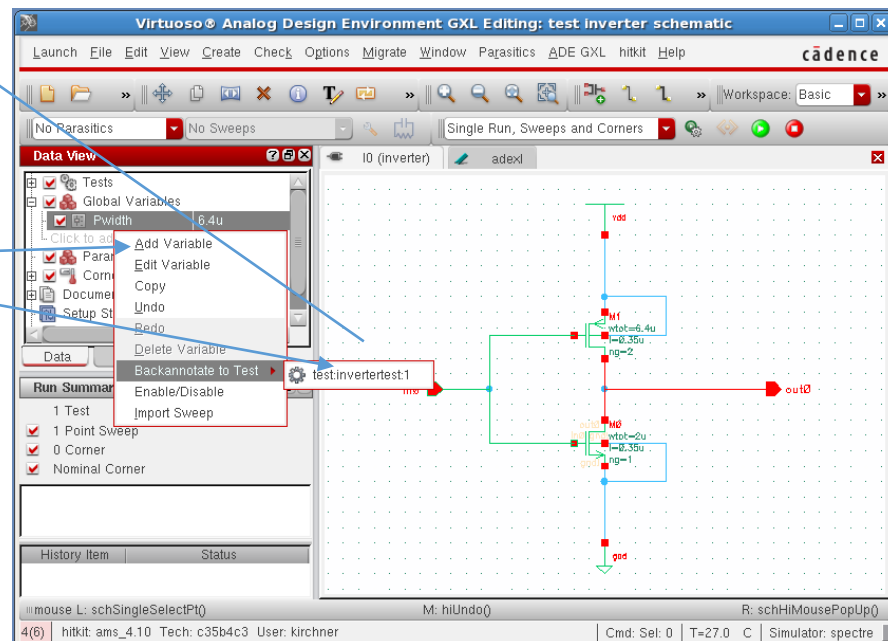


Start here to create a global variable

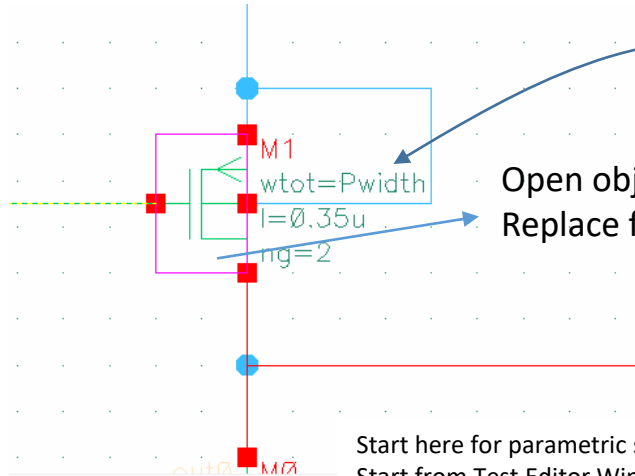


If there is only the testbench schematic open, select inverter and press "E" (descend edit) to open the inverter schematic!

Or start here to create a global variable.
It must be exported/backannotated to appear in test.

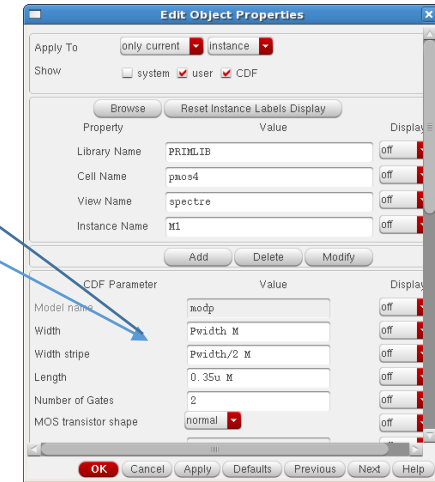


Simulation Parametric Analysis – Global Variables



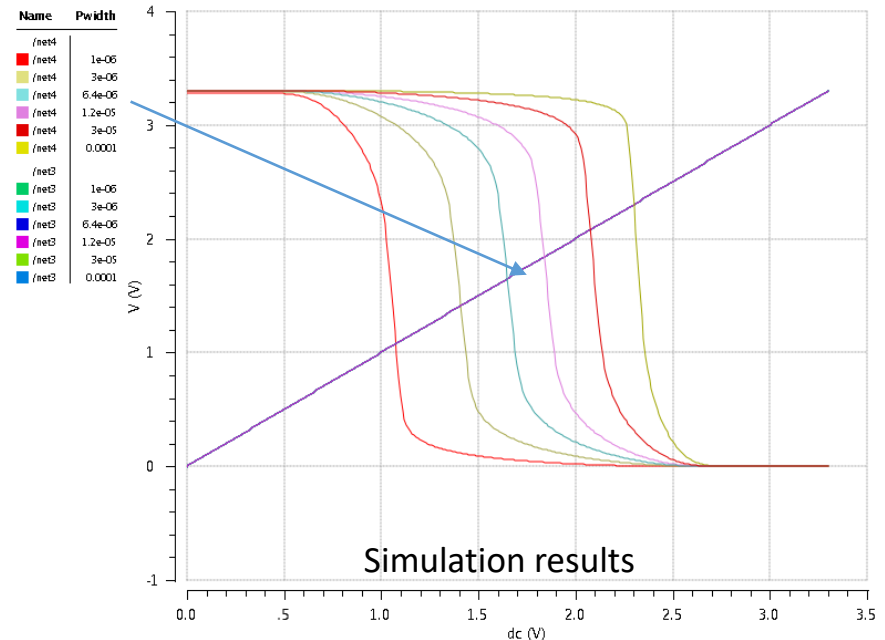
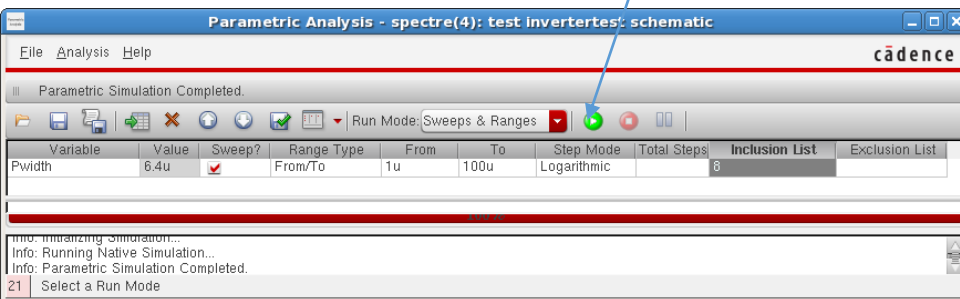
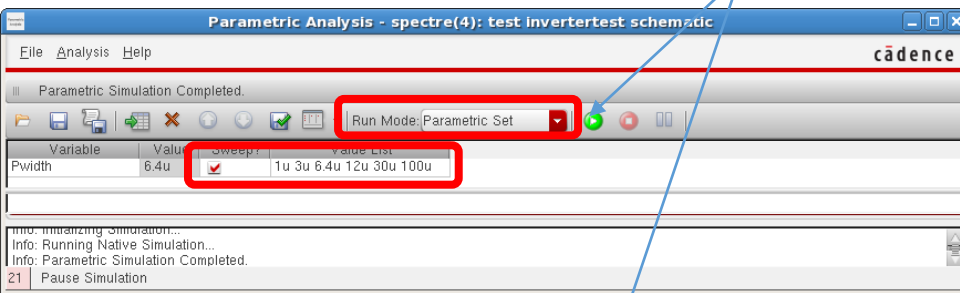
Open object parameters (q)!

Replace fixed value by parameter!



Start here for parametric simulation!

Start from Test Editor Window runs without parametric variation (Default values used).



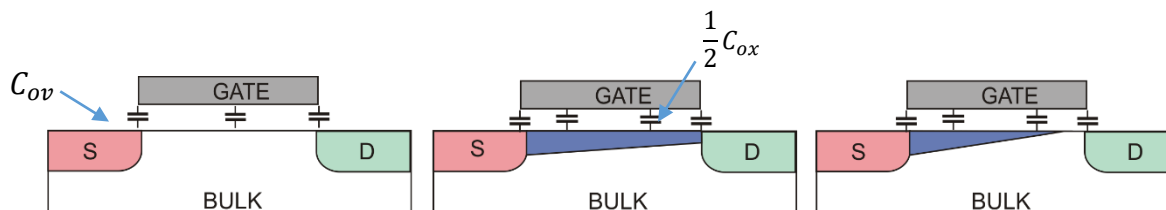
CMOS Inverter Capacitances and Delay

$$C_{in} = \frac{3}{2} (C_{ox1} + C_{ox2})$$

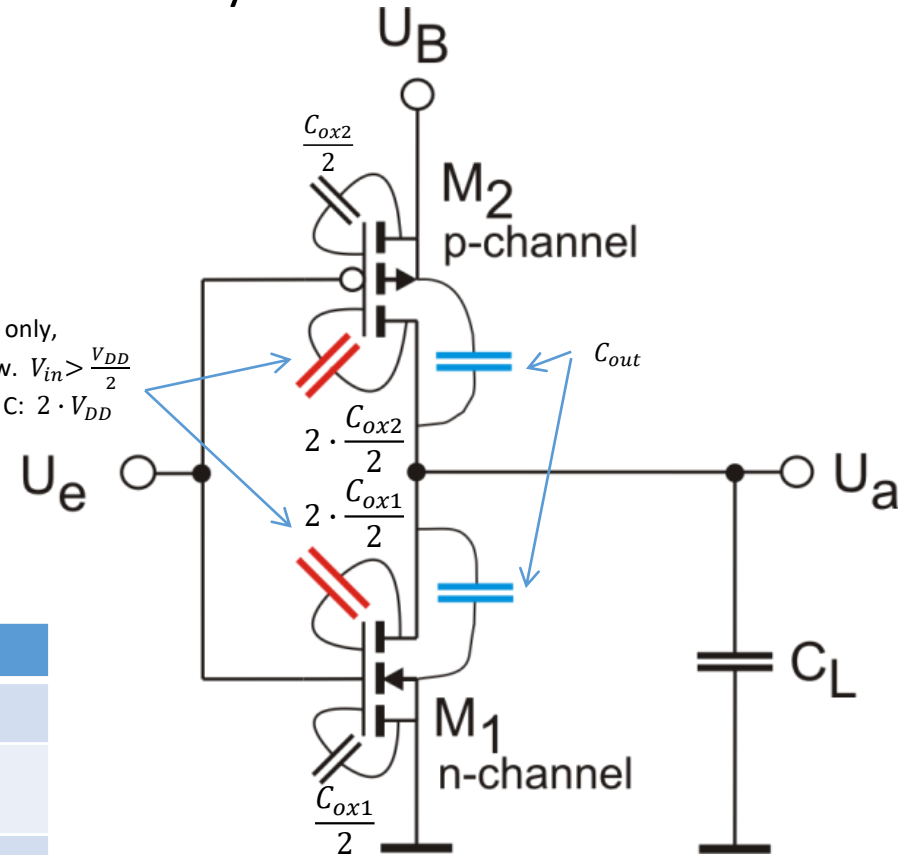
Reale Verhältnisse wesentlich komplizierter:
Gate Capacitances zu Drain, Source, Channel, Bulk ->
additional $C_{overlap}$

C_{in} nonlinear:

Region	C_{GB}	C_{GS}	C_{GD}	C_{in}
off	C_{ox}	0	0	$C_{ox} + 2 \cdot C_{ov}$
NPO	0	$\frac{1}{2} \cdot C_{ox}$	$\frac{1}{2} \cdot C_{ox}$	$C_{ox} + 2 \cdot C_{ov}$
PO	0	$\rightarrow \frac{2}{3} \cdot C_{ox}$	$\rightarrow 0$	$\frac{2}{3} \cdot C_{ox} + 2 \cdot C_{ov}$



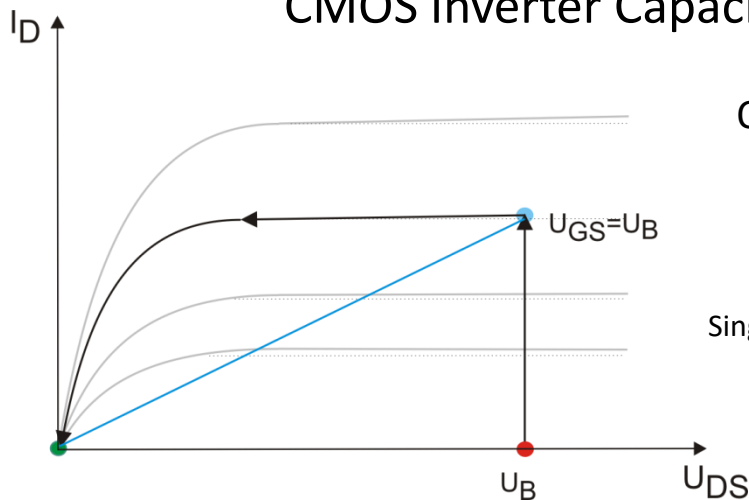
Miller-Capacitor
When will it work? -> only,
if $V_{in} > V_{SP}$, bzw. $V_{in} > \frac{V_{DD}}{2}$
Voltage change over C: $2 \cdot V_{DD}$



$$C_{out} \approx (C_{ox1} + C_{ox2})$$

Originally the junction capacitance
between drain and bulk
In the range of C_{ox} if source and bulk
are interconnected
Nonlinear $\sim \frac{1}{\sqrt{V}}$

CMOS Inverter Capacitances, Output Resistance and Delay



Output resistance of FET for charge reversal

Single transistor at V_{DD} with input voltage at V_{DD}

$$I_D = \frac{\beta_n}{2} (V_{DD} - V_{thn})^2 = \frac{KPNW}{2L} (V_{DD} - V_{thn})^2 = \frac{170 \mu A}{2} \cdot \frac{1 \mu m}{0.35 \mu m} \cdot (3.3V - 0.5V)^2 = 0.68 \text{ mA}$$

$$R_n = R_p = \frac{V_{DD}}{I_D} = \frac{3.3V}{0.68 \text{ mA}} = 4.85 \text{ k}\Omega$$

Kapazität und Zeitkonstante -> Delay time (50%-Schwelle)

$$C_{in} = \frac{3}{2} W \cdot L \cdot C'_{ox}$$

$$C_{out} = W \cdot L \cdot C'_{ox}$$

next gate
(+ wire capacitances)

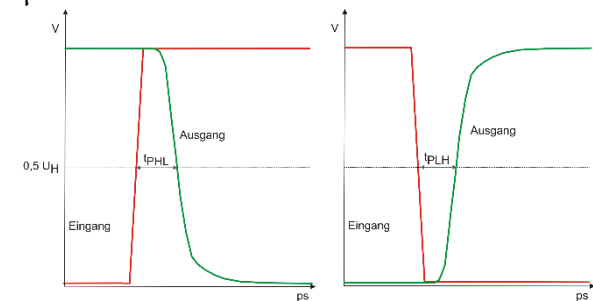
$$t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot (C_{inn} + C_{inp} + C_{outn} + C_{outp})$$

$$t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot C'_{ox} \cdot \frac{5}{2} (W_n L_n + W_p L_p)$$

$$t_{pHL} = t_{pLH} = 0.7 \cdot 4.85 \text{ k}\Omega \cdot 4.5 \frac{\text{fF}}{\mu\text{m}^2} \cdot \frac{5}{2} (1 + 3.2) \mu\text{m}^2 = 160 \text{ ps}$$

$$C_{in} = 4.5 \frac{\text{fF}}{\mu\text{m}^2} \cdot \frac{3}{2} (1 + 3.2) \mu\text{m}^2 = 28.35 \text{ fF}$$

$$C_{out} = 4.5 \frac{\text{fF}}{\mu\text{m}^2} \cdot (1 + 3.2) \mu\text{m}^2 = 18.9 \text{ fF}$$



Simulation Transient Analysis

Replace the vdc-source by a vpulse-source. (It would be possible to use this from the scratch even for dc-simulation!)

Add Instance

Library: analogLib
Cell: vpulse
View: symbol
Names:

☒ Add Wire Stubs at:
☐ all terminals ☒ registered terminals only

Array: Rows: 1 Columns: 1

Rotate Sideways Upside Down

Frequency name for 1/period:
Noise file name:
Number of noise/freq pairs: 0
DC voltage: 1.65 V
AC magnitude:
AC phase:
XF magnitude:
PAC magnitude:
PAC phase:
Voltage 1: 0 V
Voltage 2: 3.3 V
Period: 2n s
Delay time: 1n s
Rise time: 50p s
Fall time: 50p s
Pulse width: 1n s
Temperature coefficient 1:
Temperature coefficient 2:
Nominal temperature:
Type of rising & falling edge:

Hide Cancel Defaults Help

Period

Pulse width

Voltage2

Voltage1

Delay

Rise time

Fall time

t=0

Try another parametric simulation (transient) with Load Capacitance as a parameter!

Choosing Analyses -- Virtuoso® Analog Design

Analysis: ☒ tran ☐ dc ☐ ac ☐ noise
☐ xf ☐ sens ☐ dcmatch ☐ stb
☐ pz ☐ sp ☐ envlp ☐ pss
☐ pac ☐ pstb ☐ pnoise ☐ pxf
☐ psp ☐ qpss ☐ qpac ☐ qpnoise
☐ qpxf ☐ qpsp ☐ hb ☐ hbac
☐ hbnoise

Transient Analysis

Stop Time:

Accuracy Defaults (errpreset)
☒ conservative ☐ moderate ☐ liberal

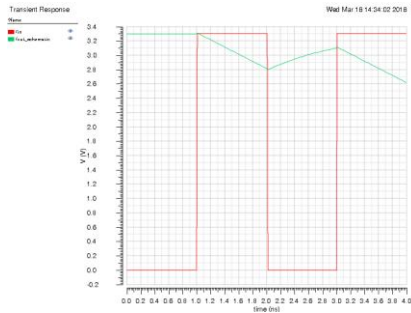
☐ Transient Noise
☐ Dynamic Parameter

Enabled ☒ Options...

OK Cancel Defaults Apply Help

How to find proper time values?

Simulation Transient Analysis

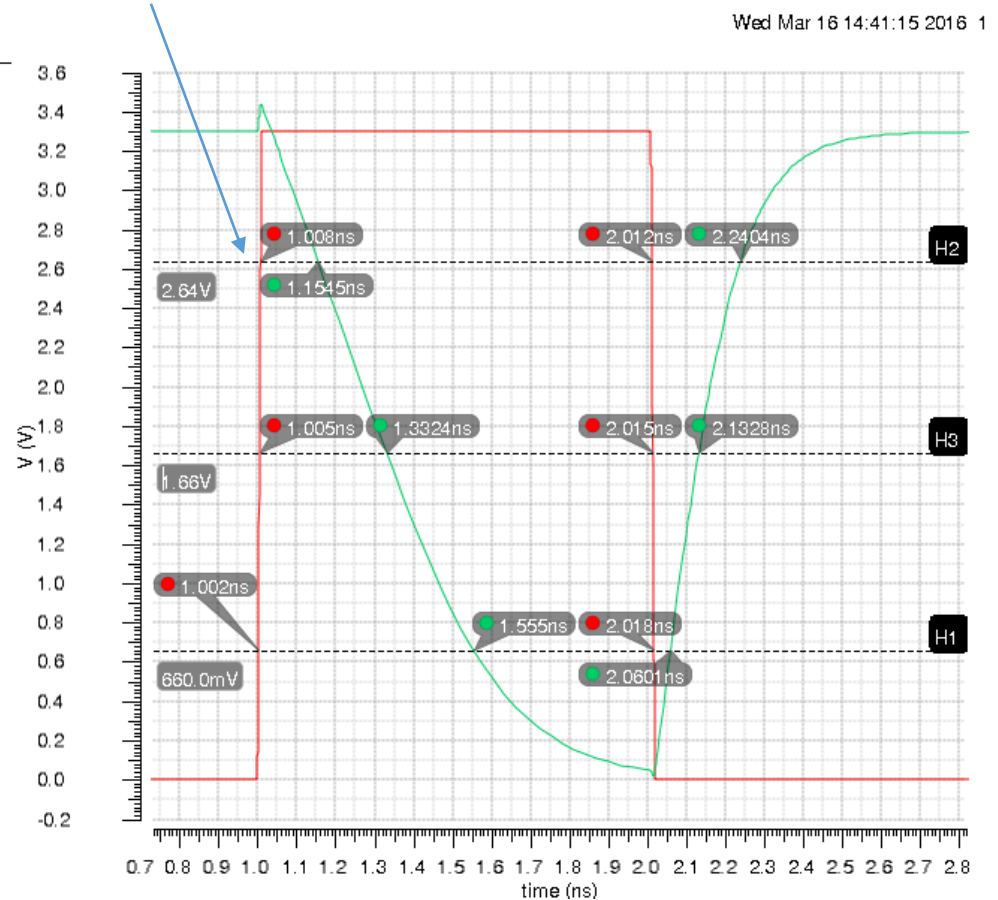


Oops!, looks strange ...
1pF load is too much for our small gate

Changed load to 80 fF
Compare with data sheet of
ams standard cell next page!

falltime: $1.555\text{ns} - 1.1545\text{ns} = 400\text{ ps}$
 risetime: $2.2404\text{ns} - 2.0601\text{ns} = 180\text{ ps}$
 delay(inp rise): $1.3324\text{ns} - 1.005\text{ns} = 327\text{ ps}$
 delay(inp fall): $2.1328\text{ns} - 2.015\text{ns} = 118\text{ ps}$

Zur Anzeige der Schnittpunkte: RM auf Markerlinie -> Intercepts -> On



Simulation Transient Analysis

Try another parametric simulation with
Load Capacitance as a parameter!
Compare results with a given cell from AMS!



INV0



Databook Build Date: Wednesday Jun 18 17:26 2014

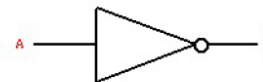
Copyright © 2004-2013 Nangate Inc.

Conditions for characterization library c35_CORELIB_TYP, corner c35_CORELIB_TYP_typical: Vdd= 3.30V, Tj= 25.0 deg. C.

Output transition is defined from 20% to 80% (rising) and from 80% to 20% (falling) output voltage.

Propagation delay is measured from 50% (input rise) or 50% (input fall) to 50% (output rise) or 50% (output fall).

Cell Area	36.400 um ²
Equation	Q = "IA"
Type	Combinational
Input	A
Output	Q



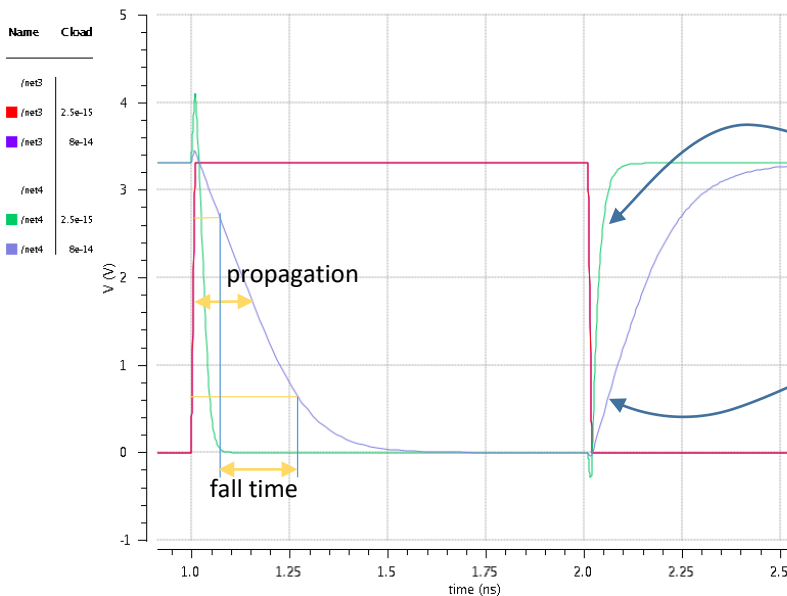
A	Q
L	H
H	L

		Propagation Delay [ns]			
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	0.05	0.53	-0.20	1.07
	rise	0.08	0.94	0.86	2.24

		Output Transition [ns]			
		0.01		4.00	
Input Transition [ns]					
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	0.05	0.71	0.56	1.48
	rise	0.10	1.39	0.54	1.87

Capacitance [fF]	Leakage [pW]
A	3.8210
	0.21

Dynamic Power Consumption [nW/MHz]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	5.98	6.28	160.14	131.01
	rise	34.83	35.09	256.12	205.46



Uups!, explain the negative value!

Layout Start and Generate from Schematic

Replace all the global variables in the design with fixed values.

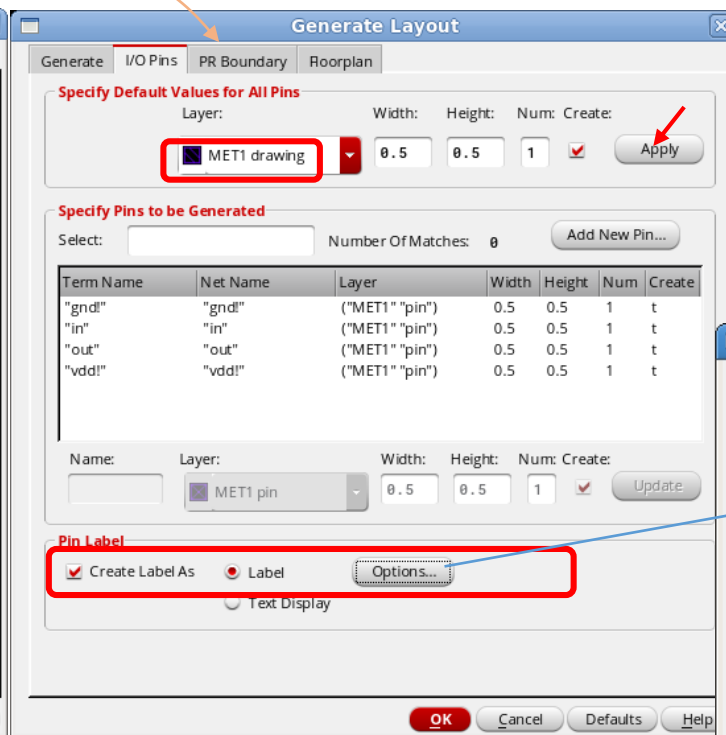
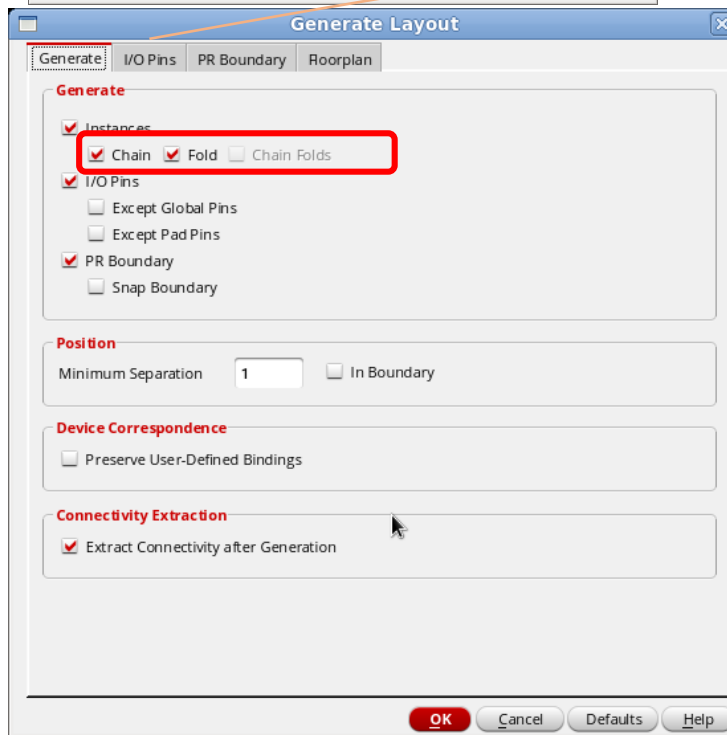
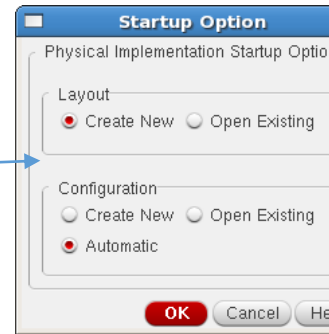
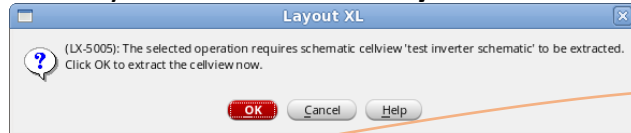
Fold the PMOS (2 gates)

Global variables have their scope in simulation only.

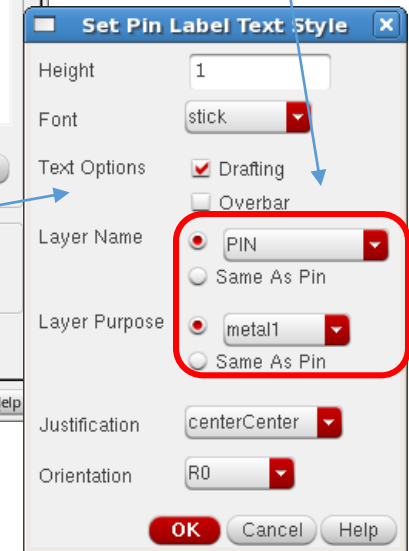
Global Variables in the testbench are not affected, because they will not be involved in the layout.

In Schematic Editor: **Launch -> Layout XL**

In Layout XL: **Connectivity -> Generate -> All From Source**



Text is used to recognize ports correctly.



Generates a layout with all instances placed outside a rectangle (estimated cell boundary)

Layout Floorplaning

To see all layers: Options -> Display -> Display Levels -> Set "stop" to 32 (Shift-f) Save to ~/.cdsenv

Suggested cell area

20µm x 6 µm cell

Edit -> Stretch
Tools-> Create Measurement*

RM ->
(De)Select Under Cursor
Routing Object Granularity
Make PR Boundary Non-Selectable

Tools -> Clear All Measurements*m
Create -> Shape -> Rectangle

Point 0,0

When moving pins include all parts.
Best practice: Snap to the little "+"!

F3 opens move options (e.g. orthogonal, all angels etc.)
(F3 opens options for all commands)

***Ruler in older versions**

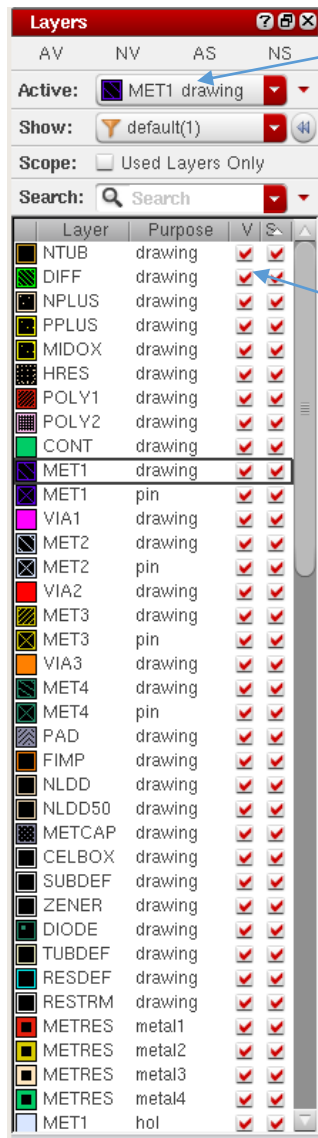
Don't have Bulk ?

Delete both transistors in layout.

Open schematic and change transistor property there (add substrate contact).

In Layout XL use Connectivity -> Update Components and Nets.

Layout Edit



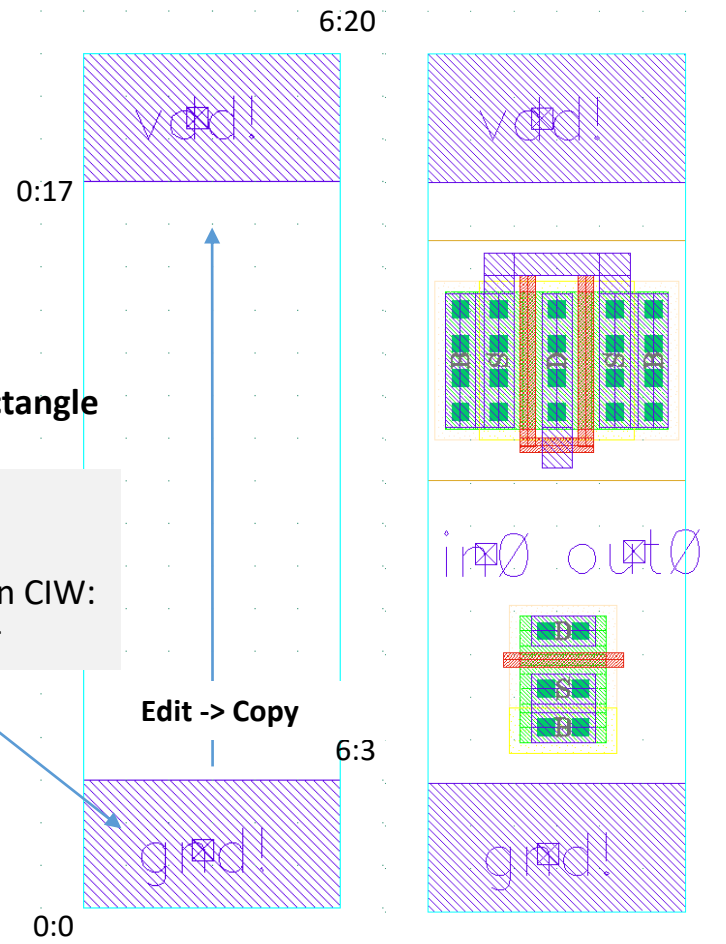
actual layer

visible/selectable

Create -> Shape -> Rectangle

First corner 0:0
Opposite Corner 6:3
Input with mouse or in CIW:
0:0 enter -> 6:3 enter

Edit -> Copy



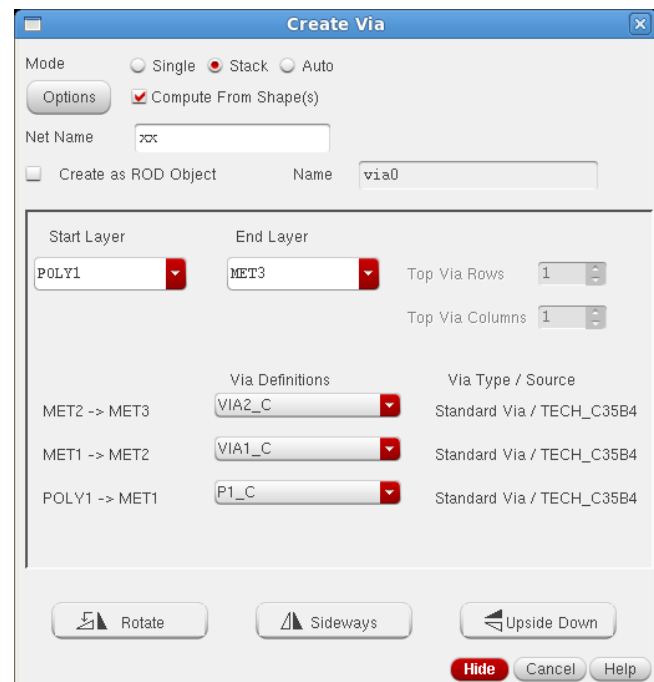
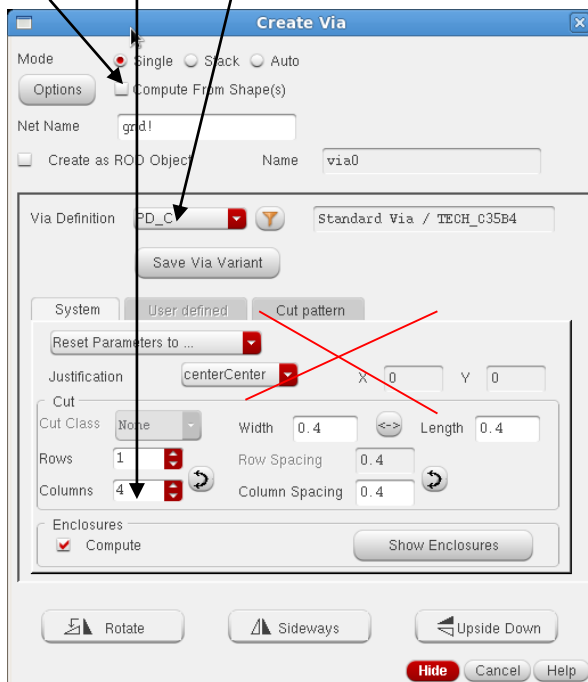
Layout - VIAs

Creating VIAs:

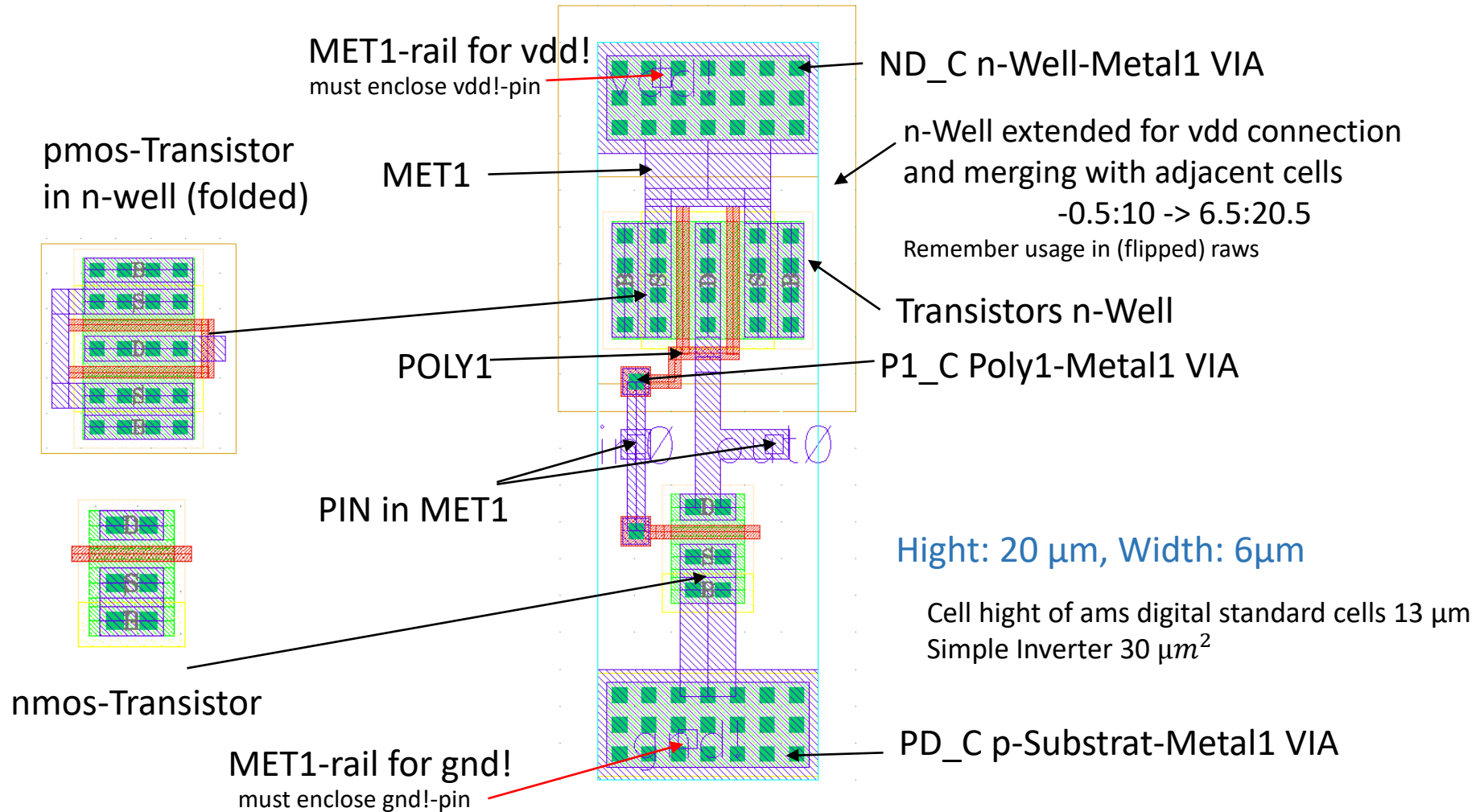
PD_C : p-Substrat-Metal1
 ND_C : n-Well-Metal1
 P1_C : Poly1-Metal1
 P2_C : Poly2-Metal1
 VIA1_C : Metal1-Metal2
 VIA2_C : Metal2-Metal3
 VIA3_C : Metal3-Metal4

Make them for the power stripes before routing of wires.

Layout of single contact predefined. **Do not change!**
 Number and alignment variable. Using "**Compute from Shape(s)**" fills area with appropriate number of contacts.



Cell Layout



To consider (design rules):

Poly1: width $\geq 0.35\mu$, space $\geq 0.45\mu$

Metal1: width $\geq 0.5\mu$, space $\geq 0.45\mu$

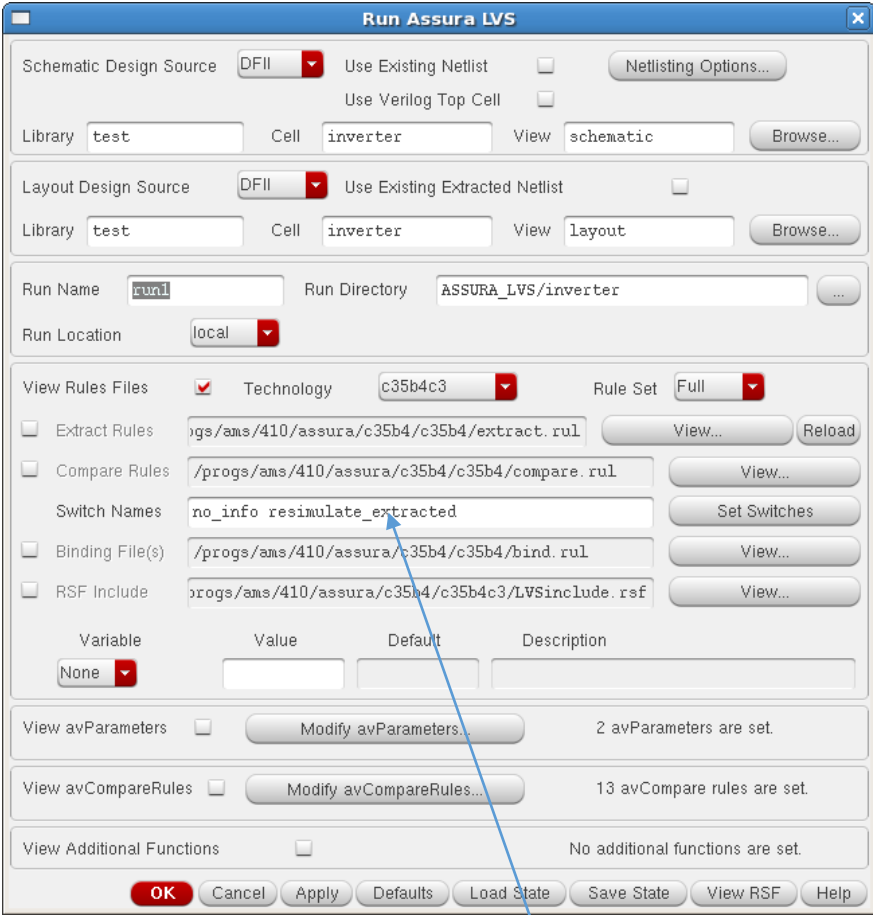
Metal2: width $\geq 0.6\mu$, space $\geq 0.5\mu$

gnd! -> Exclamation mark: global signal

Cadence Layout - LVS

Compare Layout Versus Schematic

Assura -> Run LVS

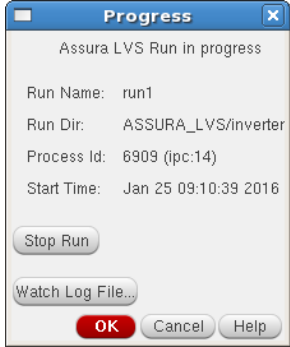


The 'Run Assura LVS' dialog box is shown with various configuration options. A blue arrow points from the 'no_info resimulate_extracted' text in the 'Switch Names' field to a text box at the bottom of the slide.

Run Assura LVS

Schematic Design Source: DFII (selected), Use Existing Netlist (unchecked), Netlisting Options...
Library: test, Cell: inverter, View: schematic, Browse...
Layout Design Source: DFII (selected), Use Existing Extracted Netlist (unchecked)
Library: test, Cell: inverter, View: layout, Browse...
Run Name: run1, Run Directory: ASSURA_LVS/inverter, Run Location: local (selected)
View Rules Files: ☒ Technology: c35b4c3 (selected), Rule Set: Full (selected)
Extract Rules: /progs/ams/410/assura/c35b4/c35b4/extract.rul, View..., Reload
Compare Rules: /progs/ams/410/assura/c35b4/c35b4/compare.rul, View...
Switch Names: no_info resimulate_extracted, Set Switches
Binding File(s): /progs/ams/410/assura/c35b4/c35b4/bind.rul, View...
RSF Include: /progs/ams/410/assura/c35b4/c35b4c3/LVSinclude.rsf, View...
Variable: None (selected), Value: , Default: , Description:
View avParameters: ☐ Modify avParameters... 2 avParameters are set.
View avCompareRules: ☐ Modify avCompareRules... 13 avCompare rules are set.
View Additional Functions: ☐ No additional functions are set.
Buttons: OK, Cancel, Apply, Defaults, Load State, Save State, View RSF, Help

Necessary for QRC parasitic extraction



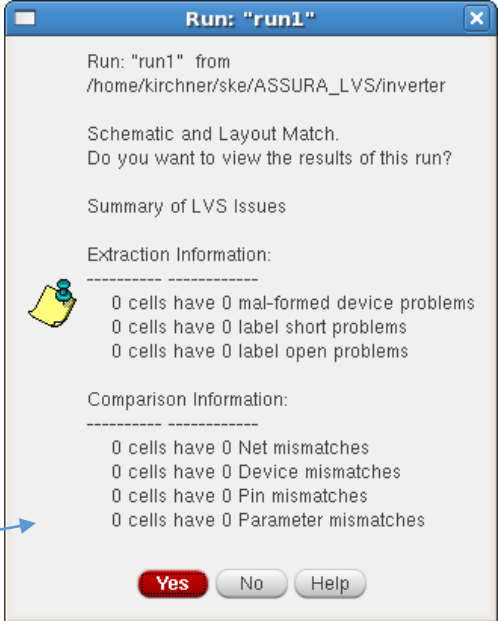
The 'Progress' dialog box shows the status of the LVS run. A blue arrow points from the 'OK' button to the 'Run: "run1"' dialog box.

Progress

Assura LVS Run in progress

Run Name: run1
Run Dir: ASSURA_LVS/inverter
Process Id: 6909 (ipc:14)
Start Time: Jan 25 09:10:39 2016
Buttons: Stop Run, Watch Log File..., OK, Cancel, Help

wait!



The 'Run: "run1"' dialog box displays the results of the LVS run. A blue arrow points from the 'wait!' text to this dialog box.

Run: "run1" from /home/kirchner/ske/ASSURA_LVS/inverter

Schematic and Layout Match.
Do you want to view the results of this run?

Summary of LVS Issues

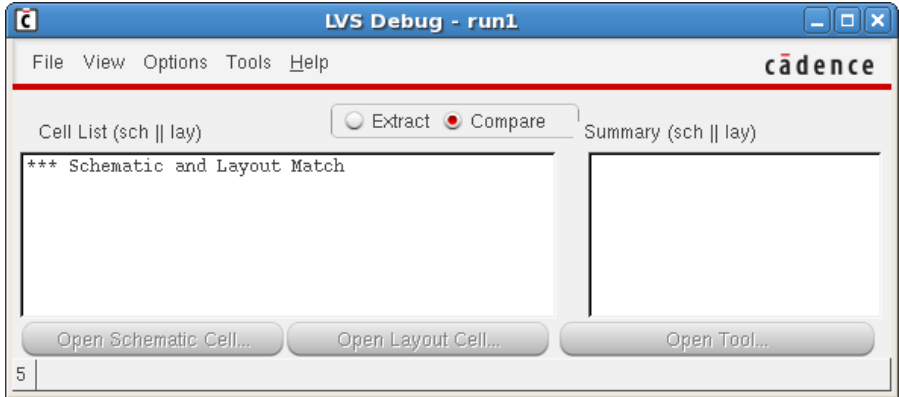
Extraction Information:

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

Comparison Information:

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

Buttons: Yes, No, Help



The 'LVS Debug - run1' window shows the results of the LVS run. A blue arrow points from the 'OK' button in the 'Progress' dialog box to this window.

LVS Debug - run1

File View Options Tools Help

Cell List (sch || lay) ☐ Extract ☒ Compare Summary (sch || lay)

*** Schematic and Layout Match

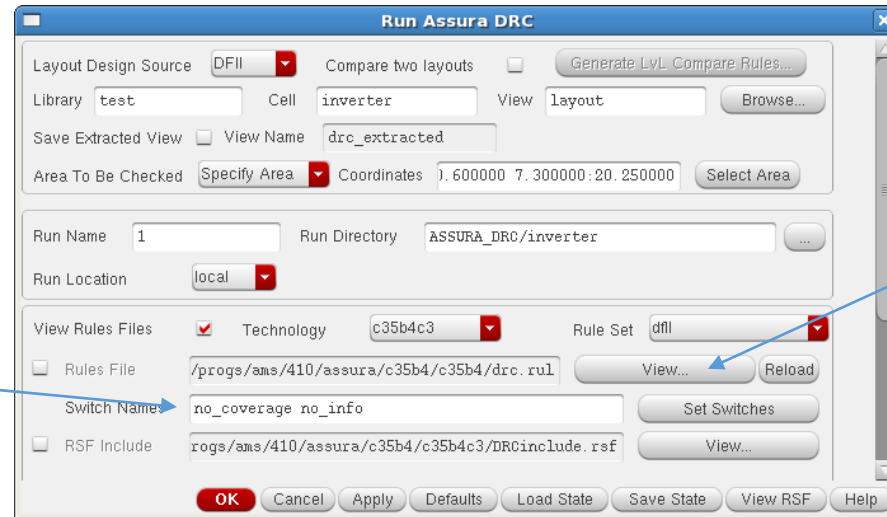
Buttons: Open Schematic Cell..., Open Layout Cell..., Open Tool...

That's what we want to see!

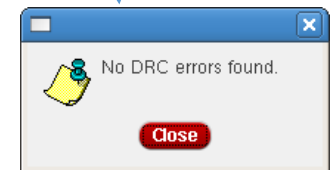
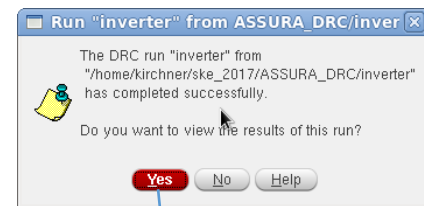
Cadence Layout - DRC

Assura -> Run DRC

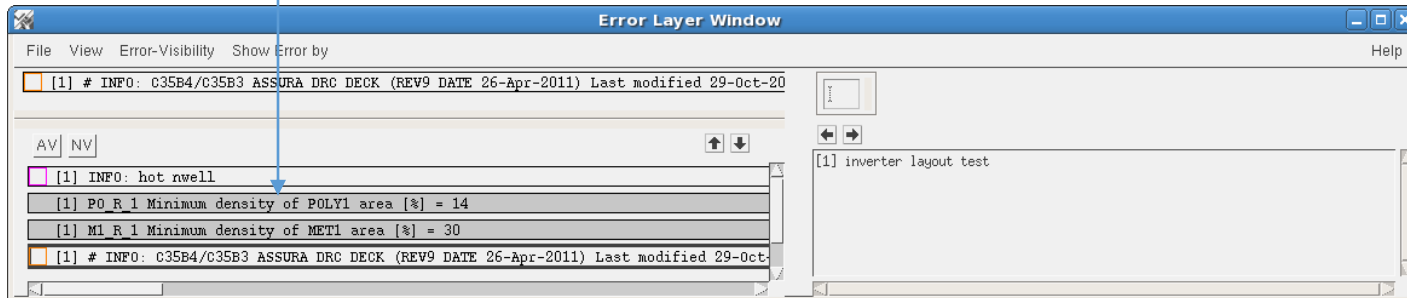
Set these switches to avoid some messages (see below!).
What does "Coverage" mean?



Here you may open the rule set file for information. Contains all the rules like distances, overlap, min. width et cetera.



That's what we would like to see!



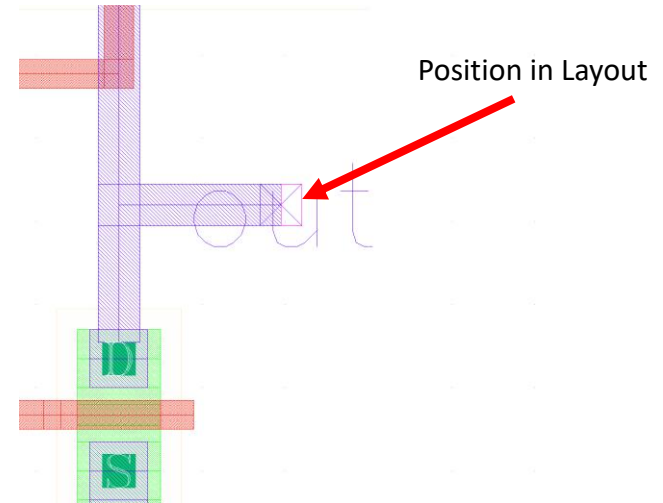
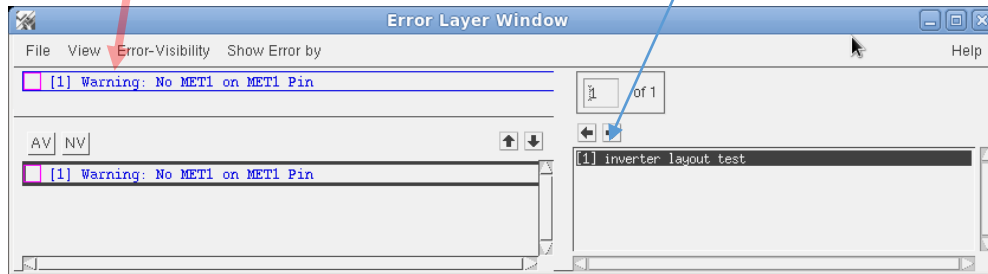
Cadence Layout – DRC with Errors remaining

Example for an Error Message:

Here: Pin is not fully covered by metal

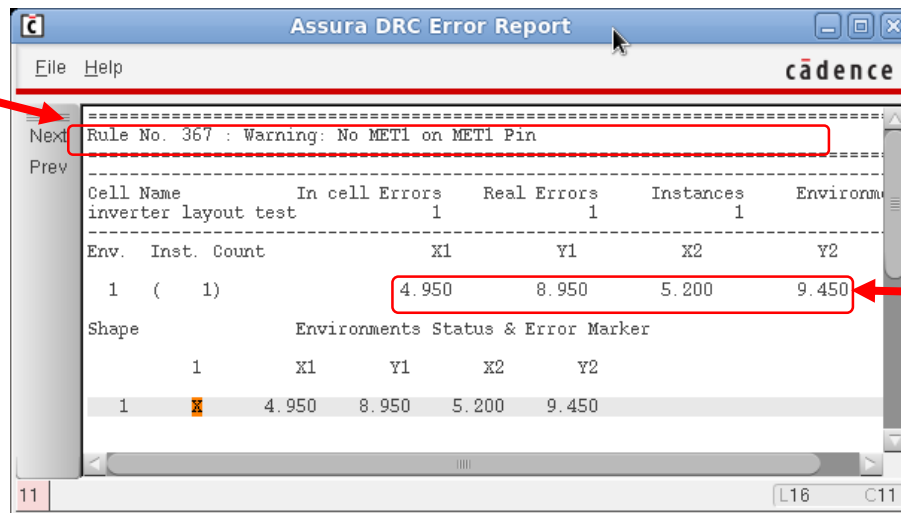
Violated Rule

Browse Errors (if multiple)



View -> Error Report

Violated Rule



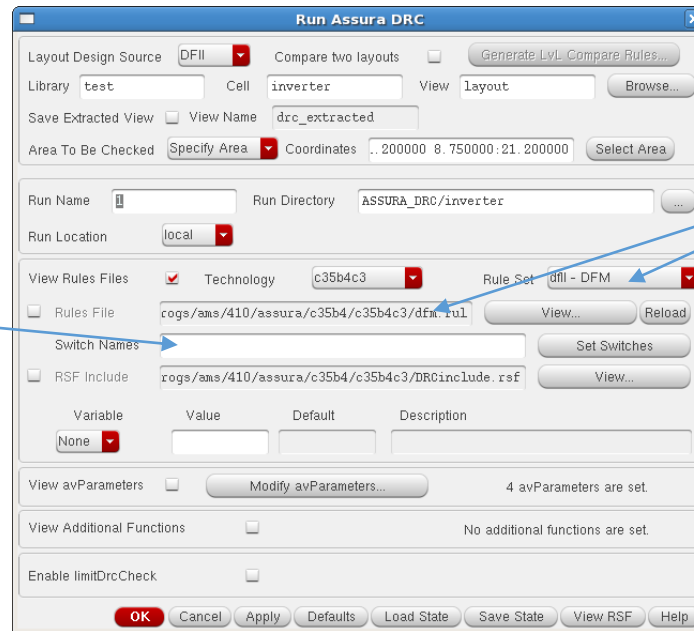
Position in Layout

Solutions:

Extend wire to the right or
add a rectangle in MET1 covering the Pin

Cadence Layout - DFM

Assura -> Run DRC

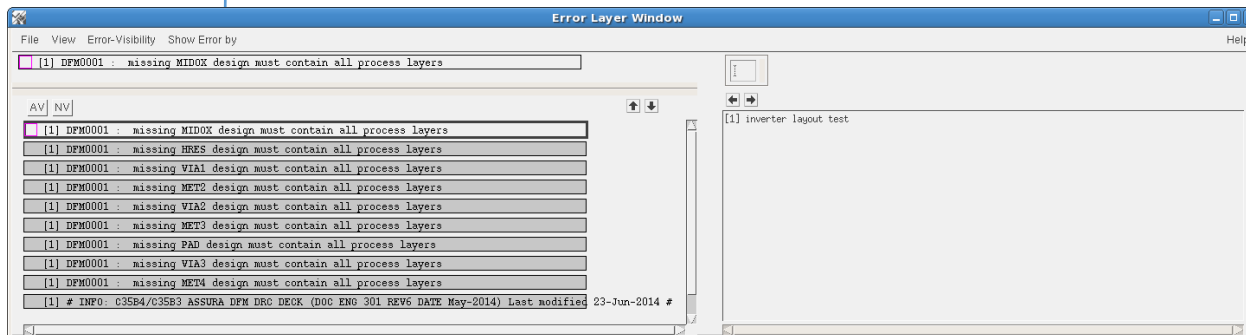


Extended ruleset:
Rules for manufacturing ->

Coverage of all but upper metal
layer et cetera.

no switches!

Errors because we did not use
some layers.
Interesting for a top layout.

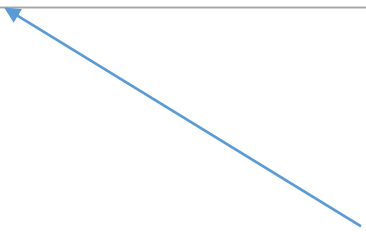


Cadence Layout - ERC

Electrical rule check is included in DRC.

There is no separate rule check in the ams-HITkit.

Starting ERC with Assura -> Run ERC opens a form similar to DRC with no technology selected and either rule files.



Up to now no verification for this.
Separate ERC-usage found nowhere.

Cadence Layout – QRC – Parametric Extraction

QRC -> Run Assura Quantus -QRC

no changes

Technology: c35b4c3 RuleSet: Typical

Output: Extracted View Lib: test Cell: inverter View: av_extracted

Parasitic Res Component: presistor auLvs PRIMLI Prop Id: r

Parasitic Cap Component: pcapacitor auLvs PRIMLI Prop Id: c

Parasitic Ind Component: pinductor auLvs PRIMLI Prop Id: l

Parasitic M Component: pmind auLvs PRIMLIB Prop Id: k

Inductance L1 Prop Id: ind1 Inductance L2 Prop Id: ind2

Substrate Extract: ☒ Extract MOS Diffusion Res: ☒

Extract MOS Diffusion AP: ☐ Add LVS MOS Diffusion Res: ☐

Substrate Profile: NONE Extract MOS Diffusion High: NONE

Library Prefix:

Library Directory:

Library Directory: Specify a directory for writing local libraries created during the hierarchical extraction of an extracted view.

OK Cancel Defaults Apply Load State Save State View Command File Help

Extraction Type: RC Name Space: Schematic Names

Max fracture length: infinite microns Temperature: 25.0 C

Cap Coupling Mode: Coupled Ref Node: gnd!!

Mult Factor: 1.0 Diffusion Equation R: ☒

PEEC Mode: ☐ Ladder Network: ☐ Global Frequency: MHz

Net Selection Type: Full Chip All Nets QRCFS Extraction Mode: NONE

Layer Setup Customization: ☐ Edit... Exclude Via Capacitance: ☐

Resistance Mesh: ☐ Edit... QRCFS High: ☐

From File: ☐ SelfFromSch: ☐ SelfFromLay: ☐

Litho Config File: ☐ View Edit

Contour Directory: ☐ View Edit

Enable QRCY: ☐ Split Ring: ☐ Split Ring Distance: 5 Microns

Progress Form: QRC Run in progress

Run Name: run1

Run Dir: /home/kirchner/ske/ASSURA_LVS/inverter

Process Id: 6897 (ipc:16)

Start Time: Jan 22 11:11:15 2016

OK Stop Run Watch Log File...

RC

Coupled C: net to net (signals)

Decoupled C: net to power and ground only

use gnd! or vcc!

wait!

The QRC run "run1" completed successfully. The output is in:

Library: test

Cell: inverter

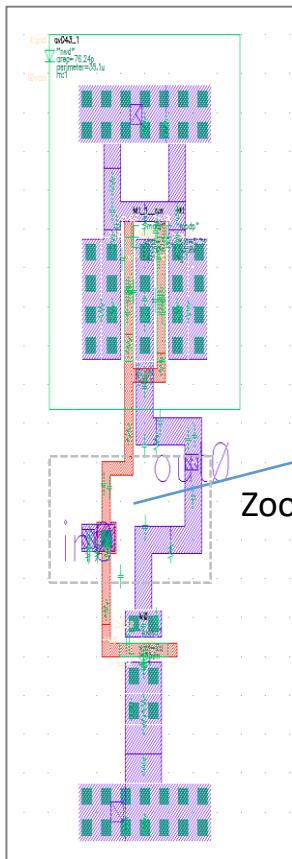
View: av_extracted

Close

Cadence – QRC – Extracted view

Open View "av_extracted" in Library Manager

Launch -> Plugins -> Parasitics : New Tab "Parasitics"
Parasitics -> Setup Parasitics (gnd! and vdd! as reference nodes)



Zoom

Try also: net to net
terminal to terminal (r)

In Schematic or av_extracted view:
Launch -> Parasitics : New Tab "Parasitics"
Parasitics -> Report Parasitics -> net : Select with cursor
In Schematic **Parasitics > Show Parasitics : Lumped values**

Viewing parasitics may be interesting.
More important is their use in postlayout simulation.
They will be included in simulation netlists.

Parasitics for net /In0

Display: ☒ R ☒ decoupled C ☒ coupled C ☐ L ☐ K

Instance	Type	Value	From	To
/rg5	R	1.98	/3:in0	/6:in0
/rg4	R	106.6	/6:in0	/8:in0
/rg3	R	51.6	/5:in0	/7:in0
/rg2	R	118.8	/5:in0	/6:in0
/rg1	R	79.89	/4:in0	/5:in0
/re3	R	74.51m	/1:in0	/2:in0
/re2	R	1.932m	/2:in0	/3:in0
/re1	R	1.932m	/in0	/1:in0
/c4	C	13.06a	/5:in0	/out0
/c3	C	70.35a	/7:in0	/6:vdd!
/c2	C	7.958a	/5:in0	/2:out0
/c1	C	552.6a	/5:in0	/gnd!
/c41	C	152.6z	/7:in0	/gnd!
/c40	C	999.2z	/3:in0	/8:vdd!
/c4	C	3.921a	/in0	/8:vdd!
/c37	C	150.6a	/5:in0	/4:gnd!
/c35	C	10.25a	/5:in0	/2:vdd!
/c34	C	72.87z	/5:in0	/1:vdd!

Close Save... Help

pico	10 ⁻¹²
femto	10 ⁻¹⁵
atto	10 ⁻¹⁸
zepto	10 ⁻²¹

Cadence – QRC – Post-Layout Simulation (ADE-L/XL)

Open testbench (schematic)
Copy the inverter and its load.
Save as a new testbench.

In **CIW**:

File -> New -> Cellview

In Schematic Editor:

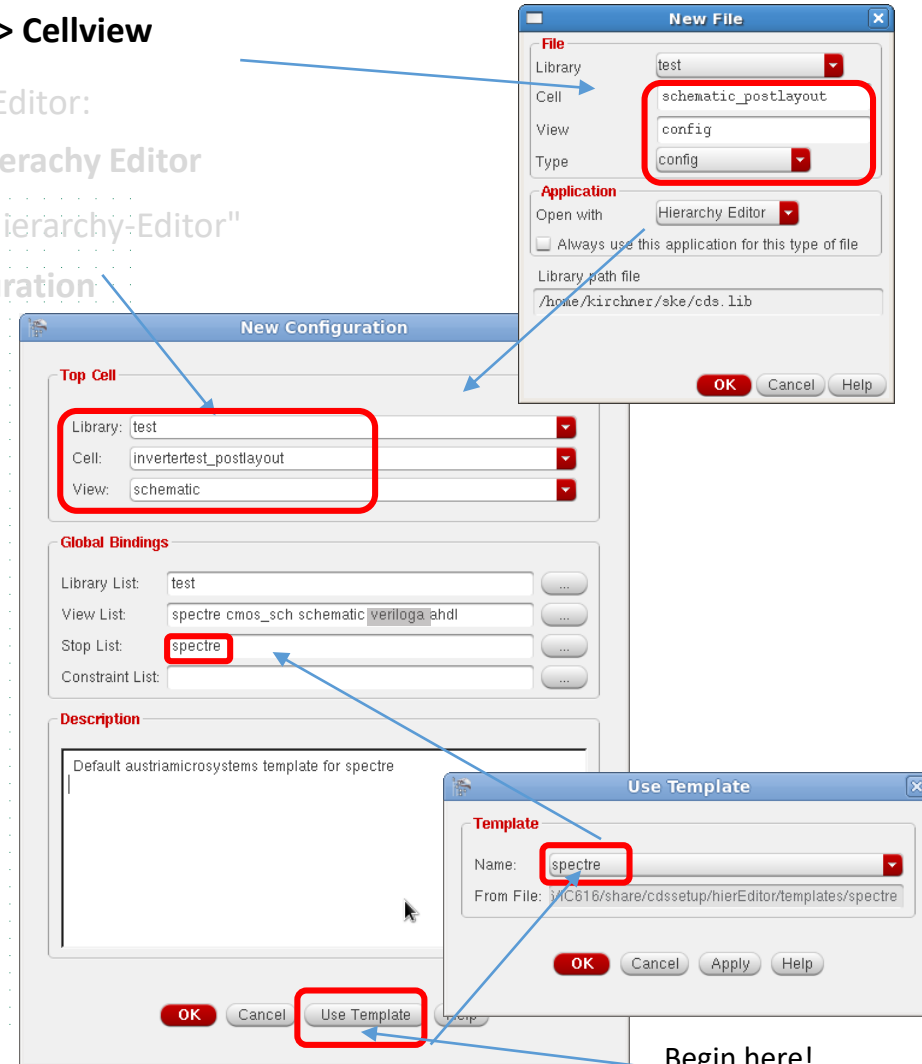
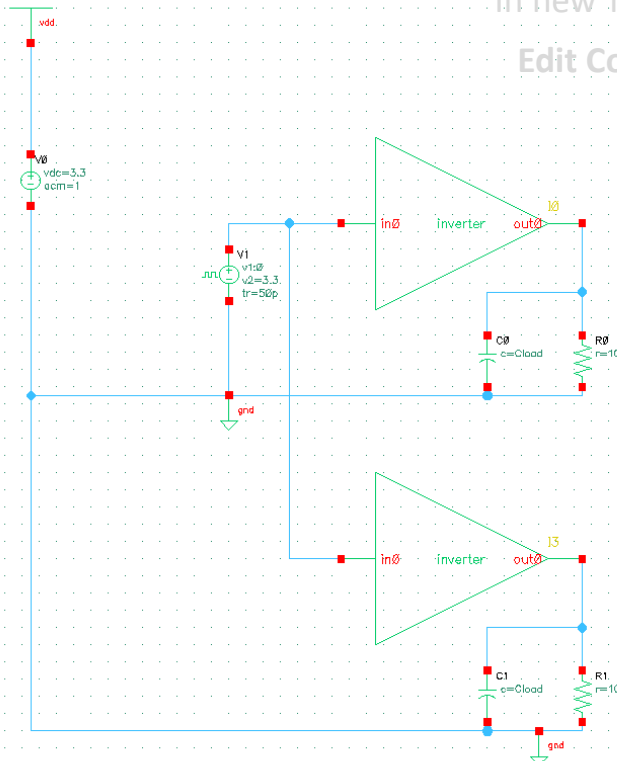
Launch -> Hierarchy Editor

In new Tab "Hierarchy-Editor"

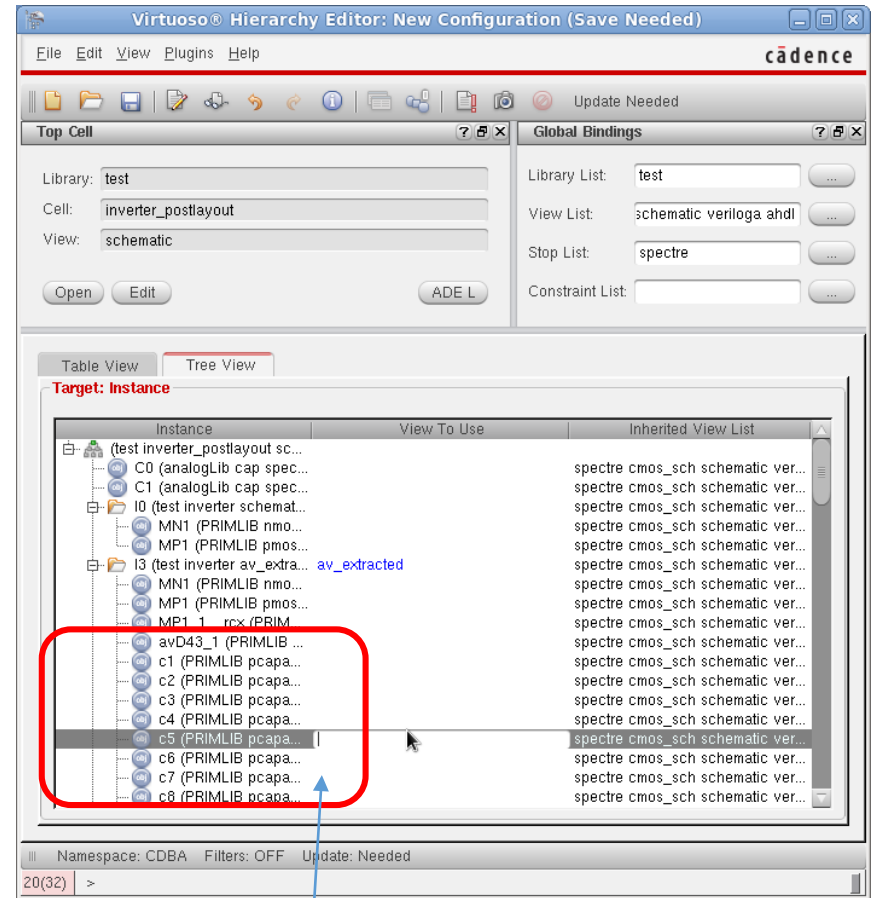
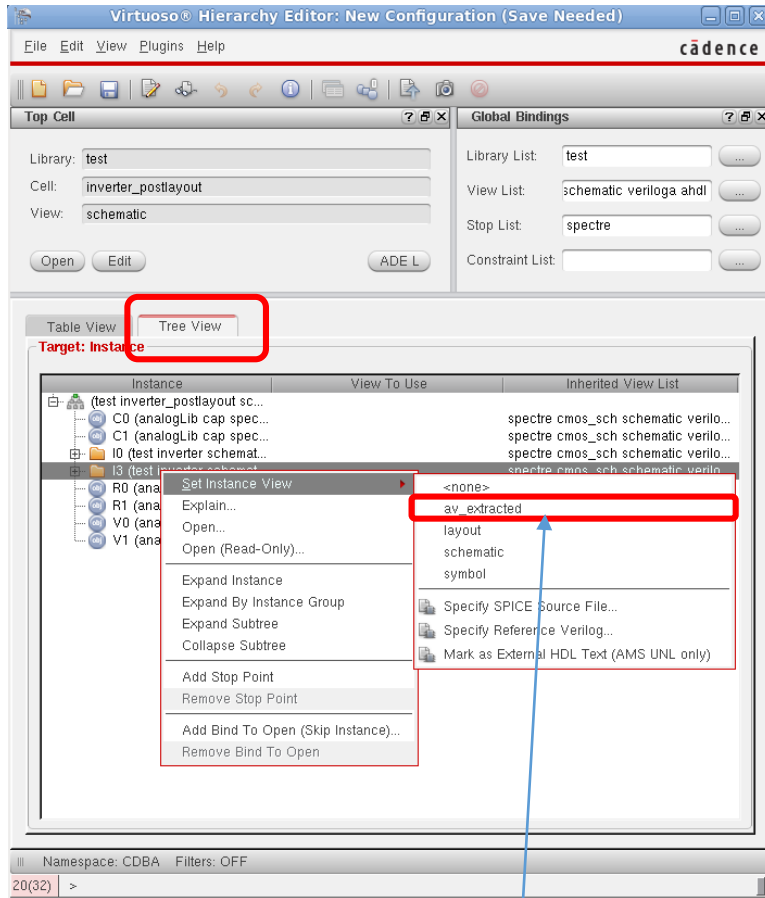
Edit Configuration

We need different models for the UUT (inverter)

- Original schematic
- Netlist with extracted parasitics.



Cadence – Post-Layout Simulation (ADE-L/XL)



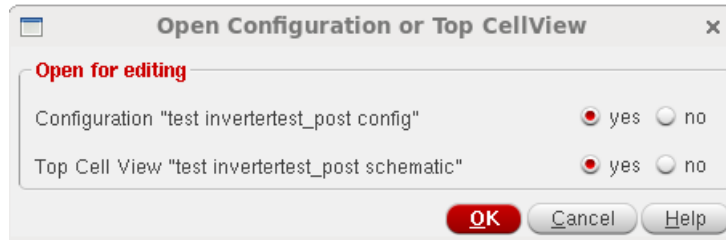
Parasitics

Replace (use RightMouse -> set instance view) schematic by av_extracted

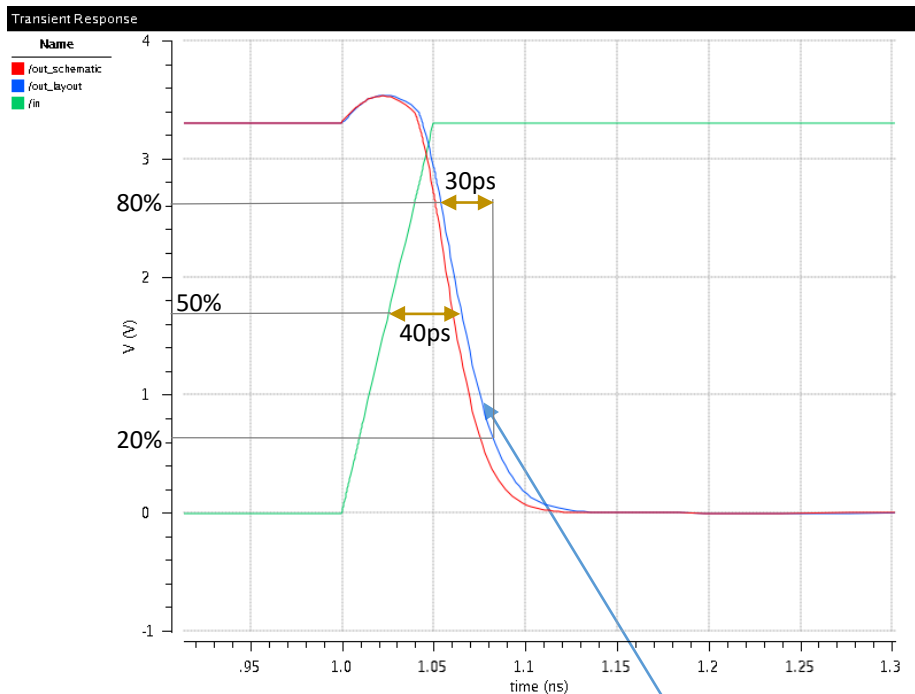
41

Cadence – Post-Layout Simulation - Result

Open the configuration in Library Manager

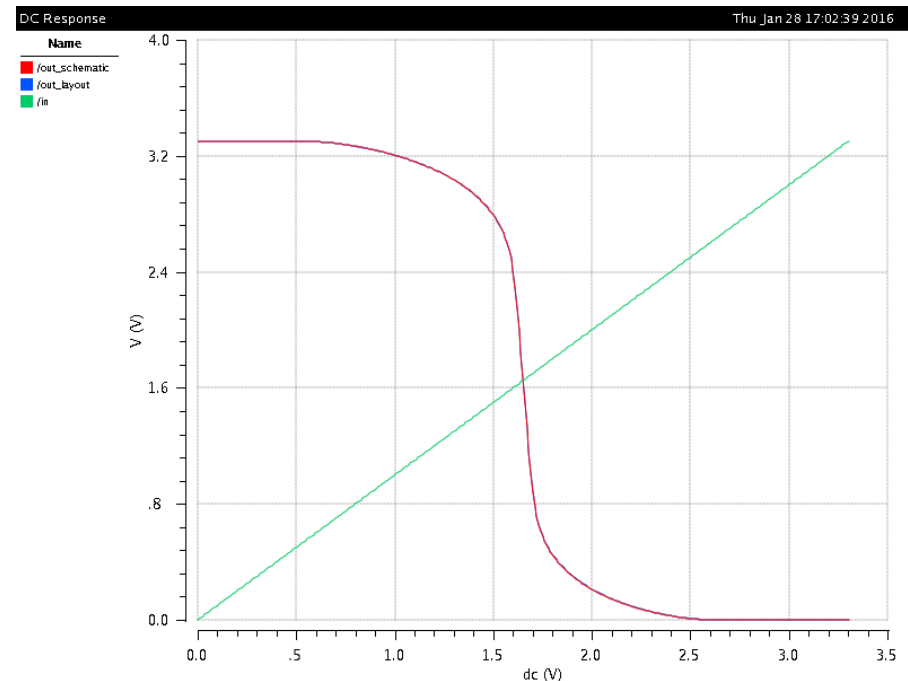


To perform simulation see slides above from "Simulation ADE GXL Start"



OK, delay increased by some ps

Shown for $C_{Load} = 4$ fF. Less difference for higher load.



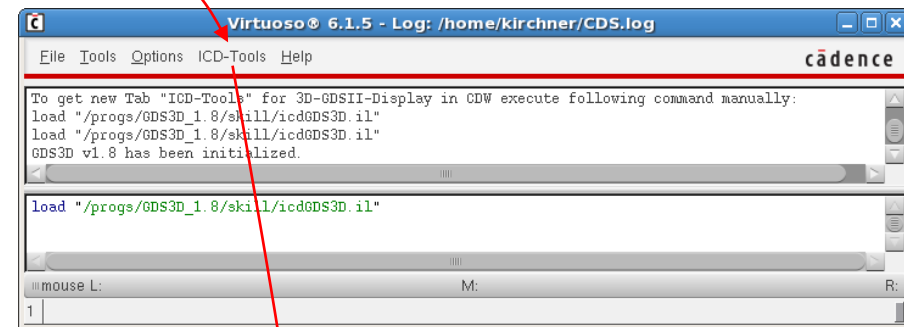
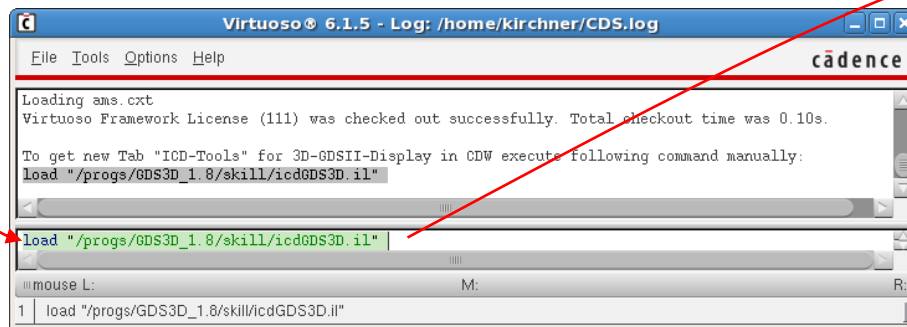
OK, no visible change

Layout 3D View

GDS3D from University of Twente, NL

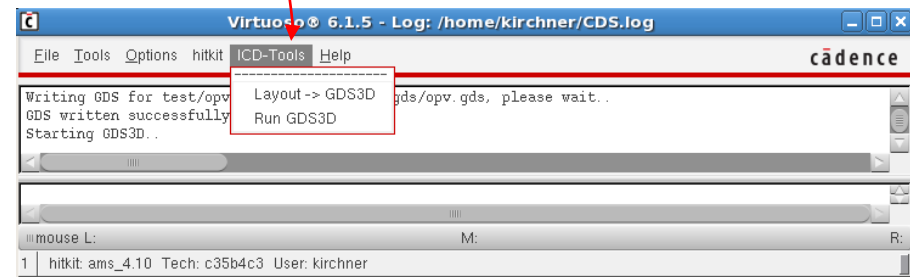
Needs a technology file (layer thickness, pitches). Generated for AMSC35B4 from process parameters.
Needs initialization for Cadence integration, but may be used standalone.

Automatic initialization does not work yet. For manual initialization observe the last output after CIW start.



With a layout opened we can make a GDSII-Stream and run the GDS3D tool. ICD - Tools

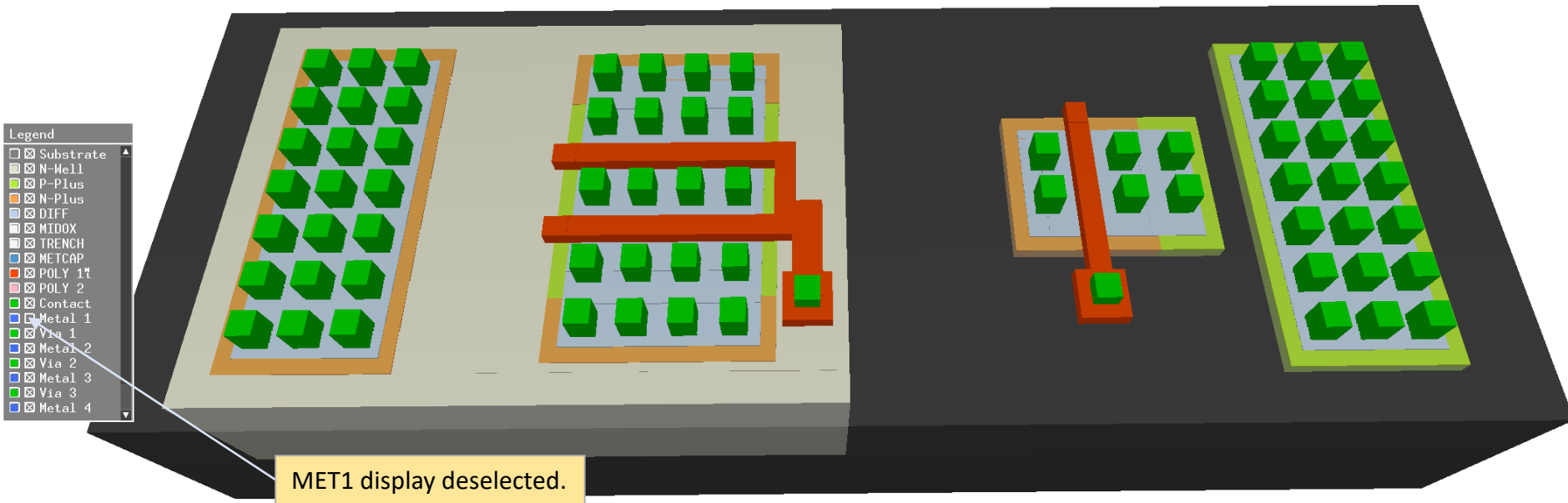
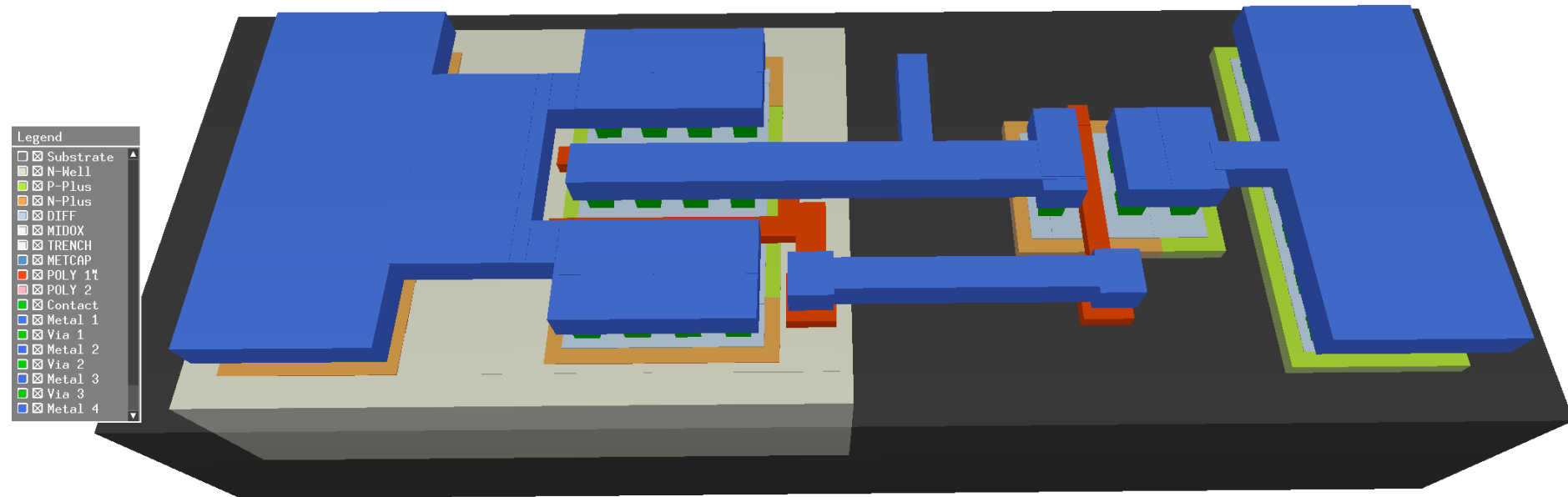
In the GDS3D-tool use F1 to see the (game like) usage.



Do not use the normal streamout from CDW (File -> Export -> Stream) because GDS3D uses a separate directory for the gds-File!

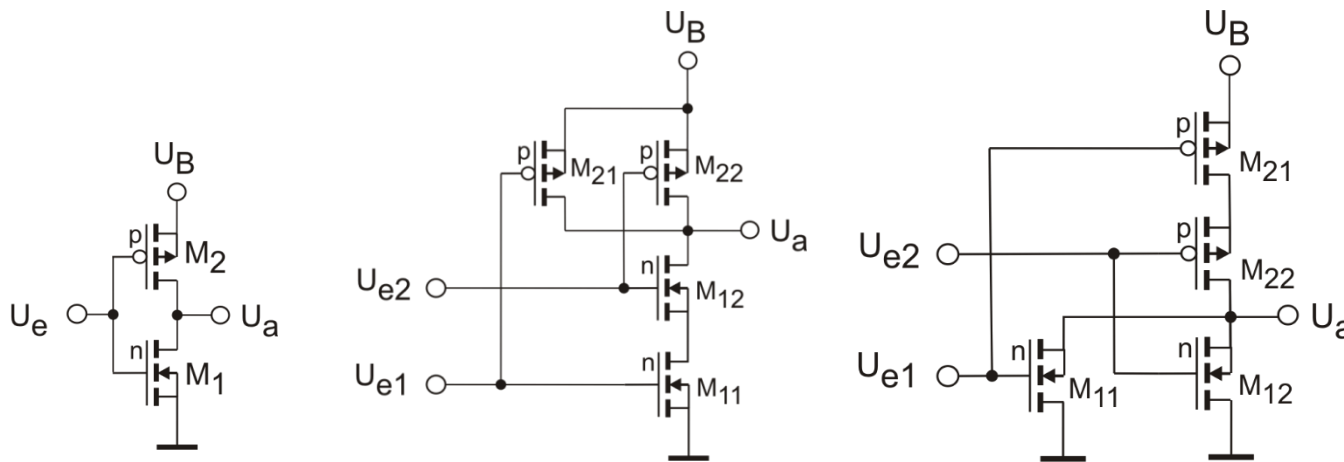
ICD is simply Integrated Circuit Design group at Twente University)

Layout 3D View



Lab: Circuit Design using Cadence and AMS CMOS 0.35μ Technology

Inverter, 2-Input-NAND, 2-Input-NOR



$$\begin{aligned}
 U_B &= 3,3V \\
 U_{GS0n} &= 0,48V \\
 U_{GS0p} &= 0,67V \\
 KP_n &= 170 \frac{\mu A}{V^2} \\
 KP_p &= 58 \frac{\mu A}{V^2} \\
 (d_{ox} &= 7,6 \text{ nm})
 \end{aligned}$$

Calculate the geometry in (W/L -ratio for p- und n-Transistors) so that you get a good compromise for the switching point and noise margin for the cases:

- Both inputs change at the same moment (connected)
- One input is preassigned to a fixed value so that the second one causes output change. (May be different for both inputs!)

Switching point should be near $\frac{U_B}{2}$ for all cases.

Design (schematic, layout) a 2-Input-NAND or a 2-Input-NOR using short channel length transistors (0.35μ) or long channel length transistors (3.5μm]. Selection of the specific design is done with the tutor.

Cell hight shall be 20 μm.

From Simulation (including postlayout) find out the following values:

Switching points and noise margin for the different cases at the two inputs.

Delay times (50%), falltime, risetime (20%-80%) dependend on load capacitance (4.. 100 fF) and temperature (-40 to 80°C).

Lab: Circuit Design using Cadence and AMS CMOS 0.35μ Technology

Inverter, 2-Input-NAND, 2-Input-NOR

At the switching point both transistor-pairs are in the pinch-off state and passed by the same current :

$$\frac{\beta_n}{2}(U_{es} - U_{GS0n})^2 = \frac{\beta_p}{2}(U_B - U_{es} - U_{SG0p})^2$$

But: There is a difference in the number of involved switching transistors for the different input cases!

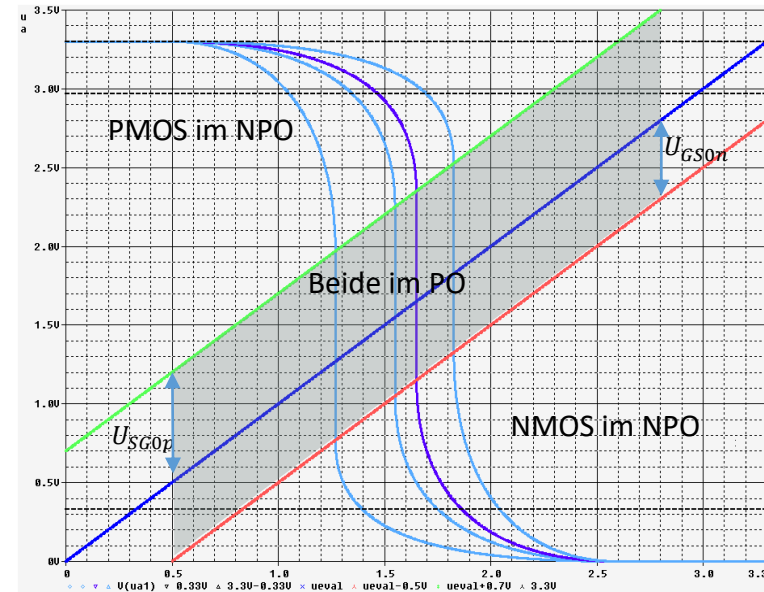
Common Equation for CMOS-Inverter:

$$\frac{\beta_n}{2}(U_{es} - U_{GS0n})^2 = \frac{\beta_p}{2}(U_B - U_{es} - U_{SG0p})^2$$

Dissolve for U_{es} :

$$\sqrt{\beta_n}(U_{es} - U_{GS0n}) = \sqrt{\beta_p}(U_B - U_{es} - U_{SG0p})$$

$$U_{es} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot U_{GS0n} + U_B - U_{SG0p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$



Für $U_{es} = \frac{U_B}{2}$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}} \right)^2$$

$$\beta = KP \cdot \frac{W}{L}$$

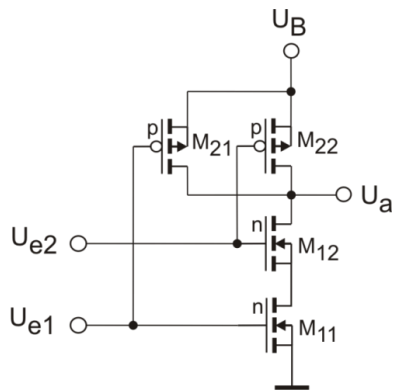
mit : $KPN = 3 \cdot KPP$

$$\frac{\left[\frac{W}{L} \right]_n}{\left[\frac{W}{L} \right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}} \right)^2$$

Lab: Circuit Design using Cadence and AMS CMOS 0.35μ Technology

Inverter, 2-Input-NAND, 2-Input-NOR

NAND-Gate



For $U_{eS} = \frac{U_B}{2}$ when both inputs change:

$$\frac{\beta_{nges}}{\beta_{pges}} = \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}} \right)^2$$

$$\beta_{nges} = KPN \cdot \frac{1}{2} \left[\frac{W}{L} \right]_n \quad \text{One transistor of double length}$$

$$\beta_{pges} = KPP \cdot 2 \left[\frac{W}{L} \right]_p \quad \text{One transistor of double width}$$

$$KPN = 3 \cdot KPP$$

$$\frac{\left[\frac{W}{L} \right]_n}{\left[\frac{W}{L} \right]_p} = \frac{4}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}} \right)^2$$

$$\frac{\left[\frac{W}{L} \right]_n}{\left[\frac{W}{L} \right]_p} = \frac{4}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n}} \right)^2 = \frac{4}{3} \left(\frac{1,65 - 0,7}{1,65 - 0,5} \right)^2 = 0,908$$

$$\frac{\left[\frac{W}{L} \right]_p}{\left[\frac{W}{L} \right]_n} = 1,1$$

Lab: Circuit Design using Cadence and AMS CMOS 0.35μ Technology

Inverter, 2-Input-NAND, 2-Input-NOR

$$\frac{\beta_n}{2} (U_{eS} - U_{GS0n})^2 = \frac{\beta_p}{2} (U_B - U_{eS} - U_{SG0p})^2$$

$$\sqrt{\beta_n} (U_{eS} - U_{GS0n}) = \sqrt{\beta_p} (U_B - U_{eS} - U_{SG0p})$$

One p-transistor is and remains off.
One n-Transistor is and remains on.
Only an inverter is switching.

Lower transistor in NAND during switching phase:

$$U_{eS} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot (U_{GS0n} + U_{DS11}) + U_B - U_{SG0p}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

See if the values are acceptable with regard to noise margin.
Try to change W/L ratios to find a compromise.

Für $U_{eS} = \frac{U_B}{2}$

$$\beta_{nges} = KPN \cdot \frac{W}{L} \quad \frac{\beta_n}{\beta_p} = \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n} - U_{DS11}} \right)^2$$

$$\beta_{pges} = KPN \cdot \frac{W}{L}$$

$$KPN = 3 \cdot KPP$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{U_B}{2} - U_{SG0p}}{\frac{U_B}{2} - U_{GS0n} - U_{DS11}} \right)^2$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1,65 - 0,7}{1,65 - 0,5 - 0,236V} \right)^2 = 0,36 \quad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 2,78$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1,65 - 0,7}{1,65 - 0,5} \right)^2 = 0,23 \quad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 4,44$$

Interesting, but we can implement one geometry only
and must configure a compromise.

Lab: Circuit Design using Cadence and AMS CMOS 0.35 μ Technology

Inverter, 2-Input-NAND, 2-Input-NOR

Practical hint to save time:

Starting from the Inverter schematic:

You may open the inverter schematic as the origin for the new design.

Then create a new schematic cellview (from CDW or Library Manager). **File -> New -> Cellview**

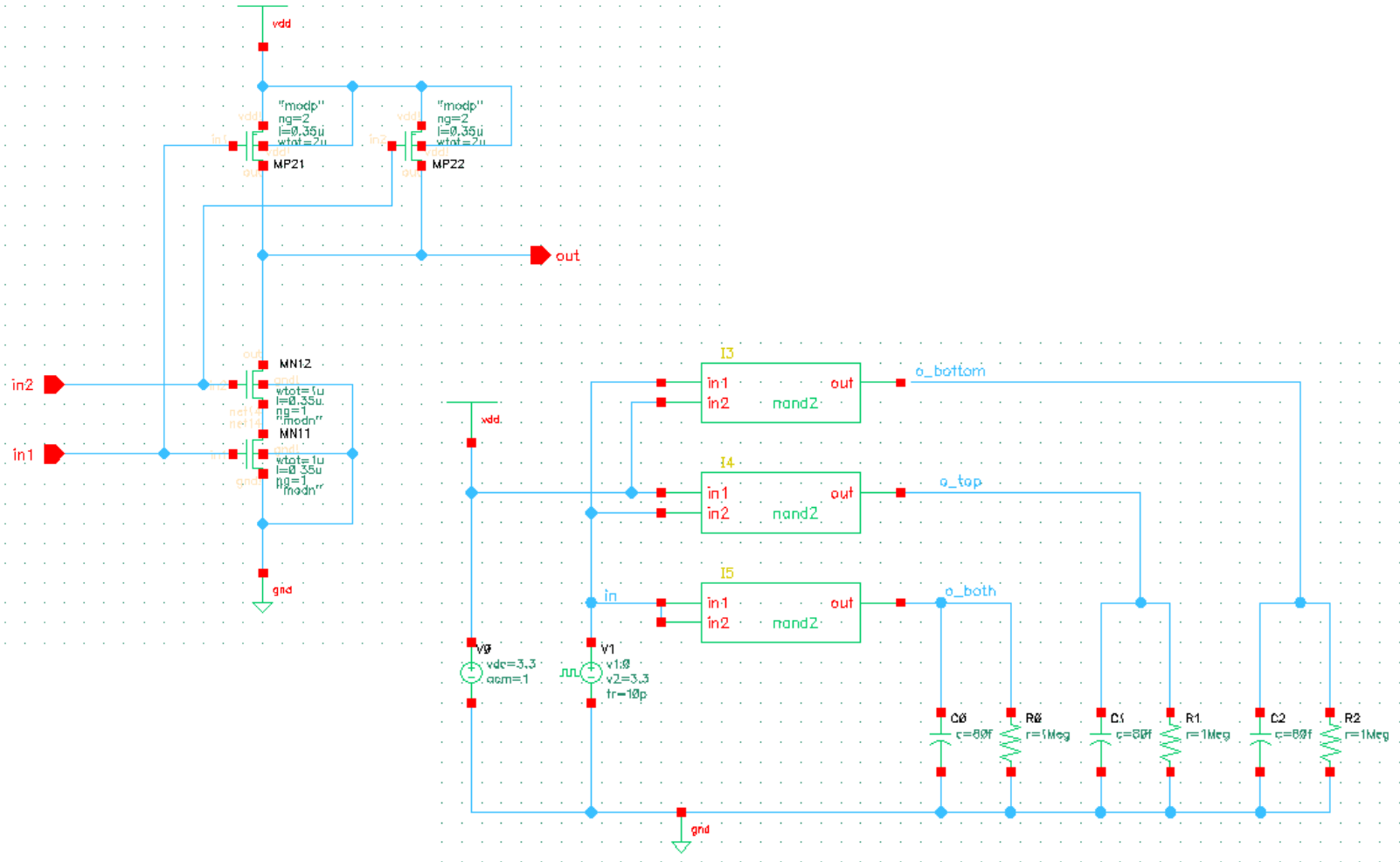
When you have the new empty schematic and the inverter schematic side by side you can copy the inverter circuit or parts of it to the new schematic.

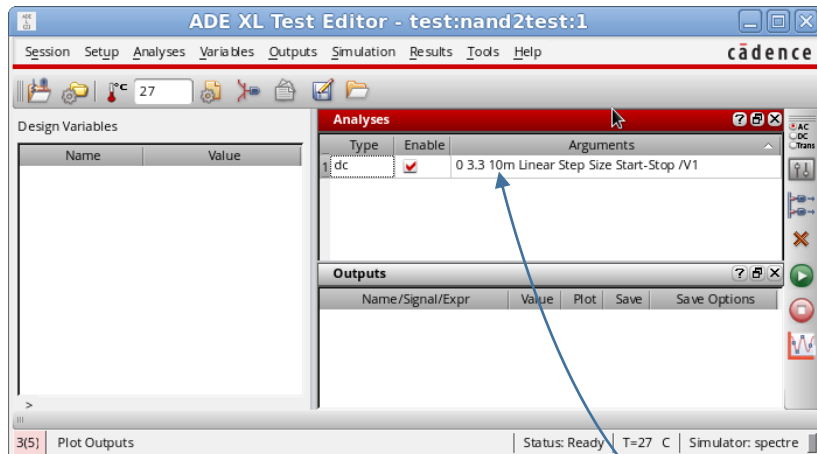
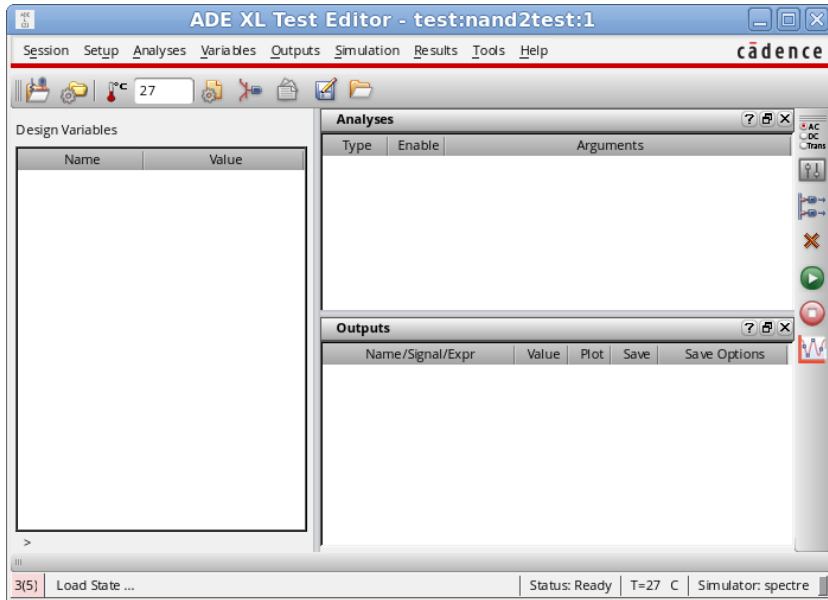
Use copy: "c" -> select the desired part using the left mouse button
 -> click on the selected part
 -> drag to the new place (may be the same schematic window or the new one)

Edit the new schematic to build the NAND or NOR design.

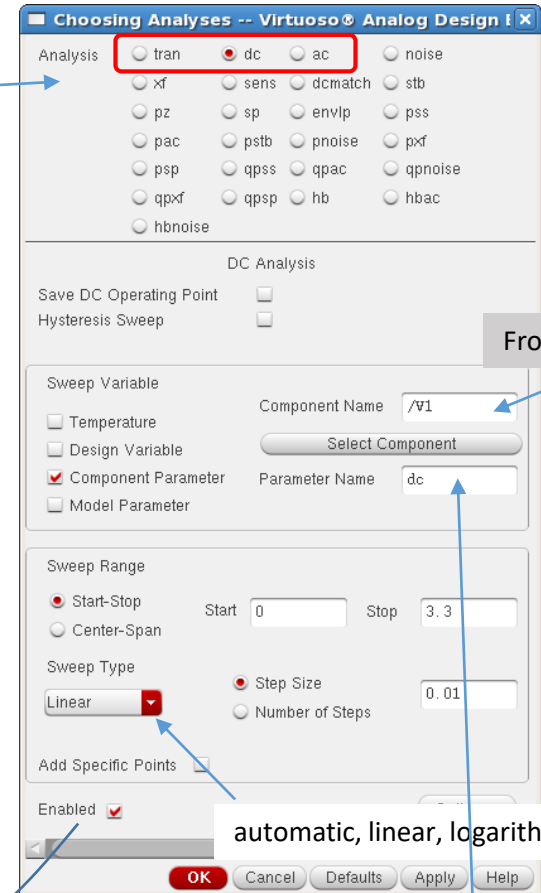
You may proceed in the same manner for the testbench.

2-input-NAND



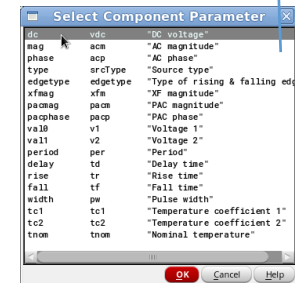


Create/Edit analyses
Design Variables
Simulation Outputs
Delete selected analyses
Run enabled analyses
Stop
Plot

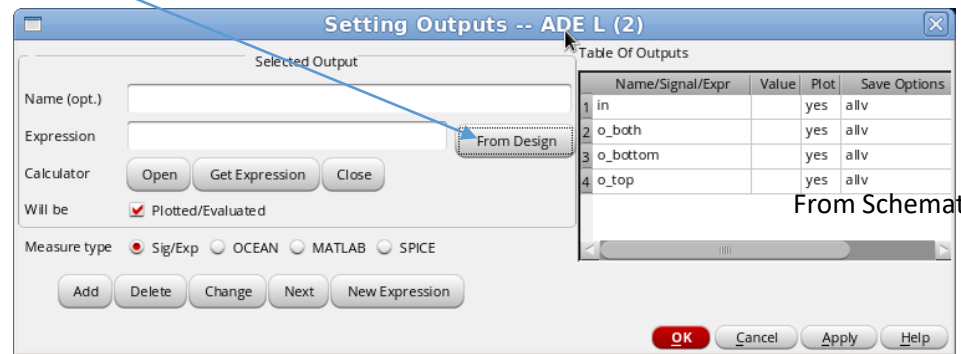
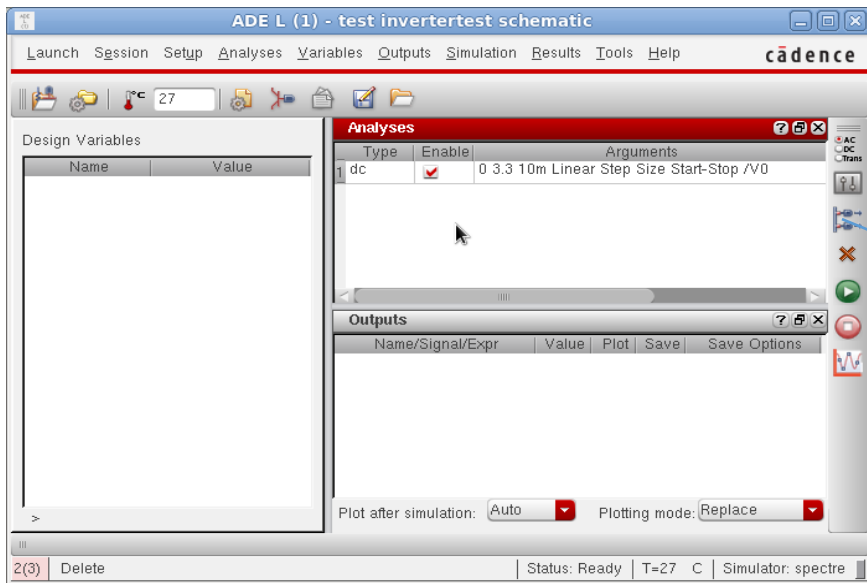


From Schematic

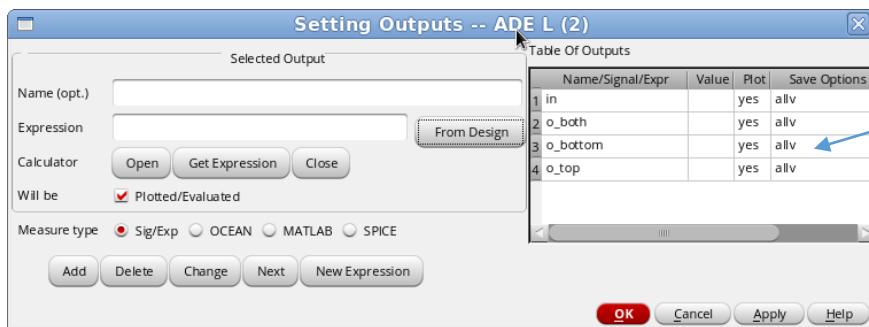
automatic, linear, logarithmic



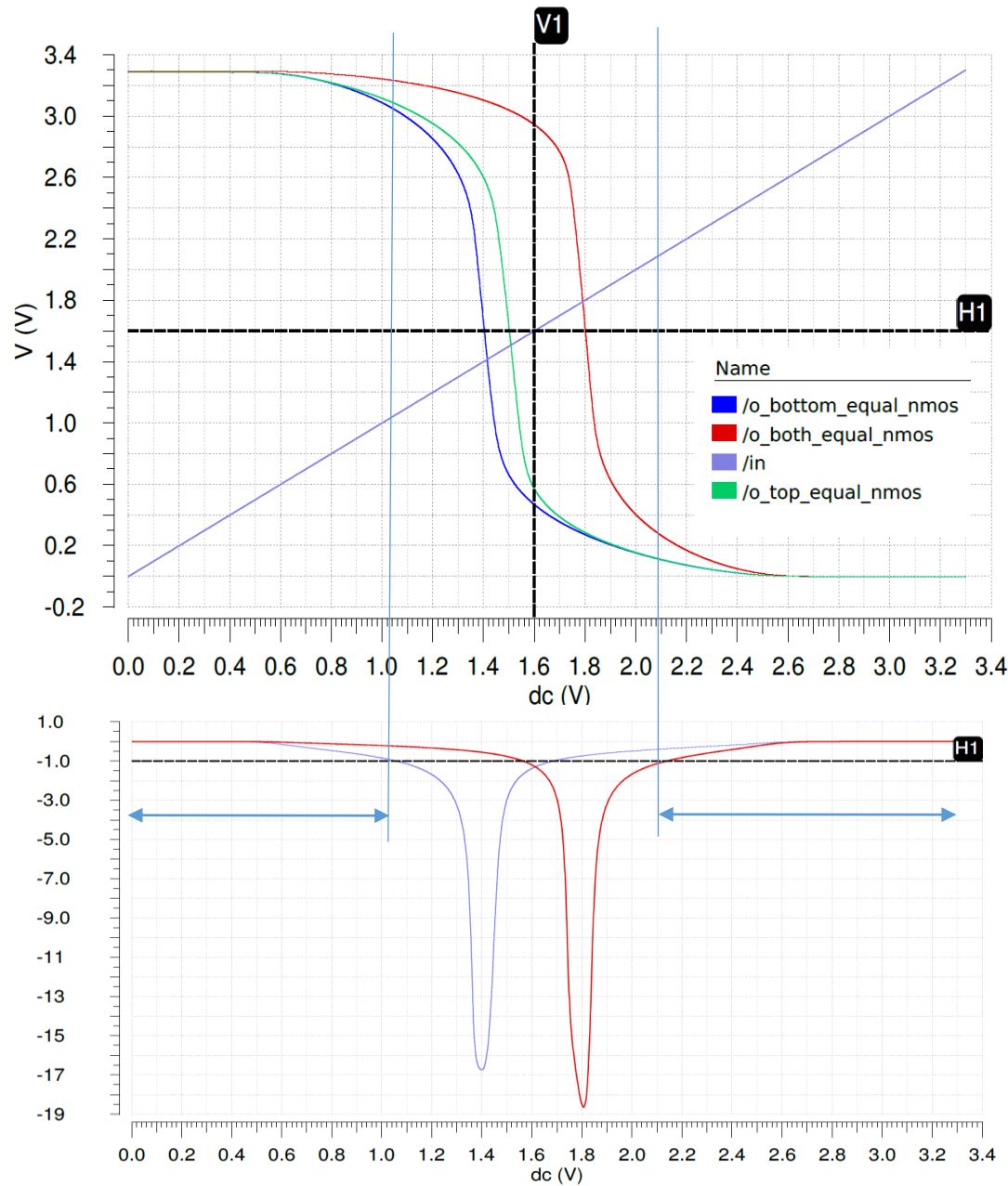
Intranet



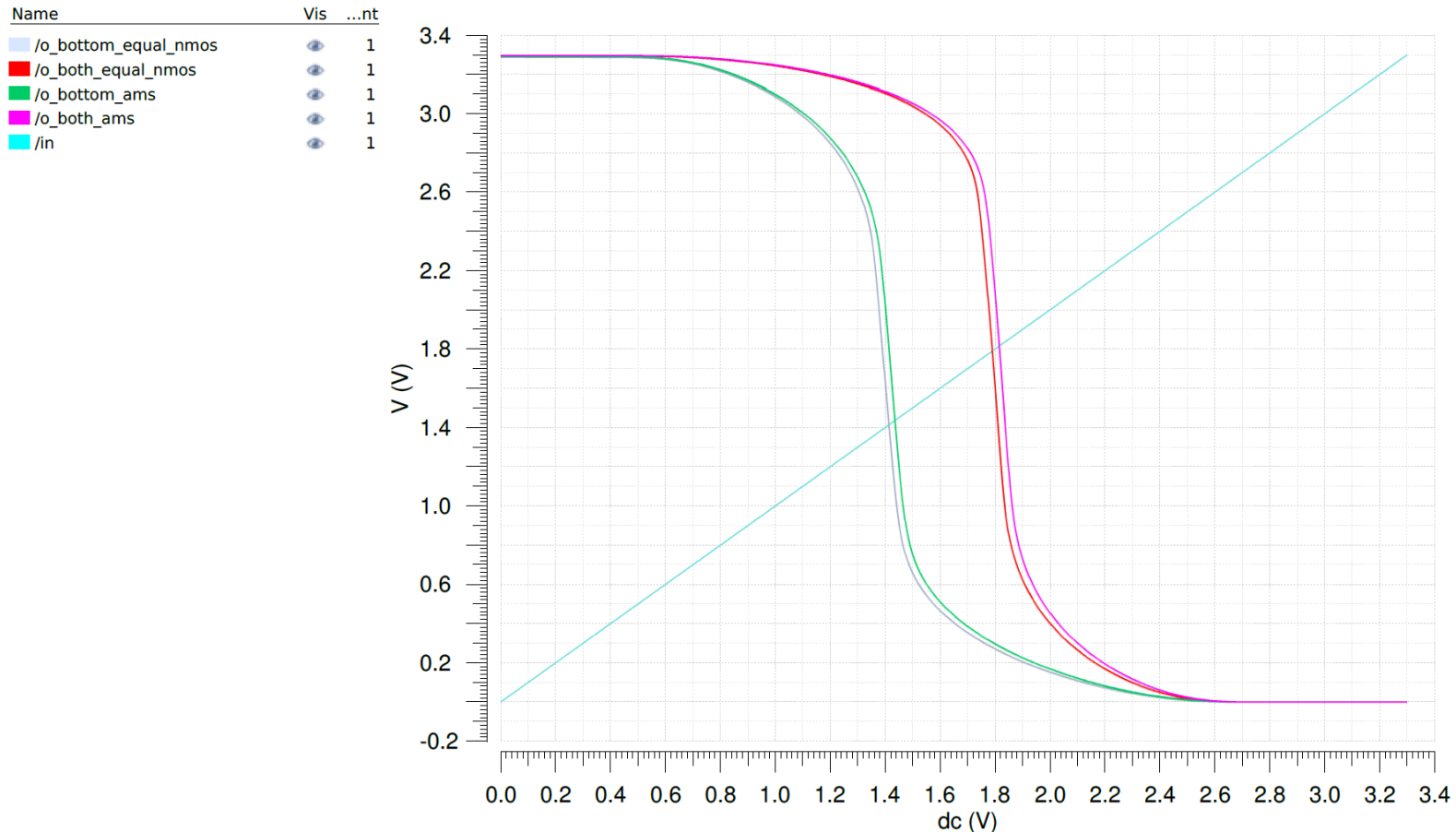
From Schematic



Transfer characteristics and noise margin for 2-Input-CMOS-NAND-Gate



Transfer characteristic for 2-Input-CMOS-NAND-Gates



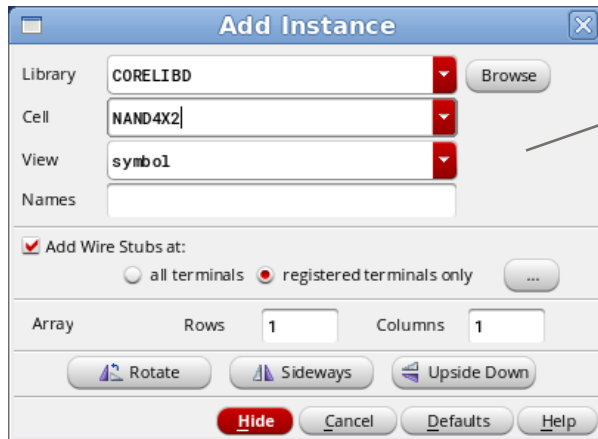
Transfer characteristic of 2-input-NAND-Gates from AMS-0.35 μ -library

with $L_{NMOS,PMOS} = 0.35\mu$ $W_{NMOS} = 1.325\mu$, $W_{PMOS} = 2.1\mu$ and self-made gate

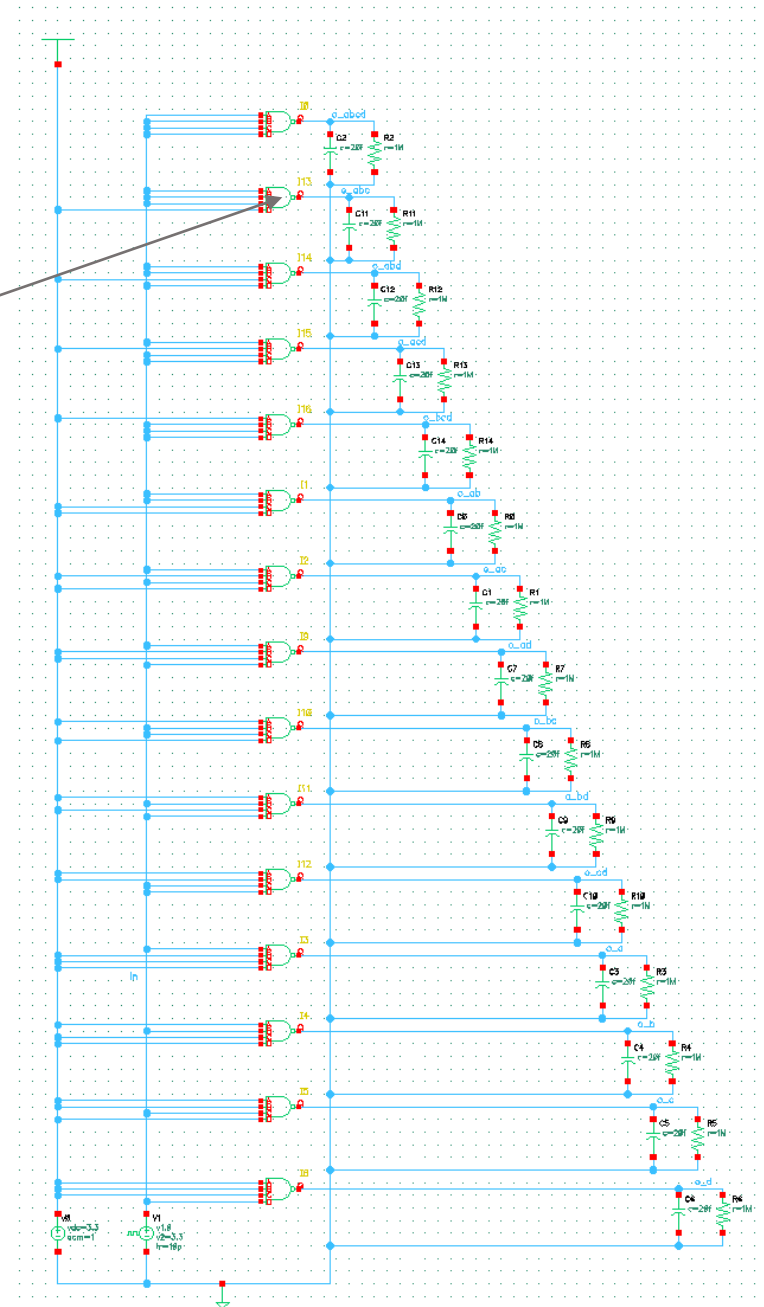
with $L_{NMOS,PMOS} = 0.35\mu$ $W_{NMOS} = 1.0\mu$, $W_{PMOS} = 1.6\mu$

(Characteristic for top N-transistor not shown, always between bottom and both)

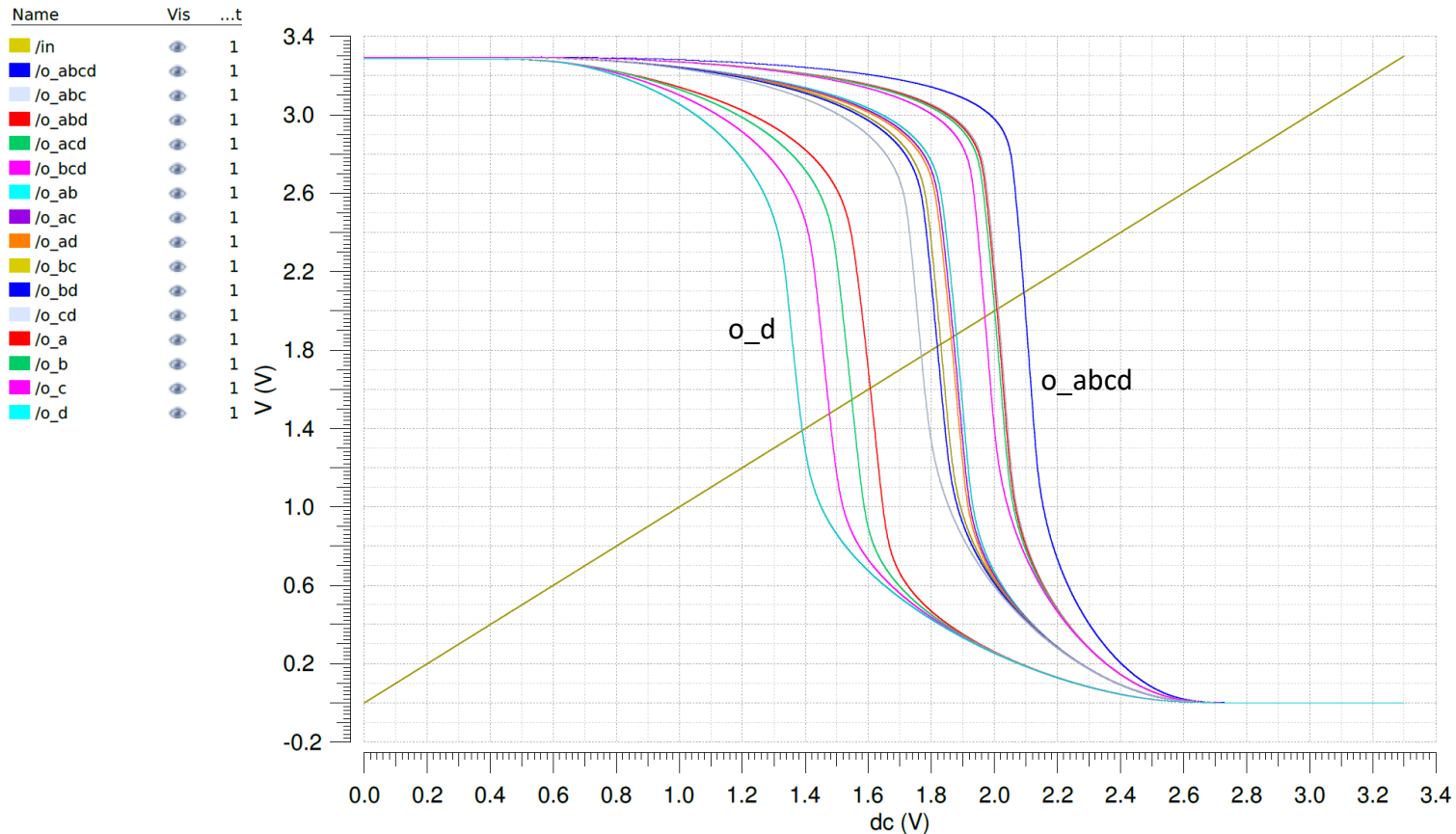
Simulation of 4-input-NAND from 0.35 μ m library



D-input uses NMOS-transistor nearest to GND, A-input is top NMOS-transistor.



4-Input-NAND-Gate



Transfer characteristic of 4-input-NAND-Gate from AMS-0.35 μ -library

with $L_{NMOS,PMOS} = 0.35\mu$ $W_{NMOS} = 1.05\mu$, $W_{PMOS} = 1.4\mu$

Leftmost line for switching lowest (nearest to ground)nmos-transistor only,
rightmost line for all 4 inputs switched simultaneously