### Cadence + AMS-Hitkit

Tutorial for creation of an inverter cell from schematic to layout with CADENCE using AMS-Hitkit and hints for multi-input gates

- 1. Using the Linux (CentOS) environment
- 2. Starting CADENCE with AMS-Hitkit
- 3. Creating a new library
- 4. Schematic entry
- 5. Creating a symbol and a testbench
- 6. Spice-Simulation using ADE XL
  - Analyses selection and setup
  - Using global variables
  - Parametric simulation
- 7. Starting Layout XL
  - Generate layout from schematic
  - The layer window
  - Wires, vias/contacts, wells
- 8. Design rule check
- 9. Layout versus schematic check (LVS)
- 10. Parasitic extraction (QRC)
- 11. Simulation of the extracted model (Post-layout simulation)

## Some UNIX-commands

We use CentOS-Linux (Free version "Community Enterprise OS" of RedHat), because Cadence supports RedHat or Suse. We use the KornShell (ksh), because it is the standard shell at ITMZ Uni Rostock.

#### pwd

ls, ls -alsi, ls dir cd -> cd /~/ske -> cd ./ske mkdir newdir cp , cp -r, cp -p mv chmod, chmod -R chmod 744 file grep use of | for pipeline -> ls | grep pattern rm, rm -r rmdir cat file man cmd history, h r 100

Our client computers use the "supported" CentOS 7, print working directory binary compatible to RedHat 7.5 list change directory make directory copy files/directories (recursive, preserve attributes) move or rename directories change file mode bits (security) -> -R recursive filter for pattern use command output as input for next command remove/delete remove directory show file at standard output show manual of cmd show command history run command number 100 from history



Or Right-Mouse on Background and select "Open Terminal"

To save windows images (.png) : Alt-Print

Unix-command to remove Cadence lock files (Close all Cadence programs before!): find ~/ -name "\*.cdslck" -exec rm {} \;

#### AMS-HitKit - Start

= Starting Cadence Design Framework with Libraries, Rules, Scripts provided for AMS-technology



AMS-HitKit - Start	ams hitkit amu hitkit Analog/Mixed-Signal Process Design Kit
🚺 What's New in IC6.1.6 Overview 📃 🗆 🗙	ama 4 10 ISB15 170901 C25/H25/S25
File Help cādence	copyright (c) 2017 ams AG, All rights reserved, ams AG entities the licensee only to develop ASICs which will be produced by the license. Usage of the hild is limited to terms and conditions defined in the hild license agreement.
Save As Search Print Refresh Close and Do Not Show Again Close For extended information on What's New in this release, select "Help - What's New - In this Release" in the CIW Window.	Were transformed appleton Laboratory Rutheford Appleton Laboratory Microelectronics Support Centre athe Science and Technology Facilities Council Rutheford Appleton Laboratory providers of WERE SCIENCE SUBJECTIONES EDESIGN TOOLS
Would stay open as long as ams_cds is running	Windows open for some seconds after ams_cds start
Command Interpreter Window - CIW Mes	ssages
Virtuoso® 6.1.6-64b - Log: /home/kirchner/C	DS.log
Eile Tools Options hitkit ICD-Tools Help	cādence

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mouse L:	M:	R:
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	Command Inputs	

#### AMS-HitKit - A new library

#### Command Interpreter Window - CIW

It is possible to create the library using the LIbrary Manager instead of CIW as well. The flow will differ (windows sequence).

Virtuoso® 6.1.6-64b - Log: /home/kirchner/CDS.log	_ O X)
<u>F</u> ile <u>T</u> ools <u>O</u> ptions hitkit ICD-Tools <u>H</u> elp	cādence
Library Manager created library "test" INFO (TECH-180011): Design library 'test' successfully attached to technology library 'TECH_C3	584 ' .
mouse L: M:     M:     I hitkit ams 4.10 Tech: c35b4c3 User: kirchner	R:

#### File -> New -> Library



#### AMS-HitKit - A new cellview

#### Command Interpreter Window CIW

(You can do this in the Library Manager as well)



🛄 Library Manager: WorkArea: /home/tfa011/ske2017test 💷 📼 🚿

View

Library... Cell View..

Category...

cādence

Lib: test Free: 25.27T

File Edit View Design Manager Help

Open.

Open (Read-Only)..

## AMS-HitKit Schematic Editor is open

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		W W BU		kirchner@KaterCent0S6: cd mypro	ject			
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#### Try to have a fixed arrangement for open windows (Terminal, CIW ..)

B

#### Schematic entry - Components



### **MOSFET:** Threshold Voltage



K.-P. Kirchner, Uni Rostock, Institut GS

# MOSFET: Threshold Voltage

inversion voltage

$$V_{TH} = \frac{Q'_b - Q'_{SS}}{C'_{OX}} - \frac{2V_{fb}}{2V_{fb}} - \frac{V_c}{V_c}$$
Contact voltage(s)
Compare with pn-junction, but here one side weakly doped:  $u_i < 2 \cdot 300mV$ 
Compare with pn-junction, but here one side weakly doped:  $u_i < 2 \cdot 300mV$ 
voltage over gate oxide
charge on gate = - charge on substrate
$$Q'_{b0} = eN_A t_d = eN_A \sqrt{\frac{2\varepsilon_{SI} \cdot |V_G - v_{fb}|}{e \cdot N_A}} = \sqrt{2eN_A\varepsilon_{SI} \cdot |-2v_{fb}|}$$
without bulk voltage
Thickness of depletion
area -> pn junction
$$t_d = \sqrt{\frac{2\varepsilon_{SI} \cdot |V_S - v_{fb}|}{e \cdot N_A}} = \sqrt{2eN_A\varepsilon_{SI} \cdot |-2v_i + V_{SB}|}$$
with bulk voltage
$$\frac{Q'_b - Q'_{SS}}{C'_{OX}} = \frac{Q'_{b0} - Q'_{SS}}{C'_{OX}} - \frac{Q'_{b0} - Q'_b}{C'_{OX}}$$
made to define a fixed part and a  $V_{SB}$ -dependent part
$$V_{TH} = -2V_{fb} - V_c + \frac{Q'_{b0} - Q'_{SS}}{C'_{OX}} - \frac{Q'_{b0} - Q'_b}{C'_{OX}} = -2V_{fb} - V_c + \frac{Q'_{b0} - Q'_{SS}}{C'_{OX}} + \frac{\sqrt{2eN_A\varepsilon_{SI}}}{C'_{OX}}} \left(\sqrt{|-2v_{fb} + V_{SB}|} - \sqrt{|-2v_{fb}|}\right)$$

K.-P. Kirchner, Uni Rostock, Institut GS

# **MOSFET: Threshold Voltage**



- $Q'_{b0}$  charge per (top) area under gate oxide in length  $\Delta L$
- $Q'_{SS}$ -charge stacked at surface

 $V_{TH}$  depends on:

substrate doping  $Q'_{b0}$  (used for adjustment) steep retrograde doping (light at surface, strong in body) thin channel, less dependent on  $V_{SB}$ )

oxide thickness (some nm, 2..20) substrate voltage (consider transistor location in circuit relative to GND/VCC) gate material (metal, n+-Si, p+-Si) surface charge density  $Q'_{SS}$ (Si, Na – ions)

### **MOSFET: Control Equation**



#### MOSFET: Control Equation, non pinched off



MOSFET: Control Equation, pinched off

$$I_D = \frac{W}{L} \cdot KP_n \cdot \left[ (V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Pinch off when:  $V_{GS} - V_{th} \le V_{DS}$ 

$$I_D = \frac{W}{L} \cdot KP_n \cdot \frac{(V_{GS} - V_{th})^2}{2} = \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2$$



## MOSFET: Control Equation, pinched off

$$I_D = \frac{W}{L} \cdot KP_n \cdot \frac{(V_{GS} - V_{th})^2}{2} = \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2$$

Channel-length modulation

$$I_D = \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2 \quad \rightarrow \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2 \cdot [1 + \lambda \cdot (V_{DS} - V_{DSsat})]$$



### **CMOS** Inverter Calculation





## File -> Check and Save (shft-x)

Avoid crossover dots. Warnings! May be deselected Check-> Rules-> Physical

17.12.2018

### Schematic Editor: Filter

Schematic editor has a filter function for selectable objects! Changing accidentally may prohibit selection!



## **Inverter Symbol from Schematic**

Symbol needed to use our design in higher levels of hierarchy.

First Example is the insertion of the design in a testbench.



Launch Eile Edit View Create Check Options Window hitkit Help

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Navigator

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MN0 (nmos4) MP0 (pmos4)

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and!

out

vdd!

in:P

- out:P

test

Library Name

Left Pins

**Right Pins** 

Top Pins

Bottom Pins

Load/Save 📃

Cell Name

»

#### Inverter Schematic for Simulation -> Testbench



### Simulation ADE GXL Start

#### From the Schematic Editor -> Launch -> ADE GXL



#### ADE XL creates a new view!

Creat	e new ADE (G)XL view 🛛 🗙
File	
Library	test 🔽
Cell	invertertest
View	adexl
Туре	adexi
Application	
Open with	ADE GXL -
🗌 Always use	this application for this type of file
Library path fil	e
/home/kirch	ner/ske/cds.lib
Open in 🥑 nev	w tab 🔾 current tab 🔾 new window
	OK Cancel Help

#### ADE (G)XL usage differs from ADE L Most tutorials use older ADE L

LDE Layout Dependent Effects EAD Electrically Aware Design



M

Status

O Corner
 Nominal Corner

mouse L

4(6)

R:

Cmd: Sel: 0

#### Simulation ADE GXL Create Test



#### Simulation ADE GXL Create Analyses



# Simulation ADE-XL/L Choose Outputs

🖀 ADE L (1) - test invertertest schematic	
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help <b>cādence</b>	
🛃 🔊   🦵 27 🛛 🔕 🎾 🖄 🗹 🗁	
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	Measure type  Sig/Exp OCEAN MATLAB SPICE
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	Add Delete Change Next New Expression
ADE L (1) - test invertertest schematic	<u>QK</u> <u>Cancel</u> <u>Apply</u> <u>Help</u>
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2/3)         Plat Outputs         Status Selecting outputs to be platted.         T=27. C. Simulator association.	
ctor Flot Outputs Selecting Outputs to be plotted   1=27 C   Simulator: spectre	

# Simulation RUN (in ADE-GXL)

# Run Simulation <

Virtuoso® Analog Design Environment GXL Editing: test invertertest schematic	_ <b> </b>	
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		Plot outputs

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#### Simulation ADE-L Evaluate Results



3.5

IGS / Uni-Rostock

Simulation ADE-L Evaluate Results using Delta Markers



K.-P. Kirchner, Uni Rostock, Institut GS

#### Simulation Parametric Analysis – Temperature (Built in)



### Simulation Parametric Analysis – Global and Design Variables

As an example we replace the fixed width of the PMOS transistor by a "Pwidth" in the inverter schematic. Open the schematic and change the "wtot" of the pmos transistor from fixed value t o "pwith"!

	ADE XL Test Editor - test:invertertest:1	_ <b>_ ×</b>	/ Start here to create a desi	gn variable
	S <u>e</u> ssion Set <u>up</u> <u>A</u> nalyses <u>V</u> ariables <u>O</u> utputs <u>S</u> imulation <u>R</u> esults <u>T</u> ools <u>H</u> elp	cādence	Editing Design Variab	les ADE L (1) ×
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	2 OUT allv	*	<u>o</u> k	<u>Cancel</u> <u>Apply</u> <u>Help</u>
	4/61 Choose Design	ive III		
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If t	here is only the testbench schematic open,	Launch <u>File</u> dit <u>V</u> iew <u>C</u> rea	e Chec <u>k</u> Options <u>M</u> igrate <u>W</u> indow Pa <u>r</u> asitics <u>A</u> DI	∃GXL hitkit <u>H</u> elp <b>cādence</b>
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Glo	bal variables are valid for all tests in the adexl-view	Vominal Corner		
Glo	bal variables overwrite design variables with same name			· · · · · · · · · · · · · · · · · · ·
Ov	erwritten design variables are shown with a horizontal strike	History Item Statu	3	
lt i	s possible ( $\rightarrow$ RM over design variable) to update a global variable	mouse L; schSingleSelectPt0		
fro	m a design variable	4(6) hitkit: ams_4.10 Tech: c35b4	c3 User: kirchner	Cmd: Sel: 0   T=27.0 C   Simulator: spectre

#### Simulation Parametric Analysis – Using Variables



# **CMOS** Inverter Capacitances and Delay





+

K.-P. Kirchner, Uni Rostock, Institut GS

# CMOS Inverter Capacitances, Output Resistance and Delay Output resistance of FET for charge reversal U<sub>GS</sub>=U<sub>B</sub> Single transistor at $V_{DD}$ with input voltage at $V_{DD}$ Uns UR $I_D = \frac{\beta_n}{2} (V_{DD} - V_{thn})^2 = \frac{KPN}{2} \frac{W}{I} (V_{DD} - V_{thn})^2 = \frac{170}{2} \frac{\mu A}{V^2} \cdot \frac{1\mu m}{0.35 \mu m} \cdot (3.3V - 0.5V)^2 = 0.68 \, mA$ $R_n = R_p = \frac{V_{DD}}{I_p} = \frac{3.3V}{0.68mA} = 4.85 \ k\Omega$ Capacity and time constant-> Delay time (50%-cross distance) $C_{in} = \frac{3}{2}W \cdot L \cdot C'_{ox}$ $C_{in} = 4.5 \frac{fF}{\mu m^2} \cdot \frac{3}{2} (1+3.2) \ \mu m^2 = 28.35 \ \text{fF}$ $C_{out} = W \cdot L \cdot C'_{ox}$ $C_{out} = 4.5 \frac{fF}{\mu m^2} \cdot (1 + 3.2) \ \mu m^2 = 18.9 \ \text{fF}$ next gate (+ wire capacitances) $t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot (C_{inn} + C_{inp} + C_{outn} + C_{outp})$ Ausgang $t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot C'_{ox} \cdot \frac{5}{2} (W_n L_n + W_p L_p)$ 0,5 UH $t_{pHL} = t_{pLH} = 0.7 \cdot 4.85 k\Omega \cdot 4.5 \frac{fF}{\mu m^2} \cdot \frac{5}{2} (1 + 3.2) \mu m^2 = 160 \text{ ps}$ Eingang Eingang ps

ps

#### Simulation Transient Analysis





## Simulation Transient Analysis



# Oops!, looks strange ... 1pF load is too much for our small gate

Changed load to 80 fF Compare with data sheet of ams standard cell next page!

Name

in (in out\_schemetic

falltime: 1.555ns-1.1545ns=400 ps risetime: 2.2404ns-2.0601ns=180 ps delay(inp rise): 1.3324ns-1.005ns=327 ps delay(inp fall): 2.1328ns-2.015ns=118 ps



#### Simulation Transient Analysis

Try another parametric simulation with Load Capacitance as a parameter! Compare results with a given cell from AMS!



INV0



Databook Build Date: Wednesday Jun 18 17:26 2014 Copyright © 2004-2013 Nangate Inc. Conditions for characterization library c35\_CORELIB\_TYP, corner c35\_CORELIB\_TYP\_typical: Vdd= 3.30V, Tj= 25.0 deg. C . Output transition is defined from 20% to 80% (risput se) and from 80% to 20% (falling) output voltage. Propagation delay is measured from 50% (input rise) or 50% (output rise) or 50% (output rise) or 50% (output fall).


#### Simulation Transient Analysis

#### Using Calculator and functions to show delay, fall time, rise time

Calculator works with stack in RPN

Input and output from voltages transient simulation VT("/in"), VT("/in") used in the function "delay"

			Virtuoso (	R) Visualiz	ation & Ana	lysis XL cal	culator		×
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#### **Simulation Transient Analysis**

Similar to the input-output-delay you may use the risetime and falltime functions



# Layout Start and Generate from Schematic

Layout Star	t anu C	Jenerale		matic		Startup Option
Replace all the Variables in the design with fixe	d values.		Fold the Pl	MOS (2 gates)	Phys	cal Implementation Startup Options
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variables in the testbench are not anected, beca	ause they	will hot be	involveu in t	The layout.	Cor	nfiguration
In Schematic Editor: Launch -> Layout XL —						Create New 🔾 Open Existing
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Congrator a layout with all instances placed out	cido a rov	stangla (act	imated cell b	oundary	Orientation	RO
Generates a layout with an instances placed out	SILLE a LEC	Langle (est		ouriuary)		OK Cancel Help

# Layout Floorplaning



# Layout Edit



METRES

METRES

MET1

metal3

metal4

hol

# Layout (Automatic) Pin Placement (optional)

#### In Layout XL: Place -> Pin Placement

Form offers a chice to place pins at top (vdd!) bottom (gnd!) left (inputs) and right (outputs) For top (vdd!) and bottom (gnd!) the pins can be extended to rails with the width up to the cell width and a defined hight.



Signal pins may be placed left or right first, then change the placement to "any" and move to the appropriate location. As long as they have the attribute "left" or "right" they are <u>locked to the edge</u>. Other way : Properties -> Placement Status -> Unplaced

# Layout (Automatic) Placement of Instances (optional)

For a simple inverter with two tansistors it is easy to identify the transistors and to place them in an appropriate pattern in the layout. Fore more complex designs some kind of automatic placement may be used. Here shown for an operational amplifier (OPA) and the placement option "like schematic". Helps to identify the instances/parts.







Layout of single contact predefined. Do not change! Number and alignment variable. Using "**Compute from Shape(s)**"/fills area with appropriate number of contacts.

			Create V	ia		×
Mode Compute	● Sin From ● Ro	gle 🔾 Stack	O Auto O Fa	st Edit Shape(s) 🔾 I	Drawn Area	Options
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Stacked VIAs connecting more than two layers available:



# Cell Layout – Design Rule Driven Design -DRD (optional)

To avoid design rule violations when moving instances or wiring we can switch on the DRD.

#### Options -> DRD-Edit

#### You must select one mode here!

	DRD	Options	$\mathbf{X}$
DRD Mode Z E	nforce 🔲 Noti	ifv 🔲 Post-Edit	
Hierarchy Depth	Top Level		
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✓ ✓	<b>V</b>	<ul> <li>Spacing</li> </ul>	
	<b>V</b> (	🗹 Via	-
✓	<b>y</b> (	Vidth Width	-
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	✓ 1	<ul> <li>Complex Spacing</li> </ul>	$\sim$
	✓ 1	<ul> <li>Edge Length</li> </ul>	
✓	✓	<ul> <li>Extension</li> </ul>	
	✓	Mum Cut	
Categories Notify	y Displa y Filter		
Interactive Display	·	Interactive Options	_
🗹 Halos		Enforce	
Dashed	True Color	Enable Pushing	
✓ Rule Text	T	Jump Wires	
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Drawing Color			
y0	drw 🗾		-1
	)		
Post-Edit Options- Marker Limit	5000	Timeout (secs)	
		cel Apply Defaults <u>H</u> e	lp)

"Enforce" stops edit action (route a wire, move an element) if a design rule is violated.

"Notify" writes a warning if a design rule is violated.

"Post-Edit" sets markers only if a design rule is violated.

# Cadence Layout - LVS



Dann fehlen im av extracted die design layer

That's what we want to see!

Necessary for QRC parasitic extraction

ams says: "Do NOT use the resimulate\_extracted switch because

in that case substrate shorts (soft connections between

different nets via substrate) might not be found correctly!

http://asic.ams.com/hitkit/hk410/assura/assura.html 17.12.2018

cādence

#### Cadence Layout - DRC

#### Assura -> Run DRC



Here you may open the rule set file for information. Contains all the rules like distances, overlap, min. width et cetera.

*	Error Layer Window		)   <	Do you want to view the results of this run?
File View Error-Visibility Show I	Fror by	Help		,
[1] # INF0: C35B4/C35B3 ASS	URA DRC DECK (REV9 DATE 26-Apr-2011) Last modified 29-Oct-20	Y		Yes No Help
AV NV	1	(1) investes lauret test	r -	
[1] INFO: hot nwell		[1] Inverter lagout test		
[1] PO_R_1 Minimum density	of POLV1 area [%] = 14			∧ 8 No DRC errors found.
[1] M1_R_1 Minimum density	of MET1 area [%] = 30			9
[1] # INF0: C35B4/C35B3 AS	SURA DRC DECK (REV9 DATE 26-Apr-2011) Last modified 29-Oct-		The second se	Close
	ד_	[]]2		

That's what we would like to see!

#### Cadence Layout – DRC with Errors remaining

#### Example for an Error Message: Here: Pin is not fully covered by metal









# Cadence Layout - DFM





Electrical rule check is included in DRC. There is no separate rule check in the ams-HITkit.

Starting ERC with Assura -> Run ERC opens a form similar to DRC with no technology selected and either rule files.

Up to now no verification for this. Separate ERC-usage found nowhere.

# Cadence Layout – QRC – Parametric Extraction

RC -> Run As	ssura Quantus -QRC	
changes	Quantus QRC (Assura) Interface X	
\	Run Directory //home/kirchner/ske2018/ASSURA_LVS/inverter	
$\langle \rangle$	Run Name	<b>Coupled C</b> : net to net (signals)
$\sim$	seit 6 1 7 dazwischengeschaltet	<b>BC</b> Decoupled C: net to power and ground only
	Sere of 117 during of the ingestimate of	
	*	
	QRC (Assura) Parasitic Extraction Run Form X	QFC (Assura) Parasitic Extraction Run Form
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Rule Command F	ile Include	Mult Factor 1.0 Dimusion Equation R
Tech Cmd File	Jser - View Edit	PEEC Mode 🗌 Ladder Network 🔲 Global Frequency MHz
		Select User Region View Edit
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Parasitic Cap Comp	onent propacitor auLys PRIML Prop Id c	
Parasitic Ind Comp	nent ninductor autus PRTMLI Pron Id 1	Select P Mash Liser Region
Paracitic M Compo	wind and and a DETMINE Propid L	
Industance L1 Pres	le industria la presidencia la Decentra industria	
inductance LT Prop	iu indi inductance L2 Propiu indz	From File
Call Procedure		SelF-romScri
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Substrate Profile	NONE Stract MOS Diffusion High	Litho QRC Run in progress View Edit
Library Drafes		Conto
Library Pretix		
Library Directory		Run Dir: //nome/kirchner/ske/ASSURA_LVS/inverter
		Process Id: 6897 (Ipc:16) The output is in :
© X		Start lime: Jan 22 11:11:15 2016
Library Directory:	Specify a directory for writing local libraries created	HRCX Cells Cell: inverter
during the hierarg	hical extraction of an extracted view	VV CIL: View: av_extracted
daring die illefalt		Watch Log File
		OK Cancel Help View Command File Help

#### Cadence – QRC – Extracted view



They will be included in simulation netlists.

# Cadence – QRC – Post-Layout Simulation (ADE-L/XL)

We need different models for the UUT (inverter)

Original schematic



17.12.2018

IGS / Uni-Rostock

Template will fill the form in background.

# Cadence – Post-Layout Simulation (ADE-L/XL)

🐂 Virtuos	so® Hierarchy Editor: New Config	uration (Save Needed)		Virtuoso® Hierarchy I	ditor: New Configura	ation (Save Neede	d) _ 🗆 🗙
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Tan Call	&			- 🕞   📝 🕹 🥱 🦿 🤅	) = ~  [] @	Ø Update Needed	
Tup Cell			Top Cell		? 🖥 🗙	Global Bindings	? 🗗 >
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Instant (test inverter C 1 (anal C 1 (anal R 0 (ana R 0 (ana R 1 (ana V 0 (ana V 1 (ana V 1 (ana	ice View To Use _postlayout sc ogLib cap spec ogLib cap spec verter schemat Explain Open Open Open (Read-Only) Expand Instance Expand Subtree Collapse Subtree Collapse Subtree Collapse Subtree Collapse Subtree Add Stop Point Remove Stop Point Add Bind To Open (Skip Instance) Remove Bind To Open	Inherited View List spectre cmos_sch schematic verilo spectre cmos_sch schematic verilo spectre cmos_sch schematic verilo snore- av_extracted layout schematic symbol Specify SPICE Source File Specify Referer ce Verilog Mark as External HDL Text (AMS UNL only)	Table	View Tree View Instance (test inverter_postlayout sc C (0 (analogLib cap spec C (1 (PRIMLIB pmos C (1 (PRIMLIB pmos C (1 (PRIMLIB pmos C (2 (PRIMLIB pmos) C (2 (PRIMLIB pmos	View To Use	Inheriter spectre cmos_si spectre cmos_si	d View List ch schematic ver ch schematic ver
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20(32) >			20(32) >				
				1			

Parasitics

Replace (use RightMouse -> Set Instance View ) schematic by av\_extracted

Now we have two different models for the two Inverters.

## Cadence – Post-Layout Simulation - Result

#### Open the configuration in Library Manager





#### Shown for $C_{Load}$ = 4 fF. Less difference for higher load.

(if  $C_{Load}$  is higher parasitic capacitors have less influence)

# To perform simulation see slides above from "Simulation ADE GXL Start"



OK, no visible change

#### Layout 3D View

#### GDS3D from University of Twente, NL

Needs a technology file (layer thickness, pitches). Generated for AMSC35B4 from process parameters. Needs initialization for Cadence integration, but may be used standalone.

Automatic initialization does not work yet. For manual initialization observe the last output after CIW start.

C Virtuoso® 6.1.5 - Log: /home/kirchner/CDS.log	Virtuoso® 6.1.5 - Log; /home/kirchner/CDS.log
Eile Iools Options Help cādence	Eile Tools Options ICD-Tools Help cadence
Loading ams.cxt Virtuoso Framework License (111) was checked out successfully. Total eneckout time was 0.10s. To get new Tab "ICD-Tools" for 3D-GDSII-Display in CDW execute following command manually: load "/progs/GDS3D_1.8/skill/icdGDS3D.il"	To get new Tab "ICD-Toolb" for 3D-GDSII-Display in CDW execute following command manually: load "/progs/GDS3D_1.8/shill/icdGDS3D.il" load "/progs/GDS3D_1.8/shill/icdGDS3D.il" GDS3D v1.8 has been initialized.
load "/progs/GDS3D_1.8/skill/iodGDS3D.il"           Immouse L:         M:           1         load "/progs/GDS3D_1.8/skill/icdGDS3D.il"	Imm         Imm           Immouse L:         M:         F           1         Immouse         F
	C Virtuoto® 6.1.5 - Log: /home/kirchner/CD5.log

With a layout opened we can make a GDSII-Stream and run the GDS3D tool. ICD - Tools

In the GDS3D-tool use F1 to see the (game like) usage.

Č	Virtuoso® 6.1.5 -	Log: /home/kirchner/CDS.log	
<u>F</u> ile <u>T</u> ools <u>O</u> ptions hitkit	ICD-Tools <u>H</u> elp		cādence
Writing GDS for test/opv GDS written successfully Starting GDS3D	Layout -> GDS3D Run GDS3D	gds∕op⊽.gds, please wait	
mouse L:		M:	R:
1 hitkit: ams_4.10 Tech: c35	ib4c3 User: kirchner		

Do not use the normal streamout from CDW (File -> Export -> Stream) because GDS3D uses a separate directory for the gds-File!

ICD is simply Integrated Circuit Design group at Twente University)

#### Layout 3D View





IGS / Uni-Rostock

#### Monte Carlo simulation using matching parameter

Open testbench schematic -> Launch ADE-XL -> existing view ADE-XL (assuming we have such a view already)

Use one of the tests from the normal schematic simulation

Here we use the dc-analyses to investigate the transfer characteristic.

RM over name of the test (e.g. test:name:19  $\rightarrow$  "Open Test Editor"

With Setup-> Model Libraries: Select cmosmc for the transistors (we have only transistors here we could select ...mc for other parts)



## Monte Carlo simulation using matching parameter



We investigate the following expressions:

Switching point: Low logic value noise margin: High logic level noise margin: cross(VDC("/vout") 1.65 1 "either" nil)
cross(deriv(VDC("/vout")) -1 1 "either" nil)
(3.3 - cross(deriv(VDC("/vout")) -1 2 "either" nil))

To set the output expressions: "add expression" - > open calculator

Monte Carlo simulation using matching parameter



For the LOW noise margin we use the "cross"-value, for the HIGH noise margin we use 3.3-"cross"-value



# Monte Carlo simulation using matching parameter



#### See it running in the buttom left corner



#### Monte Carlo simulation using matching parameter



Distribution of noise margins (mismatch only)

K.-P. Kirchner, Uni Rostock, Institut GS

#### Monte Carlo simulation using matching parameter



# Monte Carlo simulation and yield prediction

Define (realistic) specs for characteristics: Inverter:  $V_{inHL}$ ,  $V_{mHigh}$ ,  $V_{mLow}$  ...



From: https://community.cadence\_com/cadence\_blogs\_8/b/cic/posts/the-art-of-analog-design-part-2-monte-carlo-sampling

### Monte Carlo simulation and yield prediction

# Set specs in adexl outputs window:

low level margin > 1.2 V high level margin > 1.2 V 1.50 V < switching voltage < 1.80 V

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	test:invertertest:1		signal /out_scher	matic				point 🗹			
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	test:invertertest:1		expr riseTime(V	/T("/out_schematic") 3.3 nil	0 nil 20 80	nil "time")		point 🗹			
	test:invertertest:1		expr fallTime(V	T("/out_schematic") 3.3 nil (	0 nil 80 20 r	nil "time")	-	point 🗹			
	test:invertertest:1		expr (3.3 - cross	s(deriv(VDC("/out_schemati	ic")) -1 2 "eit	(her" nil	ł	point 🗹	>	1.2	
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# Monte Carlo simulation and yield prediction

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Next slide!

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	test:invertertest:1	fallTime(VT("/out_schen	natic") 3.3 nil 0 nil	80 20 nil "time")	268.5p	441.7p	341.1p	339.7p	26.8p			
	test:invertertest:1	(3.3 - cross(deriv(VDC("/	/out_schematic"))	-1 2 "either" nil))	1.178	1.521	1.36	1.361	57.22m	> 1.2		
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Be aware that we did not change opereating environment (temperature, supply voltage)

## Monte Carlo simulation and yield prediction

# $C_p$ und $C_{pk}$ Process Capability Statistics

 $C_p$  shows the relation beetwen Engeneering Tolerance (specs) to the Natural Tolerance (process) for a process with a distribution centered beetween specifications. For the Natural Tolerance the  $6\sigma$ -interval  $\pm 3\sigma$  is commonly used



Mittelwert

Mostly the distribution is not centered and the corrected value is used (maybe used for centered distribution as well):

$$C_{pk} = \frac{minimum(USL - \mu), (\mu - LSL)}{3\sigma}$$

If  $C_{pk} = 1$  then 99.73% of the samples will meet specs, for  $C_{pk} = 2$ : 99.999998%

"Recommended": Values beetween 1.25 to 2.0 dependend on safety demands > 2.5 area reduction possible? cost!

# Advanced Simulation Corner Simulation

FEOL (front end of line) Corners: Transistors n-channel , p-channel all processes used for individual parts (transistors, resistors)

"Fast" means "best":

-thin oxide -smaller length -higher width TT : typical n-channel- and p-channel-FETs SS : slow n-channel-FET, slow p-channel-FET SF : slow n-channel-FET, fast p-channel-FET FS : fast n-channel-FET, slow p-channel-FET FF : fast n-channel-FET, fast p-channel-FET

transistors affected in simila

Corners affect not only speed but also transfer characteristics (dc-dc)

BEOL (back end of line) Corners: Wires

all processes after making parts -> wires, vias

Temperature, Voltage

ams (and others):

TM: typical values - corresponds to TT WS : worst slow – slow n and slow p corresponds to SS WP: worst power – fast n and fast p corresponds to FF WO : worst One – slow n, fast p corresponds to SF WZ: worst Zero – fast n, slow p corresponds to FS

# Corner Simulation – Corner Preparation

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Here we can see all the selected corners

#### **Corner Simulation – Import Corners**



# Corner Simulation – Run and Results

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# Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology Inverter, 2-Input-NAND, 2-Input-NOR



Calculate the geometry in  $\binom{W}{L}$ -ratio for p- und n-transistors) so that you get a good compromise for the switching point and noise margin for the cases:

- Both inputs change at the same moment (connected)
- One input is preassigned to a fixed value so that the second one causes output change. (May be different for both inputs!)

Switching point should be near  $\frac{V_{DD}}{2}$  for all cases.

Design (schematic, layout) a 2-Input-NAND or a 2-Input-NOR using short channel length transistors ( $0.35\mu$ ) or long channel length transistors ( $3.5\mu$ m]. Selection of the specific design is done with the tutor.

Cell hight shall be 20 µm.

From Simulation (including postlayout) find out the following values: Switching points and noise margin for the different cases at the two inputs. Delay times (50%), falltime, risetime (20%-80%) dependend on load capacitance (4.. 100 fF) and temperature (-40 to 80°C).

## Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology Inverter, 2-Input-NAND, 2-Input-NOR

At the switching point both transistor-pairs are in the pinch-off state and passed by the same current :

$$\frac{\beta_n}{2}(V_{inSP} - U_{thn})^2 = \frac{\beta_p}{2} \left( V_{DD} - V_{inSP} - V_{thp} \right)^2$$

But: There is a difference in the number of involved switching transistors for the different input cases!

### Common Equation for CMOS-Inverter:

$$\frac{\beta_n}{2} (V_{inSP} - V_{thn})^2 = \frac{\beta_p}{2} (V_{DD} - V_{inS} - V_{thp})^2$$

Dissolve for *V*<sub>inSP</sub>:

$$\sqrt{\beta_n} (V_{inSP} - V_{thn}) = \sqrt{\beta_p} (V_{DD} - V_{inSP} - V_{thp})$$

$$V_{inSP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{thn} + V_{DD} - V_{thp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \longrightarrow$$





Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology Inverter, 2-Input-NAND, 2-Input-NOR



$$\frac{\left[\frac{W}{L}\right]_{n}}{\left[\frac{W}{L}\right]_{p}} = \frac{4}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}}\right)^{2} = \frac{4}{3} \left(\frac{1.65 - 0.7}{1.65 - 0.5}\right)^{2} = 0.908 \qquad \qquad \frac{\left[\frac{W}{L}\right]_{p}}{\left[\frac{W}{L}\right]_{n}} = 1.1$$

# Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology 2-Input-NAND, 2-Input-NOR

$$\frac{\beta_n}{2}(V_{inSP} - V_{thn})^2 = \frac{\beta_p}{2} \left( V_{DD} - V_{inSP} - V_{thp} \right)^2$$
$$\sqrt{\beta_n}(V_{inSP} - V_{thn}) = \sqrt{\beta_p} \left( V_{DD} - V_{inSP} - V_{thp} \right)$$

Lower transistor in NAND during switching phase:

One p-transistor is off and remains off. One n-Transistor is on and remains on. Only an inverter is switching.

See if the values are acceptable with regard to noise margin. Try to change W/L ratios to find a compromise.

For 
$$V_{inSP} = \frac{V_{DD}}{2}$$
  
 $\beta_{nges} = KPN \cdot \frac{W}{L}$   
 $\beta_{pges} = KPN \cdot \frac{W}{L}$   
 $KPN = 3 \cdot KPP$   

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_n} = \frac{1}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thn} - V_{DS11}}{\frac{V_{DD}}{2} - V_{thp}}\right)^2$$

 $\frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot (V_{thn} + V_{DS11}) + V_{thn_B} - V_{thp}}{1 + \frac{\beta_n}{\beta_n}}$ 

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1.65 - 0.7}{1.65 - 0.5 - 0.236}\right)^2 = 0.36 \qquad \qquad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 2.78$$
$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1.65 - 0.7}{1.65 - 0.5}\right)^2 = 0.23 \qquad \qquad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 4.44$$

Interesting, but we can implement one geometry only and must configure a compromise.

 $U_{eS} =$ 

IGS / Uni-Rostock

# Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology 2-Input-NAND, 2-Input-NOR



 $= \frac{\sqrt{\frac{3}{1.1}} \cdot 0.5V + 3.3V - 0.7V}{1 + \sqrt{\frac{3}{1.1}}} = 1.29V$  $V_{inSPu} = \frac{\sqrt{\frac{3}{1.1}} \cdot 0.5V + 3.3V - 0.7V}{1 + \sqrt{\frac{3}{1.1}}} = 1.29 V$ witching both tion = 1.1:  $\left[\frac{W}{L}\right]_{p} / \left[\frac{W}{L}\right]_{n} \qquad V_{inSPo} = \frac{\sqrt{\frac{3}{1.1}} \cdot 0.5V + 0.236V + 3.3V - 0.7V}{1 + \sqrt{\frac{3}{1.1}}} = 1.38 V$ 

KPN/KPP

Not considered:

Conducting NMOS has a resistance ( $U_{DS} > 0$ ) Body-/Backgate-Effect ( $U_{Th}$  dependent of subtrate voltage)

<sup>W</sup> / <sub>L</sub> – RelationPMOS/NMOS	$V_{inSP}$ when switching both inputs [Volts] and difference to $V_{DD}$	$V_{inSP}$ only "upper NMOS" switching [Volts] and difference to $V_{DD}$	$V_{inSP}$ only "lower NMOS" switching [Volts] and difference to $V_{DD}$
1.1	1.65 / 1.65	1.36 / 1.94	1.30 / 2.00
2.2	1.83 / 1.47	1.55 / 1.75	1.47 / 1.83
3.3	1.92 / 1.38	1.66 / 1.64	1.58 / 1.72
4.4	1.98 / 1.32	1.74 / 1.56	1.66 / 1.64

Switching input voltage  $V_{inSP}$  for different W/L - relations of the transistors from Simulation

# Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology 2-Input-NAND, 2-Input-NOR

### Practical hint to safe time:

Starting from the inverter schematic:

You may open the inverter schematic as the origin for the new design.

Then create a new schematic cellview (from CDW or Library Manager). File -> New -> Cellview

When you have the new empty schematic and the inverter schematic side by side you can copy the inverter circuit or parts of it to the new schematic.

Use copy: "c" -> select the desired part using the left mouse button

- -> click on the selected part
- -> drag to the new place (may be the same schematic window or the new one)

Copy object from one schematic window to another: In target no command should be active! (Use ESC sometimes!)

Edit the new schematic to build the NAND or NOR design.

You may proceed in the same manner for the testbench.

#### "modp" ng=2 l=0,35u "modp" ng=2 l=0.35u wtot=2u L=0.35 μ W=2 μ wtot=2 MP22 MP21 MN1-Z vtot= \u l=0.35u ng=1 ".modn" MN11 în 1 out in2 mandZr wtot=1u l=0 35u ng=1 modn" L=0.35 µ W=1 µ out în2 nand2 gnd o\_both în 1 is a site out in2 · · · mand2· ٧1 V V1:0 vde=3.3 acm=1 v2=3.3 tr-1Øp CØ C2 CS R1. c=8Øf r=1Meg -c=8Øf gnd

# 2-input-NAND Schematic and associated Testbench

# 2-Input-NAND, 2-Input-NOR – Use steps as before in inverter simulation

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		→ →	◯ pac
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	6		◯ qpxf ◯ qpsp ◯ hb ◯ hbac
			hbnoise
	Outputs ?  X	4	DC Analysis
	Name/signal/expr value Plot Save Save Options		Save DC Operating Point
			Hysteresis Sweep
			Sweep Variable
			Temperature
			Design Variable
			Model Parameter Parameter Name dc
3(5) Load State	Status: Ready T=27 C Simulator: spectre		
			Sweep Range
ADE XL Test	Editor - test:nand2test:1		Start-Stop
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P 🖓 🎦 27			Sweep Type
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Name Value	1 dc 0 3.3 10m Linear Step Size Start-Stop /V1 약당	Create/Edit analyses	O Number of Steps
		Design variables	Add Specific Points
		Simulation Outputs	
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	Name/Signal/Expr Value Plot Save Save Options	Run enabled analyses	adtomatic, inical, logarithmic
		Stop 🥆	OK Cancel Defaults Apply Help
		Plot	Select Component Parameter
>		Plot	dc vdc '00 voltage' mag v acm 'AC magnitude' bbaa soo '40 bbaa
2(5) Plat Outputs	Status Postul T-17, C   Simulator motiva		type arClype "Source type" edgetype edgetype "Type of rising & falling edg
3(5) Piot Outputs	Status: Ready 1=27 C Simulator: spectre		xfmag xXfm "XF magnitude" pacmag pacm "PAC magnitude" pacpase pacp "PAC phase"
			val0 v1 "Voltage 1" val1 v2 "Voltage 2" period per "Period"
			delay td "Delaytine" rise tr "Rise time"
			Tall tf "Palltume" width pw "Pulse width" tol tol "Temperature coefficient 1"
			tc2 tc2 "Temperature coefficient 2" tnom tnom "Nominal temperature"
47.42.2040			
17.12.2018		IGS / Uni-Rostock	

# 2-Input-NAND, 2-Input-NOR – Use steps as before in inverter simulation

ADE L (1) - test invertertest schematic	
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help	cādence
📥 🔊   🧊 27   🔊 🎾 🖄 🗹 🗁	
Design Variables       Analyses         Name       Value         1 dc       © 0 3.3 10m Linear Step Size Start-St         0 utputs       Outputs         Name/Signal/Expr       Value	2 P /V0 P /V0
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	Apply Help

Transfer characteristics and noise margin for 2-Input-CMOS-NAND-Gate



## Transfer characteristic for 2-Input-CMOS-NAND-Gates



Transfer characteristics of 2-input-NAND-Gates

from AMS-0.35µ-library with  $L_{NMOS,PMOS} = 0.35\mu$ ,  $W_{NMOS} = 1.325\mu$ ,  $W_{PMOS} = 2.1\mu$  and

self-made gate with  $L_{NMOS,PMOS} = 0.35\mu$ ,  $W_{NMOS} = 1.0\mu$ ,  $W_{PMOS} = 1.6\mu$ 

(Characteristics for switching top N-transistor only not shown, always between bottom and both cases)



### 4-Input-NAND-Gate from AMS-0.35µ-library



Transfer characteristic of 4-input-NAND-Gate from AMS-0.35 $\mu$ -library with  $L_{NMOS,PMOS} = 0.35 \mu W_{NMOS} = 1.05 \mu, W_{PMOS} = 1.4 \mu$ Leftmost line for switching lowest (nearest to ground )nmos-transistor only, rightmost line for all 4 inputs switched simultaneously

## Cadence Transfer Library Content to a new Library

Use Cadence tools always! DO NOT copy in linux.

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