Cadence + AMS-Hitkit

Tutorial for creation of an inverter cell from schematic to layout with CADENCE using AMS-Hitkit and hints for multi-input gates

1. Using the Linux (CentOS) environment
2. Starting CADENCE with AMS-Hitkit
3. Creating a new library
4. Schematic entry
5. Creating a symbol and a testbench
6. Spice-Simulation using ADE XL
   - Analyses selection and setup
   - Using global variables
   - Parametric simulation
7. Starting Layout XL
   - Generate layout from schematic
   - The layer window
   - Wires, vias/contacts, wells
8. Design rule check
9. Layout versus schematic check (LVS)
10. Parasitic extraction (QRC)
11. Simulation of the extracted model (Post-layout simulation)

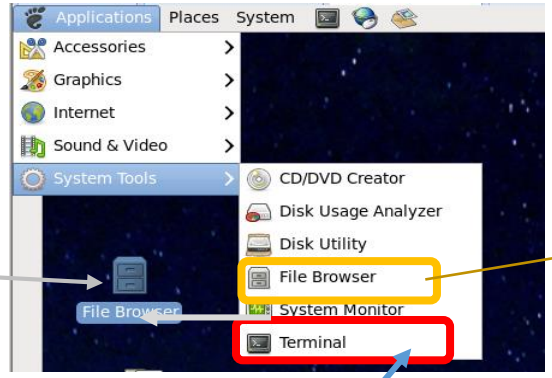
Some UNIX-commands

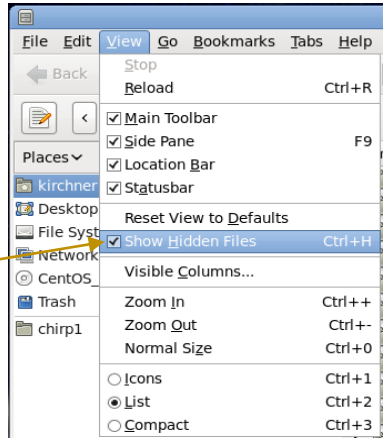
We use CentOS-Linux (Free version "**C**ommunity **Ent**erprise **OS**" of RedHat), because Cadence supports RedHat or Suse.
We use the KornShell (ksh), because it is the standard shell at ITMZ Uni Rostock.

Our client computers use the "supported" CentOS 7, binary compatible to RedHat 7.5

pwd	print working directory
ls, ls –alsi, ls *dir*	list
cd -> cd /~/ske -> cd ./ske	change directory
mkdir *newdir*	make directory
cp , cp -r, cp -p	copy files/directories (recursive, preserve attributes)
mv	move or rename directories
chmod, chmod –R chmod 744 *file*	change file mode bits (security) -> -R recursive
grep	filter for pattern
use of | for pipeline -> ls | grep *pattern*	use command output as input for next command
rm, rm –r	remove/delete
rmdir	remove directory
cat file	show file at standard output
man *cmd*	show manual of cmd
history, h	show command history
r 100	run command number 100 from history

Move icon to desktop for easy use





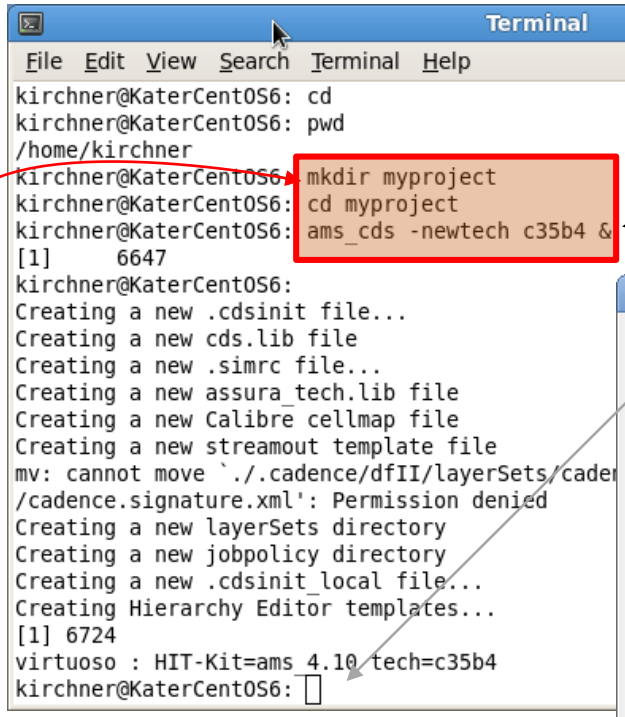
Or Right-Mouse on Background and select "Open Terminal"

To save windows images (.png) : Alt-Print

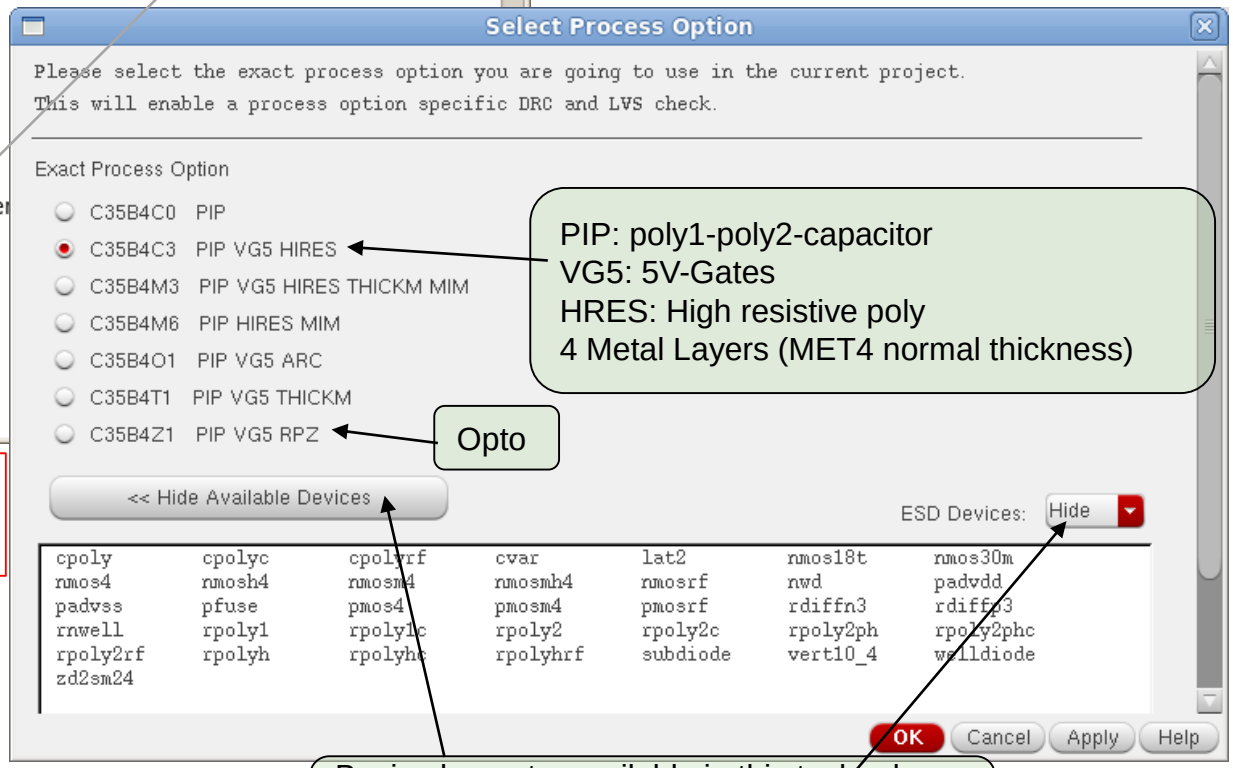
Unix-command to remove Cadence lock files (Close all Cadence programs before!) : **find ~/ -name "*.cdslck" -exec rm {} \;**

AMS-HitKit - Start

= Starting Cadence Design Framework with Libraries, Rules, Scripts provided for AMS-technology



First start !
Later use "ams_cds" simply!
(or "ams_cds &" to release the terminal for further use)



PIP: poly1-poly2-capacitor
VG5: 5V-Gates
HRES: High resistive poly
4 Metal Layers (MET4 normal thickness)

Opto

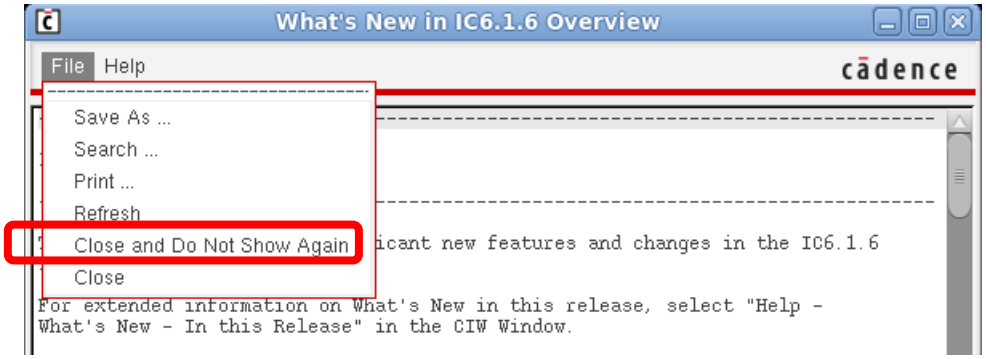
Do not use your homedir!
Create a separate project directory!

Make your favourite directory structure
~/ske
~/ske/inverter

Basic elements, available in this technology
Show additional elements for ESD
Electro**S**tatic **D**ischarge

You may use one single directory for different designs.

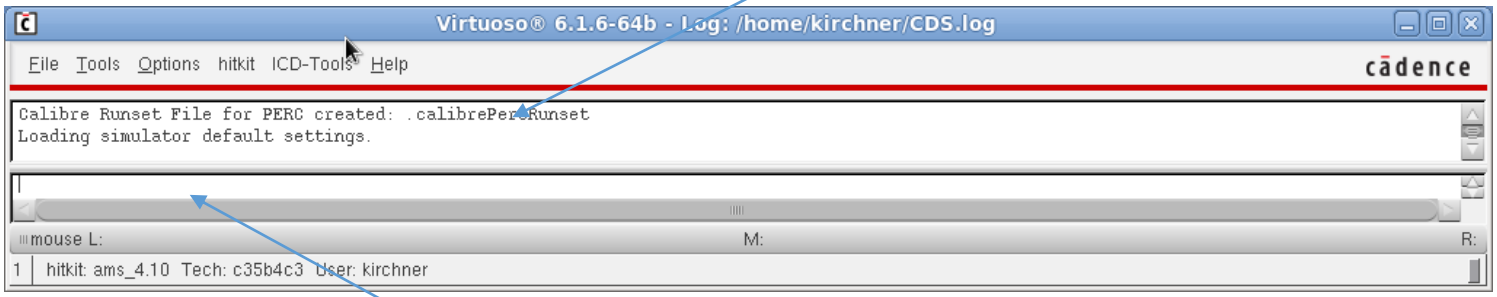
AMS-HitKit - Start



Would stay open as long as ams_cds is running

Windows open for some seconds after ams_cds start

Command Interpreter Window - CIW



Messages

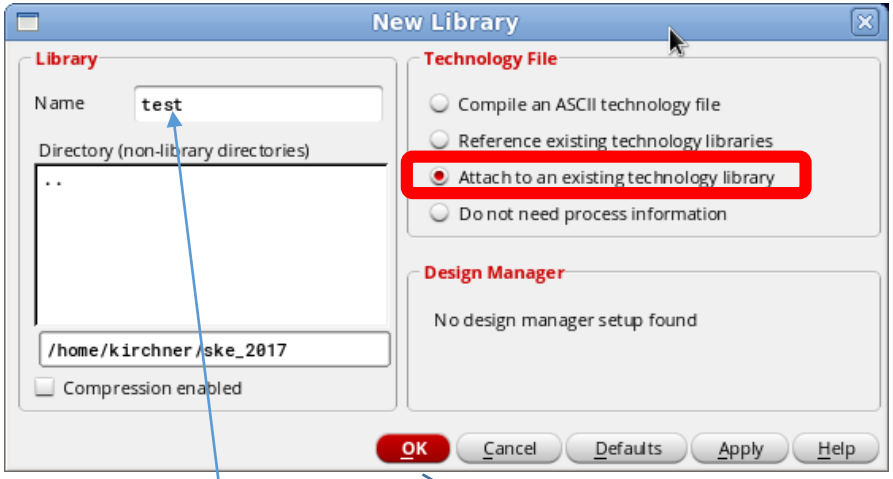
Command Inputs

AMS-HitKit - A new library

Command Interpreter Window - CIW

It is possible to create the library using the LIbrary Manager instead of CIW as well. The flow will differ (windows sequence).

File -> New -> Library

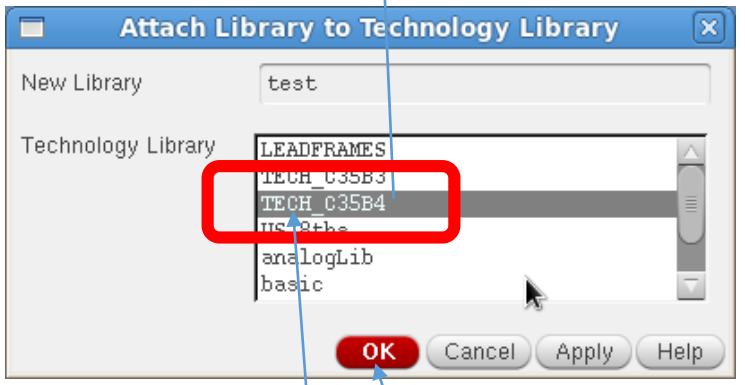


Choose a name for your library!
(You may use one library for different designs.)

Select
"Attach to an existing technology library" -> OK

important step!

If we skip this step, we will not see any elements for layout later

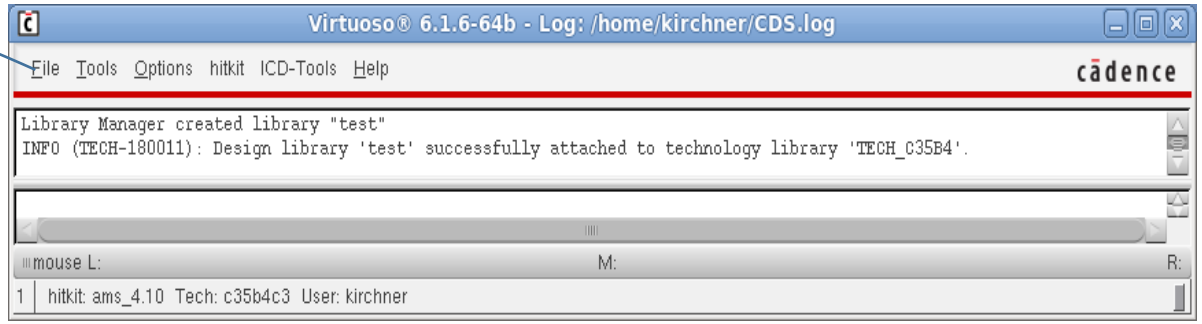


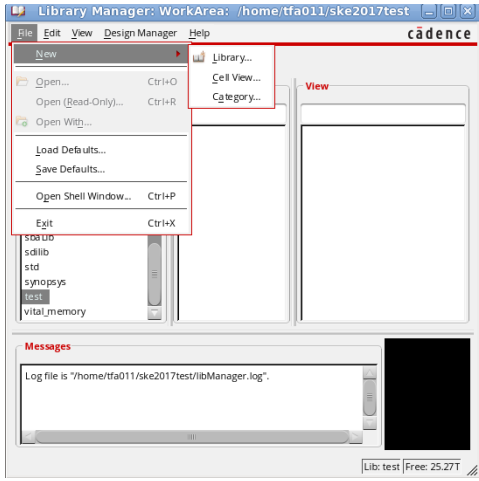
We use the 4 metal layer technology here.
Do not press OK before you have selected the TECH-library!

Quit with OK!

AMS-HitKit - A new cellview

Command Interpreter Window CIW (You can do this in the Library Manager as well)



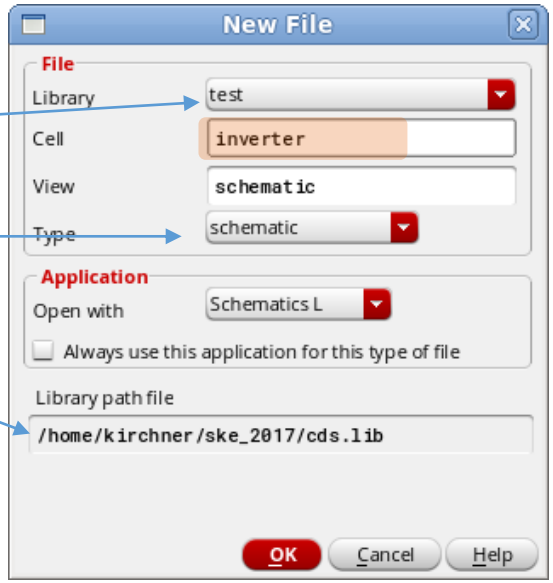


File -> New -> Cellview

Your new library

Start with schematic view

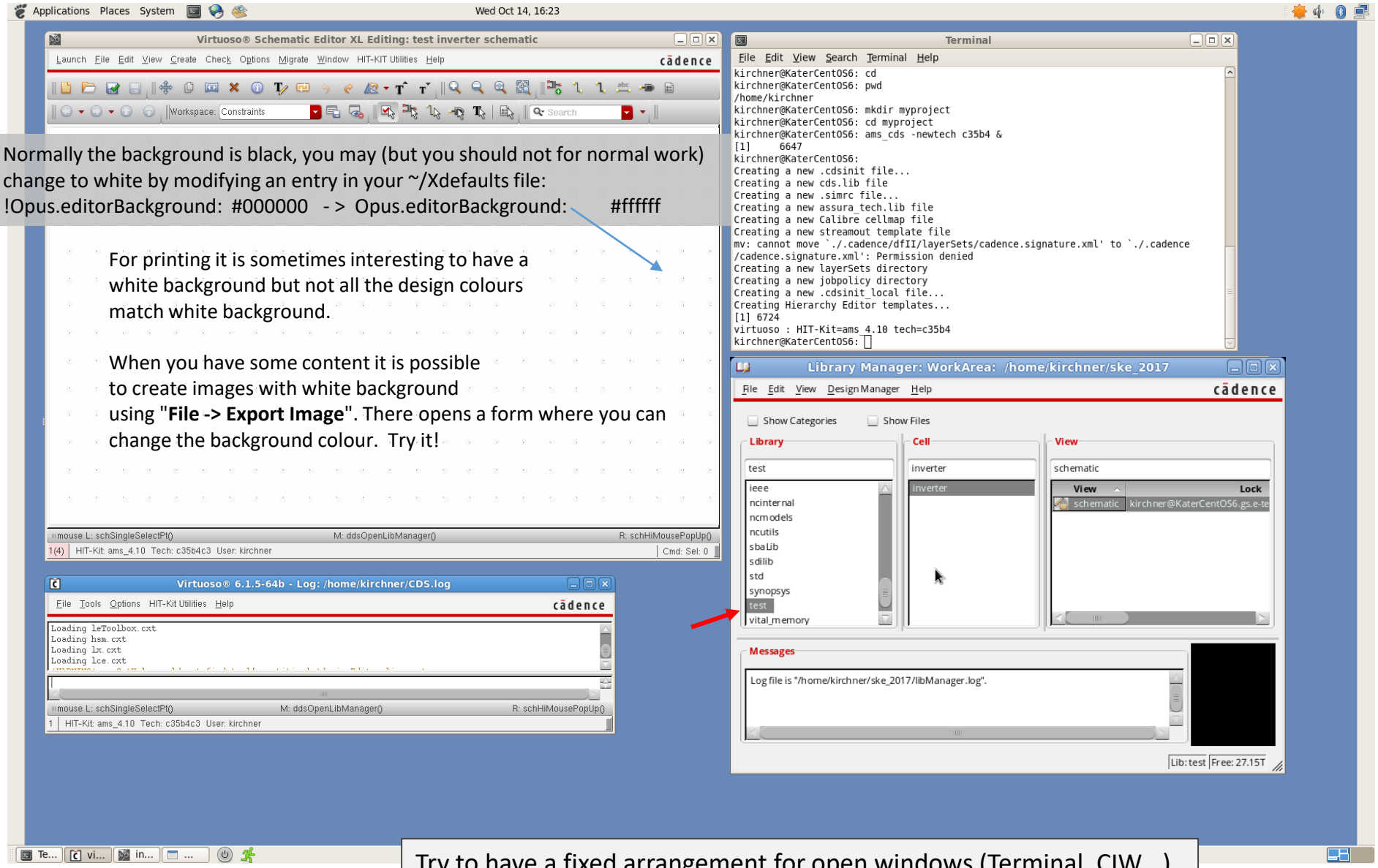
Depends on your project path



Choose a cell name, check "schematic" as cellview -> OK Quit with OK !

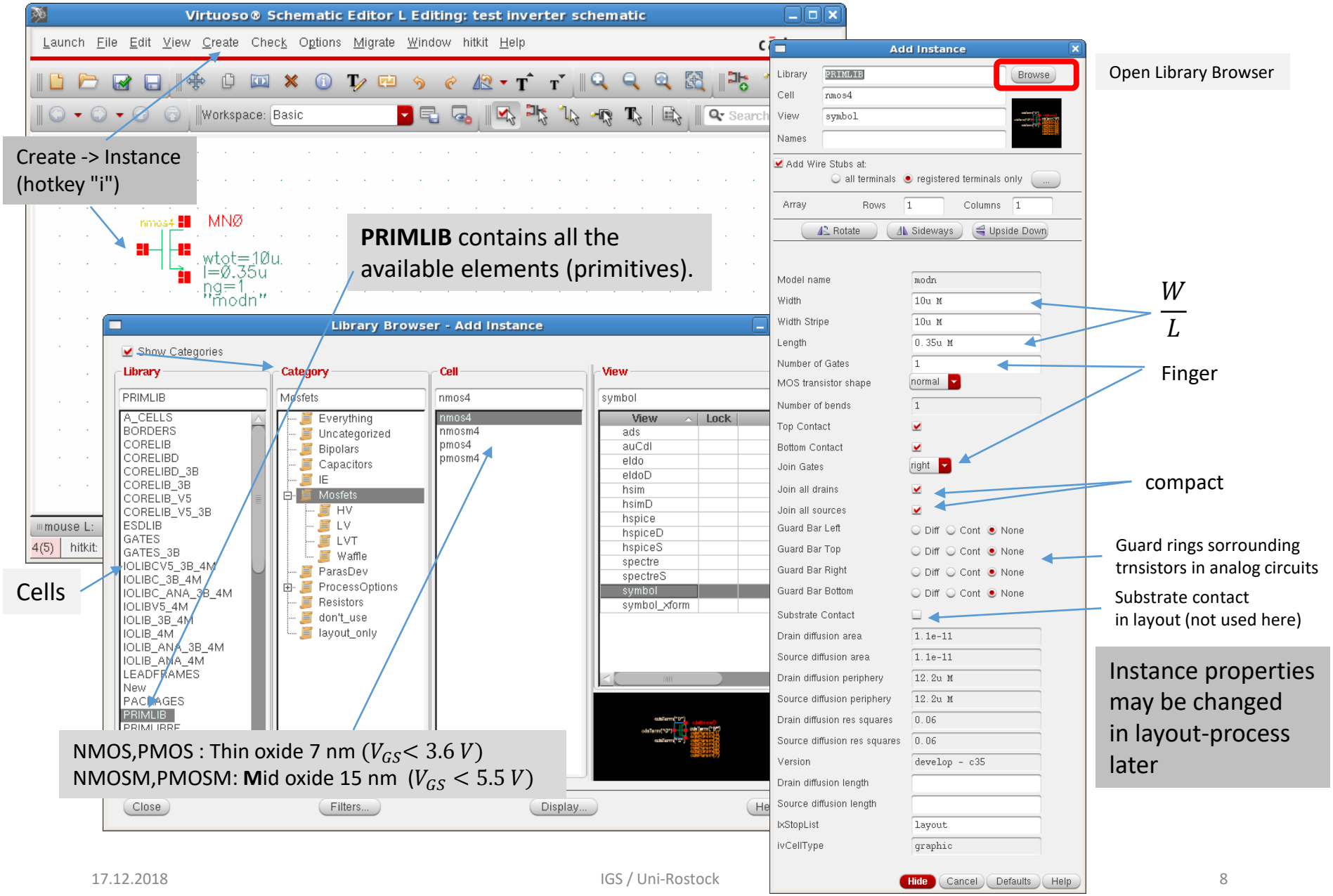
Best choice for names/identifiers: use letters, numbers, underscore only

AMS-HitKit Schematic Editor is open

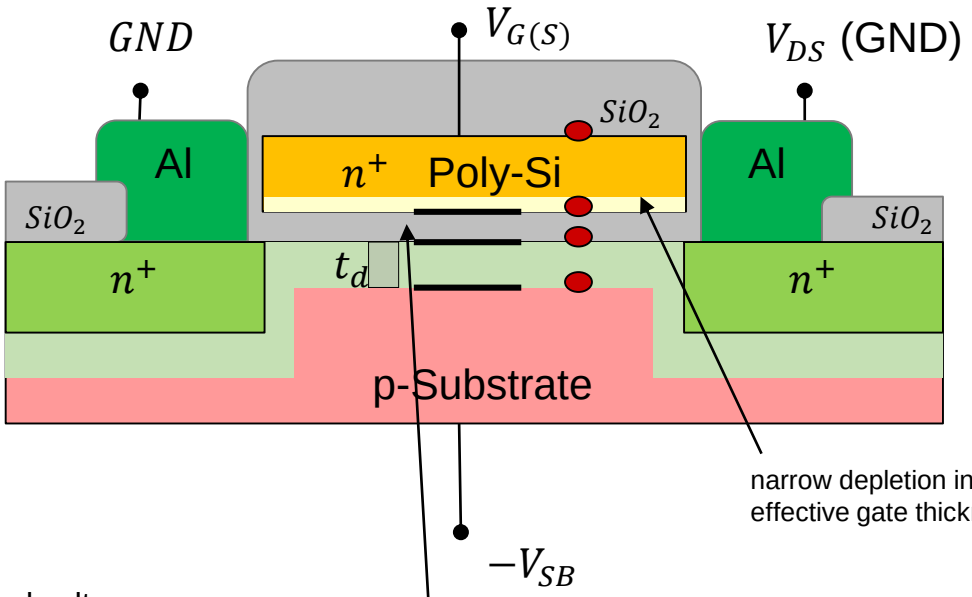


Try to have a fixed arrangement for open windows (Terminal, CIW ..)

Schematic entry - Components



MOSFET: Threshold Voltage



$$\Phi_{F\ gate} = \frac{kT}{e} ln \frac{N_{Dpoly}}{n_i}$$

Remember that the gate is used as the mask for the doping process making source and drain (self alignment)

$$\Phi_{F\ substr} = V_{fp} = -\frac{kT}{e} ln \frac{N_{Asubstr}}{n_i}$$

narrow depletion in heavely doped gate
effective gate thickness increases

flatband voltage

$$V_{fb} = (V_G - V_{OX}) + (V_{OX} - V_{fp}) = V_G - V_{fp} = \frac{kT}{e} ln \frac{N_{Dpoly}}{n_i} + \frac{kT}{e} ln \frac{N_{ASubstr}}{n_i} = \frac{kT}{e} ln \frac{N_{Dpoly} \cdot N_{ASubstr}}{n_i}$$

inversion voltage

Voltage necessary to achieve channel inversion
2x the potential in the depletion area
(from p-conduction to zero to n-conduction)

contact voltage(s))

$$V_{TH} = \frac{Q'_b - Q'_{SS}}{C'_{OX}} - 2V_{fp} - V_{contact}$$

Voltage over gate oxide (observe that the charge quantity on gate is equal to bulk $Q_g = -Q_b$)

MOSFET: Threshold Voltage

inversion voltage

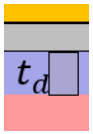
$$V_{TH} = \frac{Q'_b - Q'_{SS}}{C'_{OX}} - 2V_{fb} - V_c$$

contact voltage(s)

voltage over gate oxide

Compare with pn-junction, but here one side weakly doped: $u_i < 2 \cdot 300mV$

charge on gate = - charge on substrate



Charge per area in channel volume element

$$Q'_{b0} = eN_A t_d = eN_A \sqrt{\frac{2\varepsilon_{Si} \cdot |V_G - v_{fb}|}{e \cdot N_A}} = \sqrt{2eN_A\varepsilon_{Si} \cdot |-2\, v_{fb}|}$$

without bulk voltage

$V_G = -v_{fb}$

Thickness of depletion area -> pn junction

$$t_d = \sqrt{\frac{2\varepsilon_{Si}|V_G - v_{fb}|}{e \cdot N_A}}$$

$$Q'_b = eN_A D_d = eN_A \sqrt{\frac{2\varepsilon_{Si} \cdot |V_S - v_{fb}|}{e \cdot N_A}} = \sqrt{2eN_A\varepsilon_{Si} \cdot |-2v_i + V_{SB}|}$$

with bulk voltage

$$\frac{Q'_b - Q'_{SS}}{C'_{OX}} = \frac{Q'_{b0} - Q'_{SS}}{C'_{OX}} - \frac{Q'_{b0} - Q'_b}{C'_{OX}}$$

made to define a fixed part and a V_{SB}-dependent part

$$V_{TH} = -2V_{fb} - V_c + \frac{Q'_{b0} - Q'_{SS}}{C'_{OX}} - \frac{Q'_{b0} - Q'_b}{C'_{OX}} = -2V_{fb} - V_c + \frac{Q'_{b0} - Q'_{SS}}{C'_{OX}} + \frac{\sqrt{2eN_A\varepsilon_{Si}}}{C'_{OX}}\left(\sqrt{|-2v_{fb} + V_{SB}|} - \sqrt{|-2v_{fb}|}\right)$$

MOSFET: Threshold Voltage

$-2v_{fp}$

surface potential

does not depend on V_{SB}

contact voltage

$$V_{TH} = -2v_{fb} - V_c + \frac{Q'_{b0} - Q'_{SS}}{C'_{OX}} + \frac{\sqrt{2eN_A\varepsilon_{Si}}}{C'_{OX}}\left(\sqrt{|-2v_{fp} + V_{SB}|} - \sqrt{|-2v_{fp}|}\right)$$

γ – body effect parameterr

$$V_{TH} = -2V_{fp} - V_c - \frac{Q'_{SS}}{C'_{OX}} + \frac{Q'_{b0}}{C'_{OX}} + \gamma\left(\sqrt{|-2v_{fp} + V_{SB}|} - \sqrt{|-2v_{fp}|}\right)$$

$$V_{TH} = -V_c - \frac{Q'_{SS}}{C'_{OX}} - 2v_{fb} + \frac{Q'_{b0}}{C'_{OX}} + \gamma\left(\sqrt{|-2v_{fp} + V_{SB}|} - \sqrt{|-2v_{fp}|}\right)$$

V_{FB}- Flat Band Voltage

$\sqrt{2eN_A\varepsilon_{Si} \cdot |-2\,v_{fp}|}$

$$V_{TH} = V_{FB} - 2v_{fp} + \frac{Q'_{b0}}{C'_{OX}} + \gamma\left(\sqrt{|-2v_{fp} + V_{SB}|} - \sqrt{|-2v_{fp}|}\right)$$

$$V_{TH} = V_{GS0} = V_{TH0} + \gamma\left(\sqrt{|-2v_{fp} + V_{SB}|} - \sqrt{|-2v_{fp}|}\right)$$

Q'_{b0} – charge per (top) area under gate oxide in length ΔL

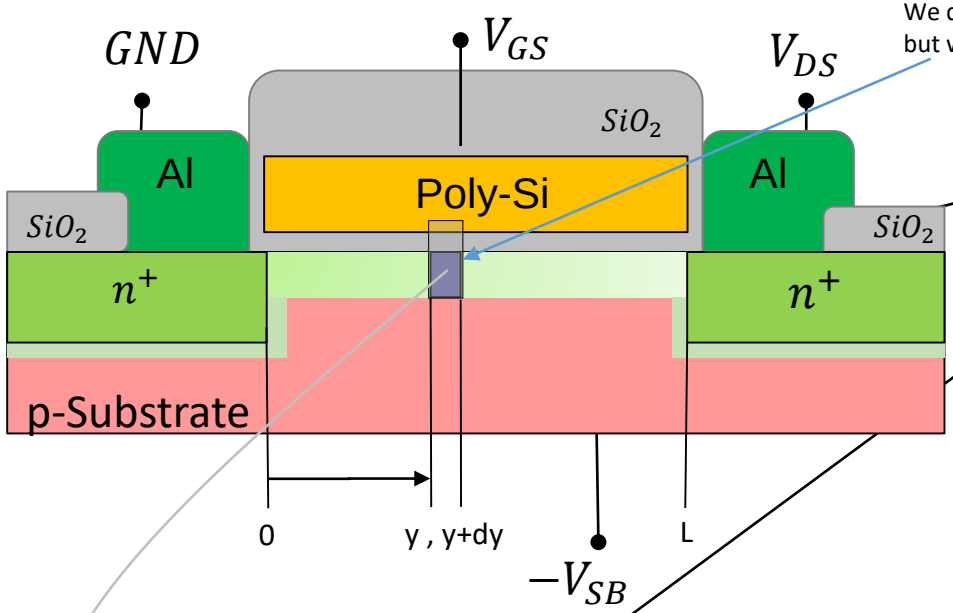
Q'_{SS}–charge stacked at surface

V_{TH} depends on:

substrate doping Q'_{b0} (used for adjustment)
steep retrograde doping (light at surface, strong in body)
thin channel, less dependent on V_{SB})

oxide thickness (some nm, 2..20)
substrate voltage (consider transistor location in circuit relative to GND/VCC)
gate material (metal, n+-Si, p+-Si)
surface charge density Q'_{SS}(Si, Na – ions)

MOSFET: Control Equation



We do not know the profile of the channel in advance but we can evaluate the conditions in a small volume

$$Q'(y) = C'_{OX}(V_{GS} - V(y) - V_{th})$$

Charge of gate capacitor per area $\Delta y \cdot W$

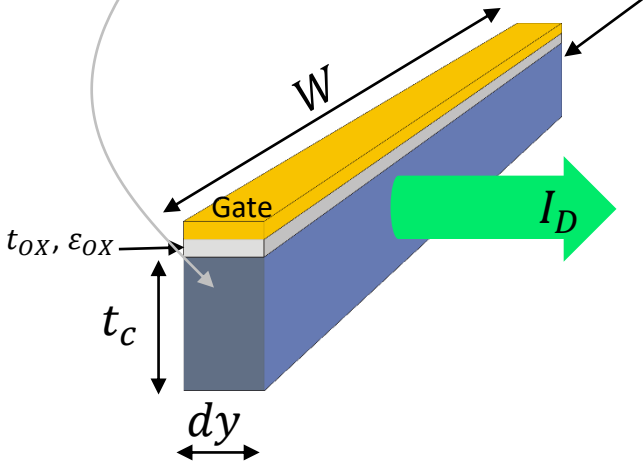
$$\rho = \frac{1}{e \cdot n \cdot \mu} = \frac{1}{\frac{Q'(y)}{t_c} \cdot \mu}$$

Charge in volume $\Delta y \cdot W \cdot t_c$

$$r_\square = \frac{\rho}{t_c} = \frac{1}{\mu \cdot Q'(y)}$$

$$dR = \frac{1}{\mu_n Q'(y)} \cdot \frac{dy}{W}$$

$$dV(y) = I_D \cdot dR = \frac{I_D}{W \cdot \mu_n Q'(y)} \cdot dy \qquad (I_D \text{ over } r_\square)$$



$$I_D \cdot dy = W \cdot \mu_n \cdot C'_{OX}(V_{GS} - V(y) - V_{th})dV(y)$$

$$\mu_n \cdot C'_{OX} = \mu_n \cdot \frac{\varepsilon_{OX}}{t_{OX}} = KP_n$$

Effective mobility in inverted channel less than mobility in table for n-Si : 450 vs. 1650 $\frac{cm^2}{Vs}$

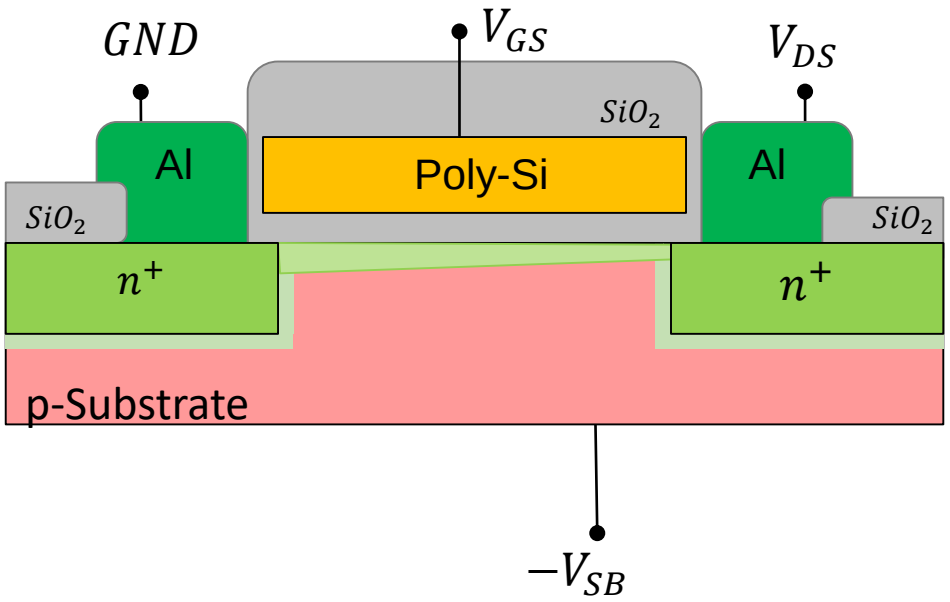
$$I_D \cdot dy = W \cdot KP_n \cdot (V_{GS} - V(y) - V_{th})dV(y)$$

MOSFET: Control Equation, non pinched off

$$I_D \cdot dy = W \cdot KP_n \cdot (V_{GS} - V(y) - V_{th}) \cdot dV(y)$$

$$I_D \int_0^L dy = W \cdot KP_n \int_0^{V_{DS}} (V_{GS} - V_{th} - V(y)) \cdot dV(y)$$

$$I_D = \frac{W}{L} \cdot KP_n \cdot \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] = \beta \cdot \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

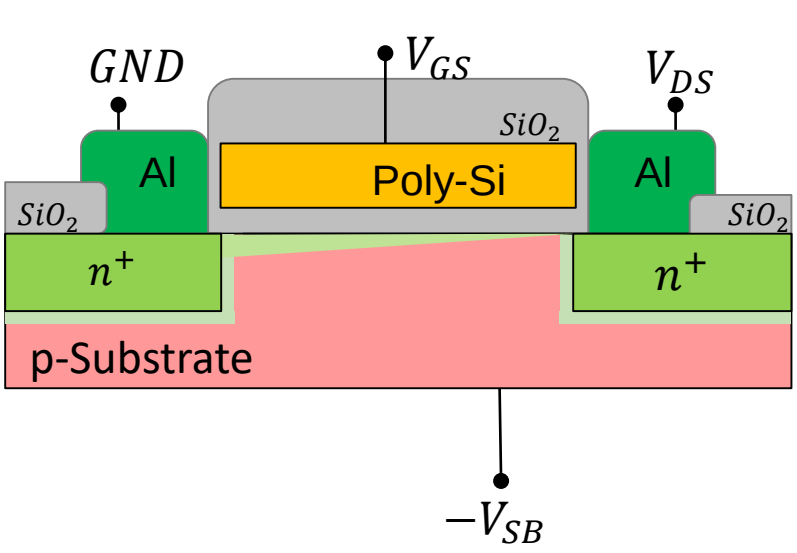


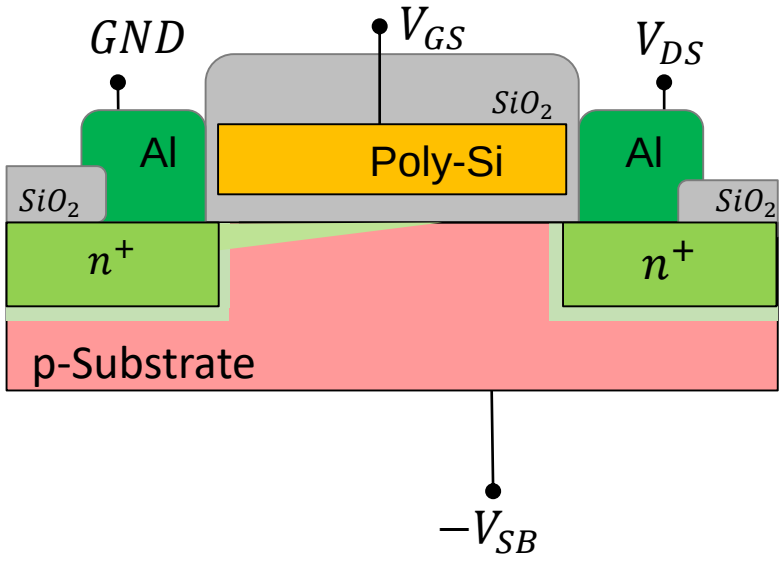
MOSFET: Control Equation, pinched off

$$I_D = \frac{W}{L} \cdot KP_n \cdot \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Pinch off when: $V_{GS} - V_{th} \leq V_{DS}$

$$I_D = \frac{W}{L} \cdot KP_n \cdot \frac{(V_{GS} - V_{th})^2}{2} = \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2$$



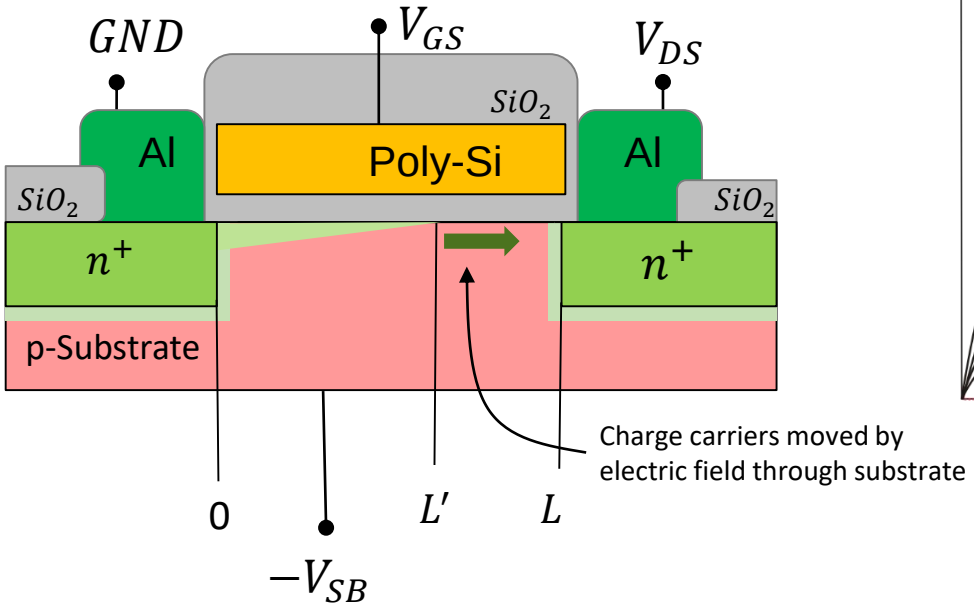


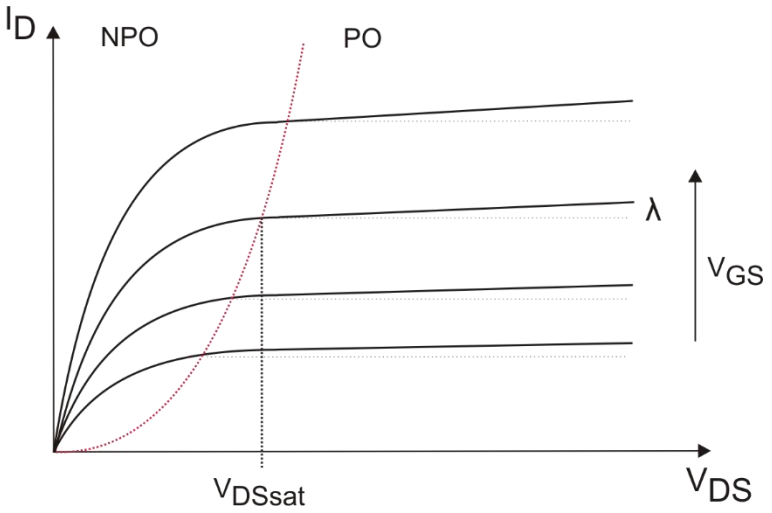
MOSFET: Control Equation, pinched off

$$I_D = \frac{W}{L} \cdot KP_n \cdot \frac{(V_{GS} - V_{th})^2}{2} = \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2$$

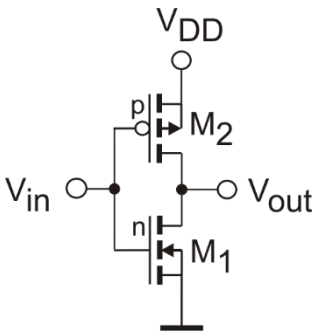
Channel-length modulation

$$I_D = \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2 \quad \rightarrow \frac{\beta}{2} \cdot (V_{GS} - V_{th})^2 \cdot [1 + \lambda \cdot (V_{DS} - V_{DSsat})]$$

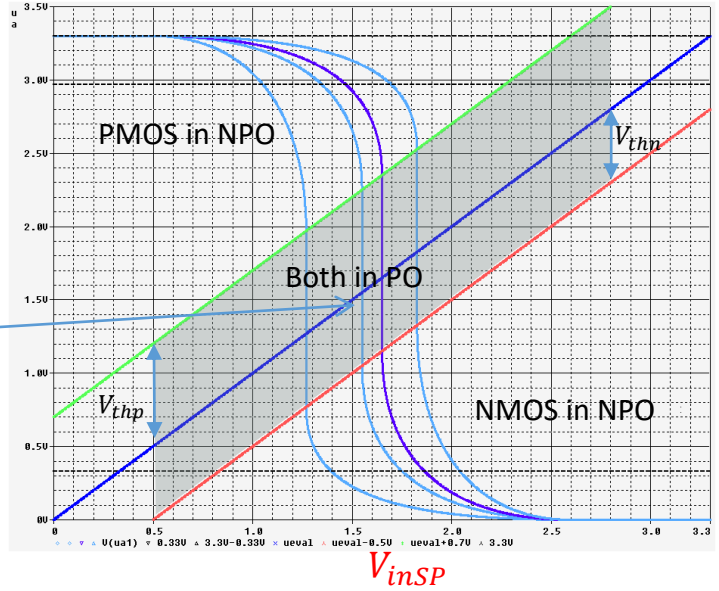




CMOS Inverter Calculation



There is the same current flowing through both transistors.Beide. For ideal switching point is $V_{in} = V_{GSn} = V_{SGp} = V_{out} = V_{DSn} = V_{SDp} = \frac{V_{DD}}{2}$.
Because of $|V_{DS}| > |V_{GS} - V_{th}|$ both transistors are in the pinch-off state and we can assume:



$$\frac{\beta_n}{2}(V_{inSP} - V_{thn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{inSP} - V_{thp})^2$$

$V_{thn} = 0.5\text{V}$, KPN $= 170\ \frac{\mu A}{V^2}$

$V_{thp} = 0.65\text{V}$, KPP $= 58\ \frac{\mu A}{V^2}$

Dissolving for V_{inSP}:

$$\sqrt{\beta_n}(V_{inSP} - V_{thn}) = \sqrt{\beta_p}(V_{DD} - V_{inSP} - V_{thp})$$

$$V_{inSP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{thn} + V_{DD} - V_{thp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

For desired $V_{inSP} = \frac{V_{DD}}{2}$ we calculate the relation $\frac{\beta_n}{\beta_p}$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - U_{thn}}\right)^2$$

$$\beta = KP \cdot \frac{W}{L}$$

using: $KPN = 3 \cdot KPP$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}}\right)^2 \approx \boxed{\frac{1}{3}}$$

for $|V_{DD}| \gg |V_{thp} - V_{thn}|$

Inverter schematic

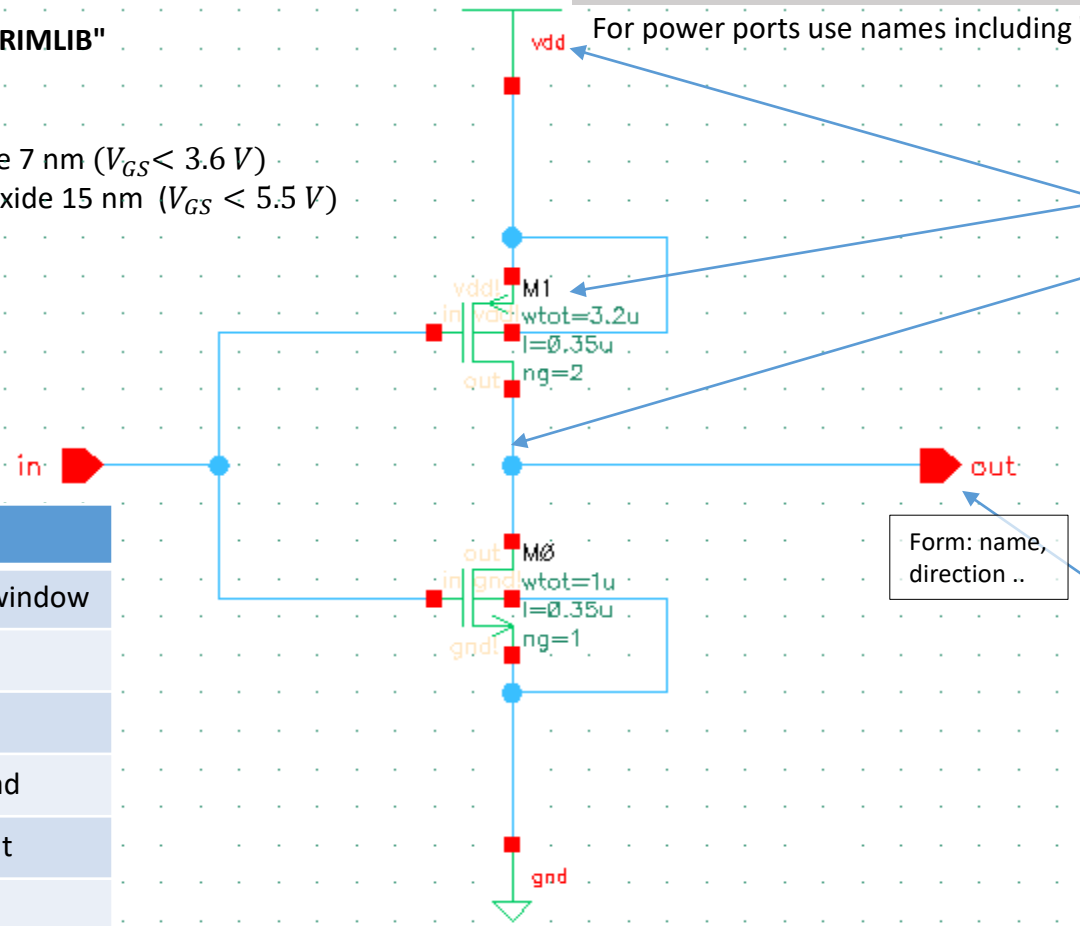
vdd, gnd etc. from library "**analogLib/**globals"

For power ports use names including "vdd" or "vcc"

tranistors from library "**PRIMLIB**"
(also **Design**-R,C,L)

NMOS,PMOS : Thin oxide 7 nm ($V_{GS} < 3.6\ V$)
NMOSM,PMOSM: Mid oxide 15 nm ($V_{GS} < 5.5\ V$)

no substrate contact for
the transistors in logic

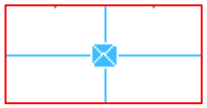


key	function
i	create instance
w	create wire
M	move
m	stretch (im Layout "S" !)
c	copy
q	object properties
p	add pin
l	add wire name (label)
x	check current cellview
f	fit
]	zoom in
[	zoom out

Form: name, direction ..

key	function
F3	show option window
u	undo
U	redo
e	descend & read
E	descend & edit
CTRL-e	return
DEL	delete

For ground ports use names including "gnd".
(Some scripts (ERC) need this naming convention.)

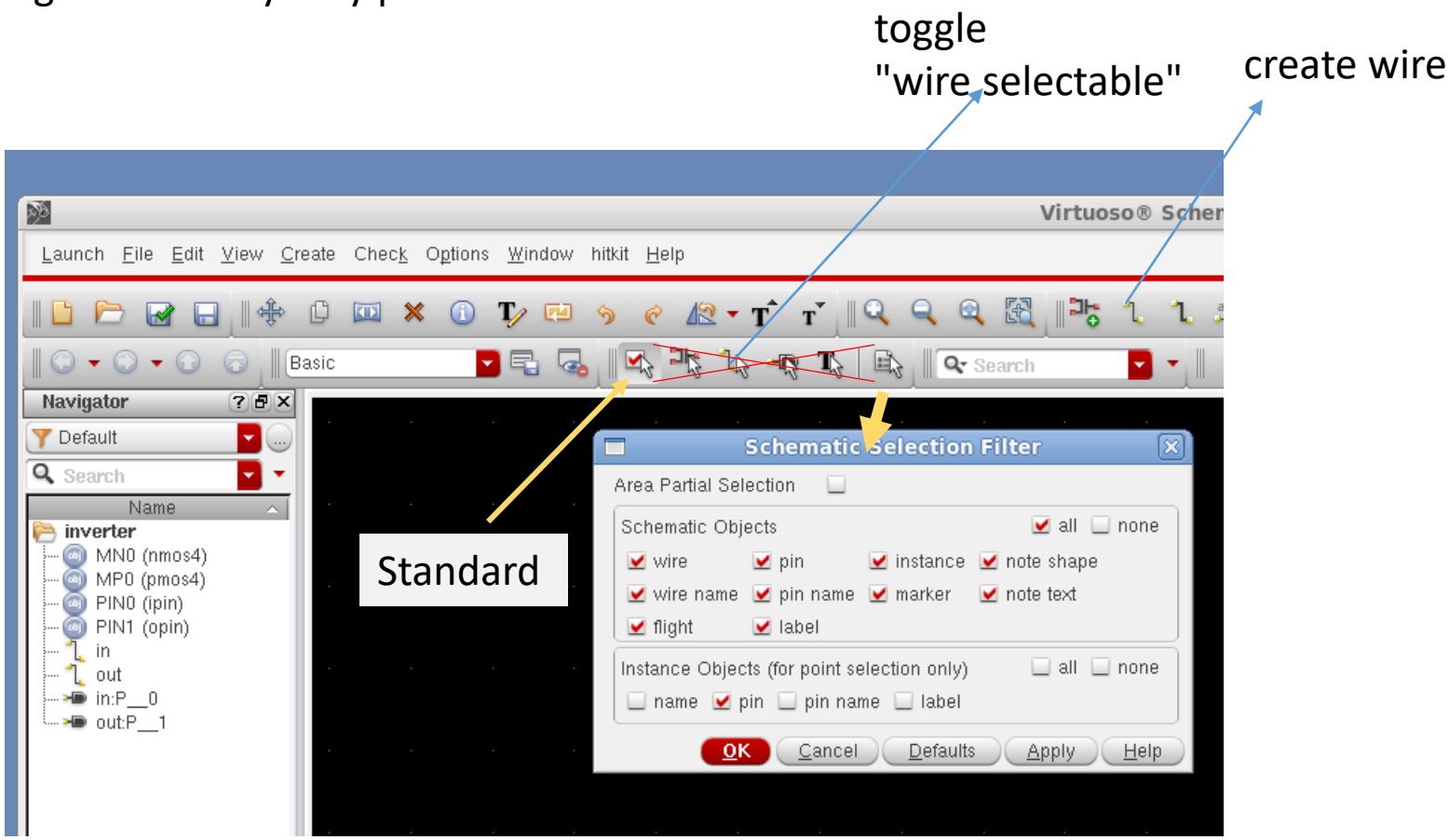


Avoid crossover dots.
Warnings! May be deselected
Check-> Rules-> Physical

File -> Check and Save (shft-x)

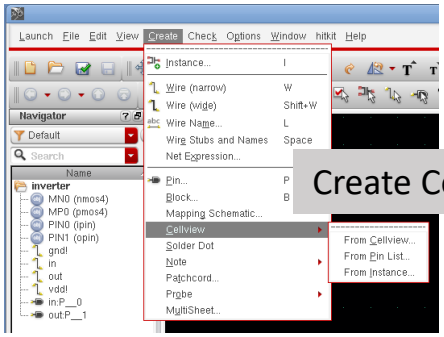
Schematic Editor: Filter

Schematic editor has a filter function for selectable objects!
Changing accidentally may prohibit selection!

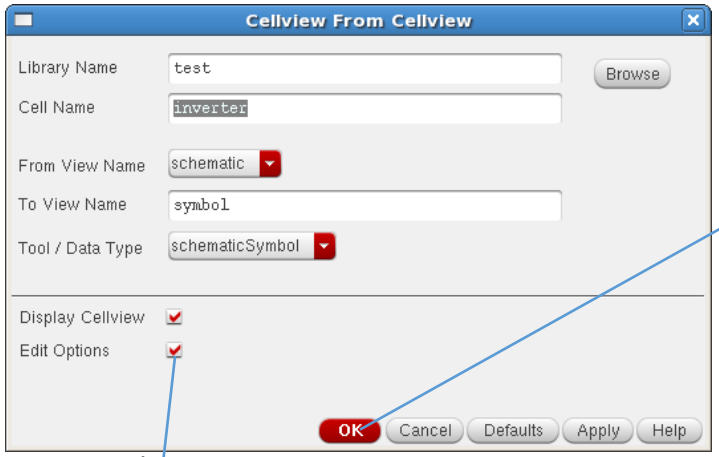


Inverter Symbol from Schematic

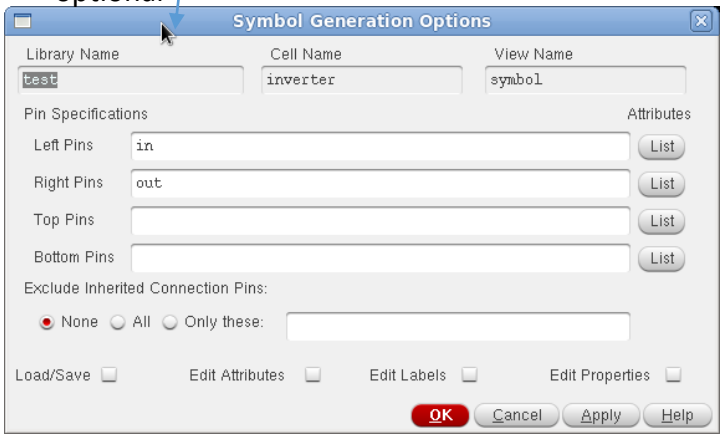
Symbol needed to use our design in higher levels of hierarchy.
First Example is the insertion of the design in a testbench.



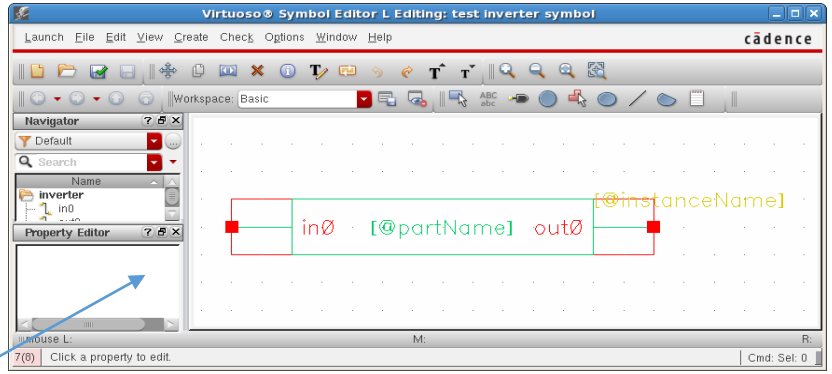
Create Cellview -> From Cellview -> OK



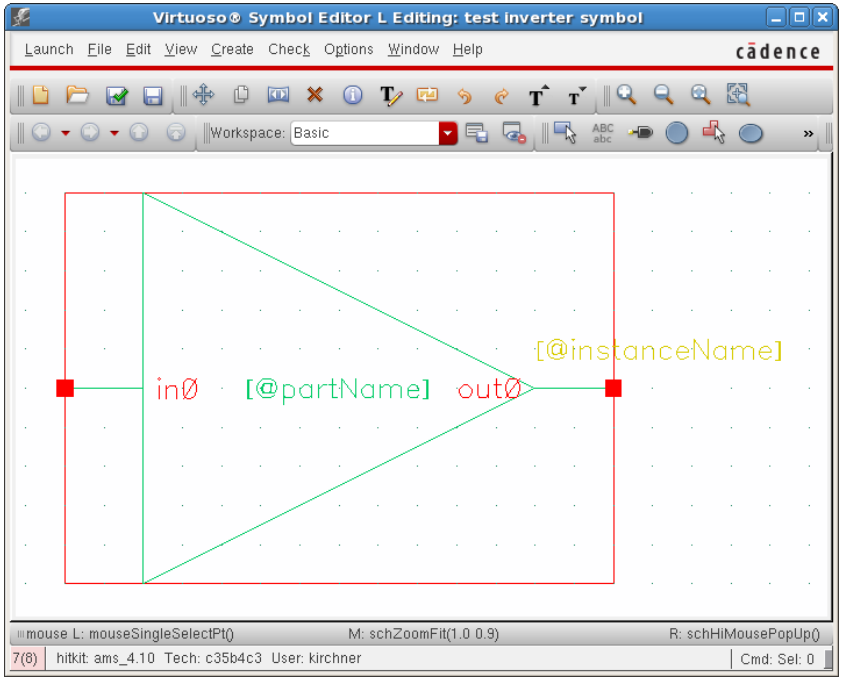
optional



Standard: rectangle

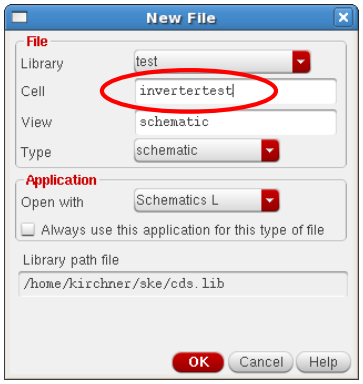


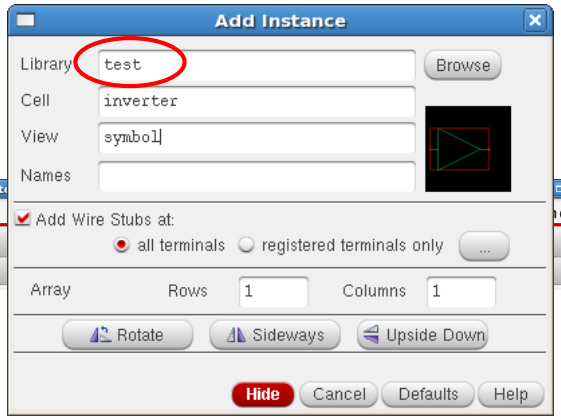
One may change shapes:
outline (green), selection frame (red)
use: stretch, delete,move,create polygon

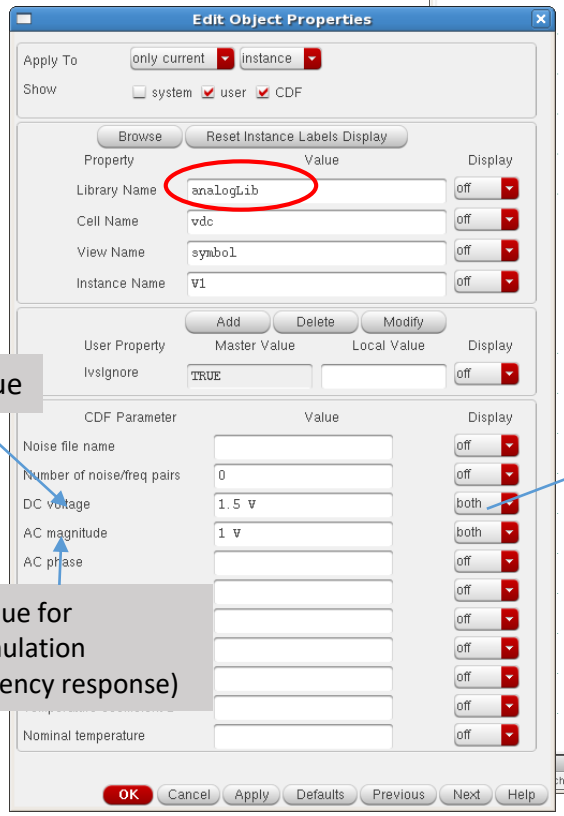


Inverter Schematic for Simulation -> Testbench

In CIW (or Library Manager): File -> New -> Cellview







DC-value

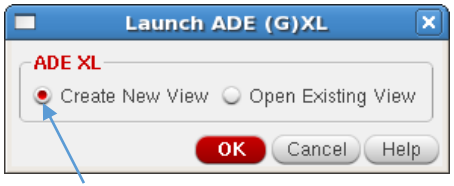
AC-value for ac-simulation (frequency response)

Simulation ADE GXL Start

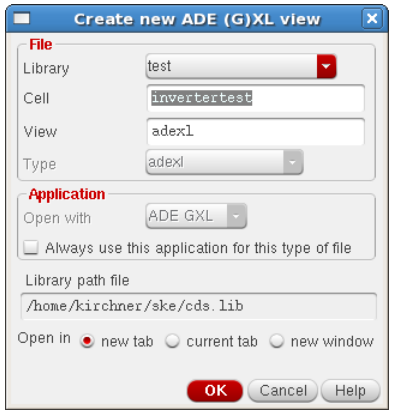
From the Schematic Editor -> **Launch -> ADE GXL**

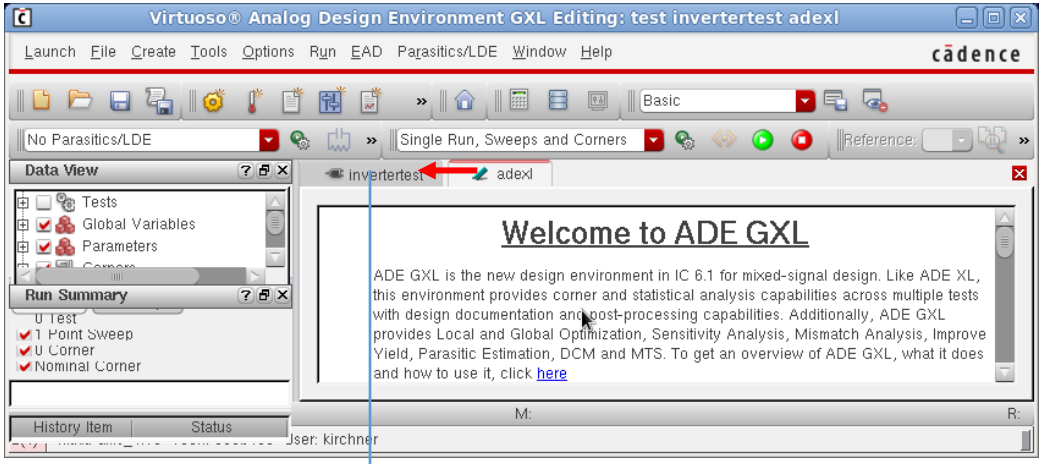
ADE (G)XL usage differs from ADE L
Most tutorials use older ADE L

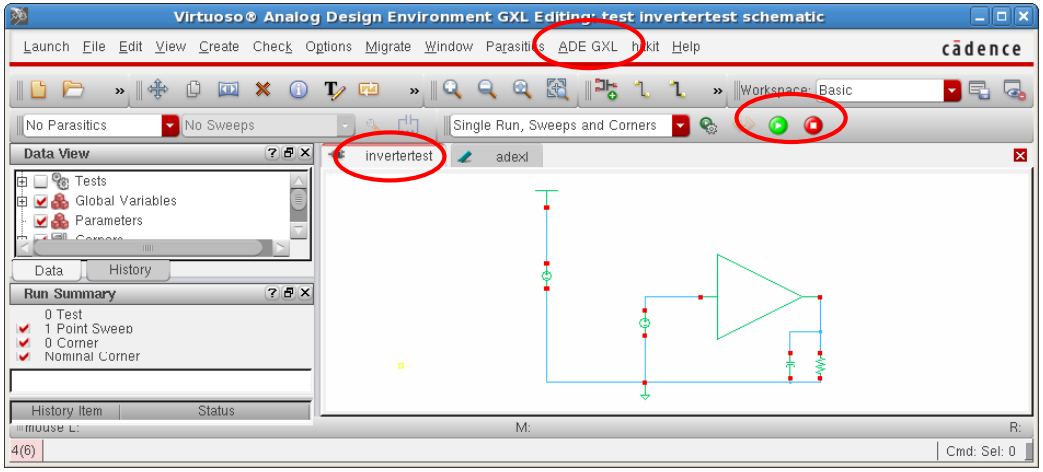
LDE Layout Dependent Effects
EAD Electrically Aware Design



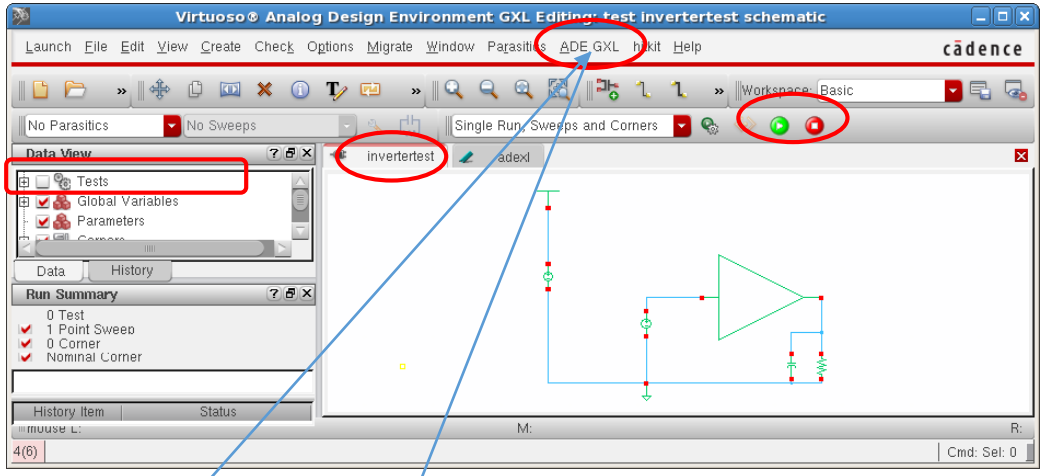
ADE XL creates a new view!



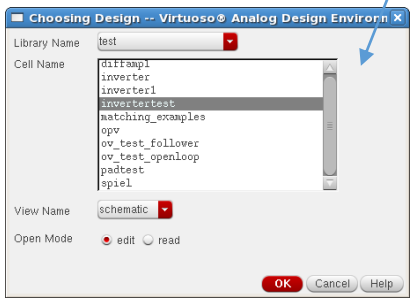


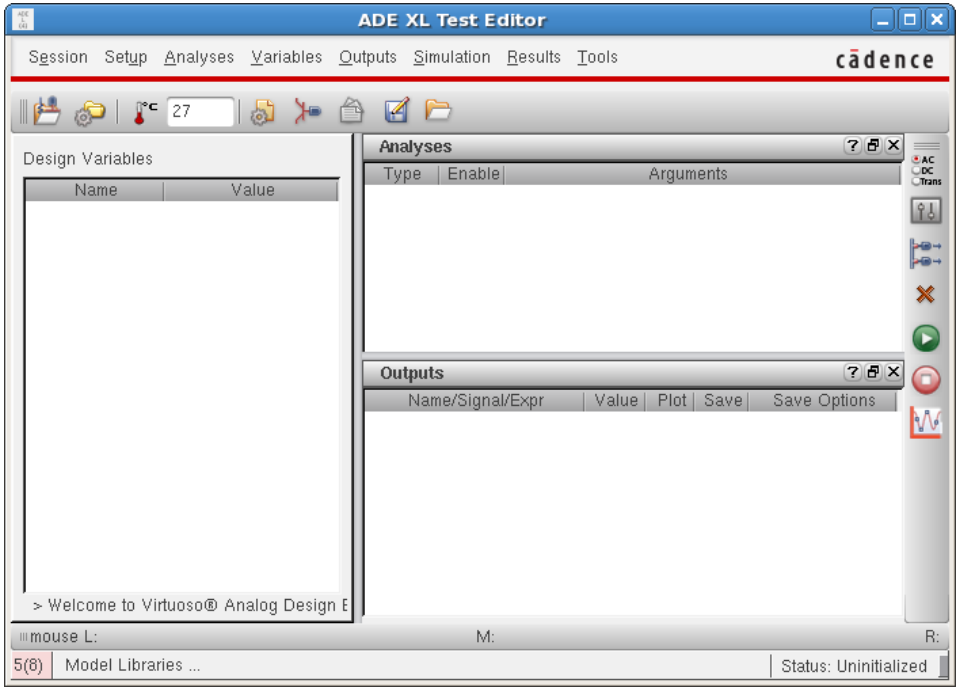


Simulation ADE GXL Create Test

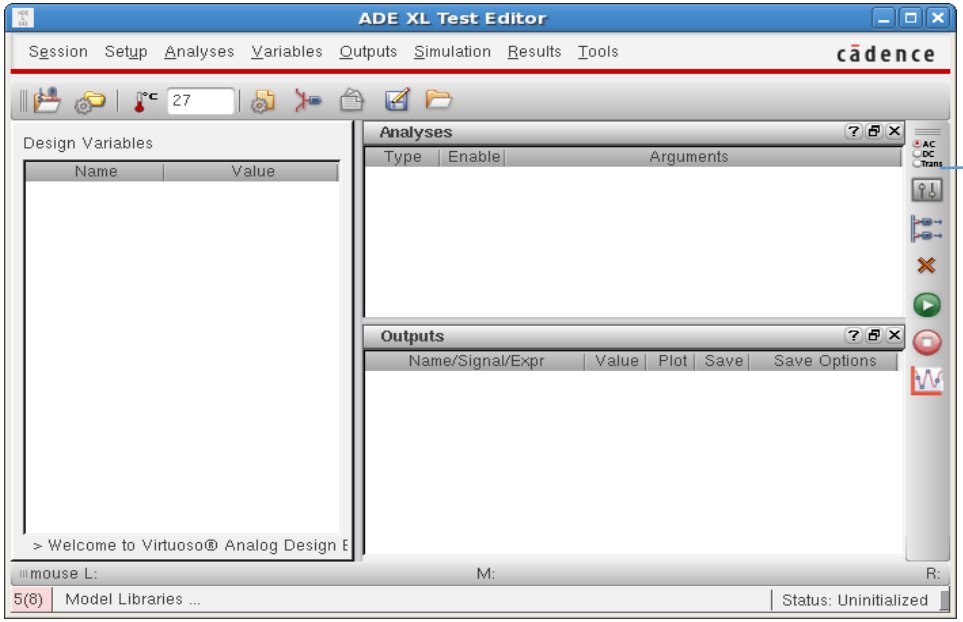


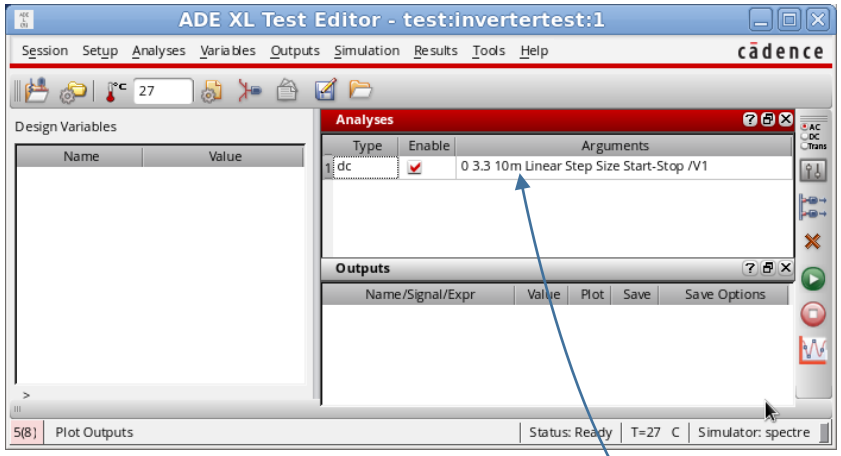
Choose: ADE GXL -> Create -> Test

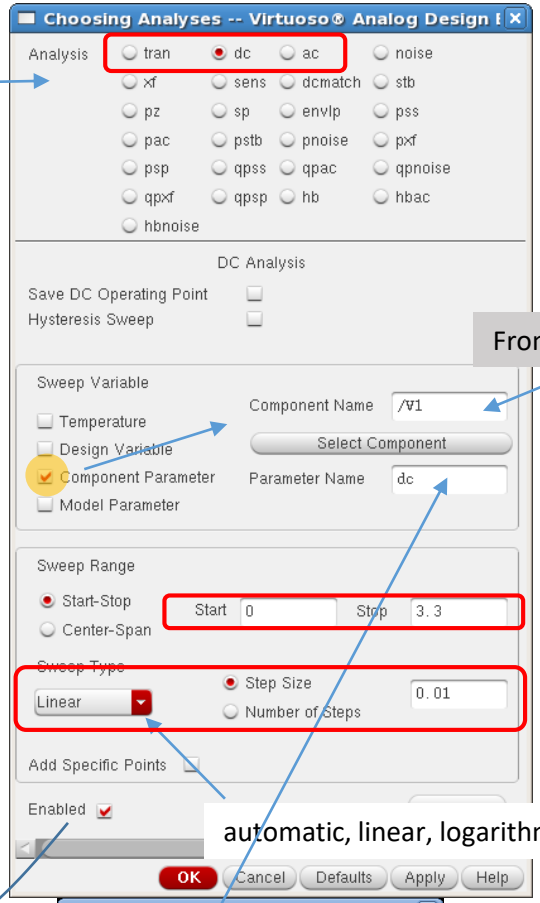




Simulation ADE GXL Create Analyses

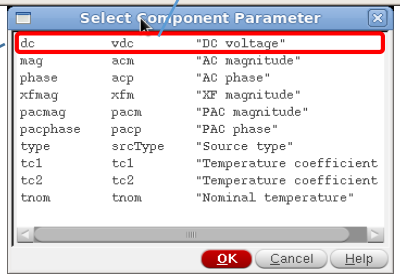






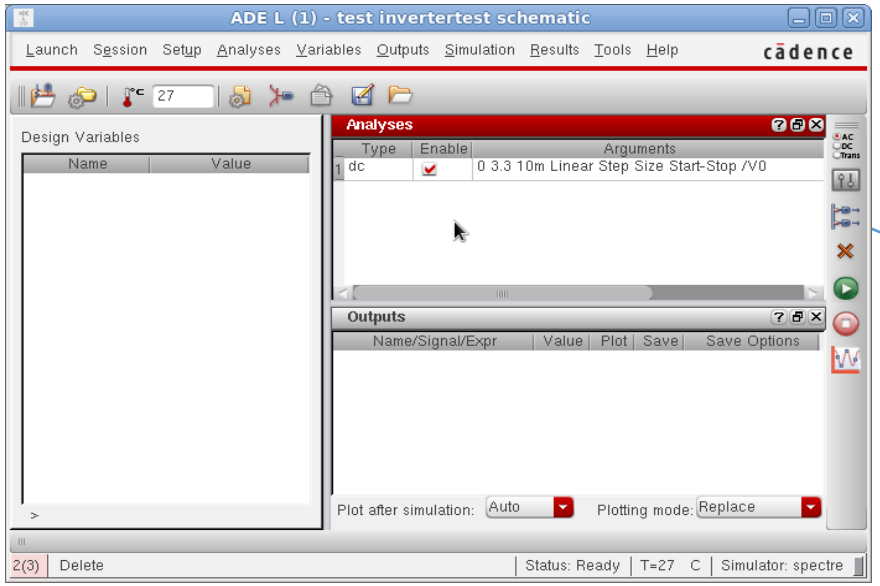
From Schematic

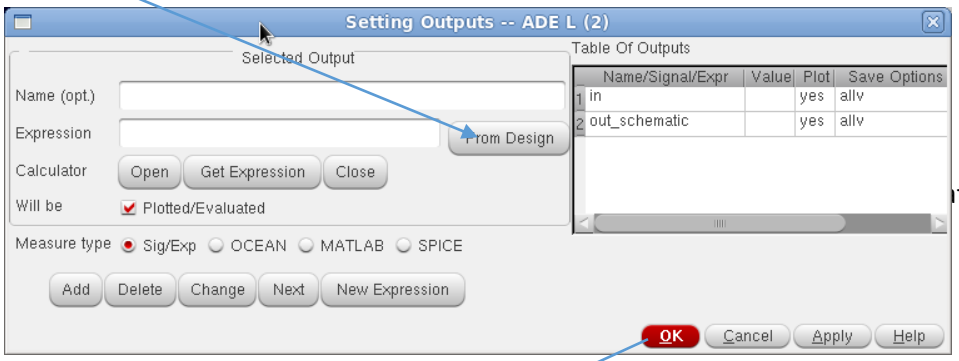
automatic, linear, logarithmic

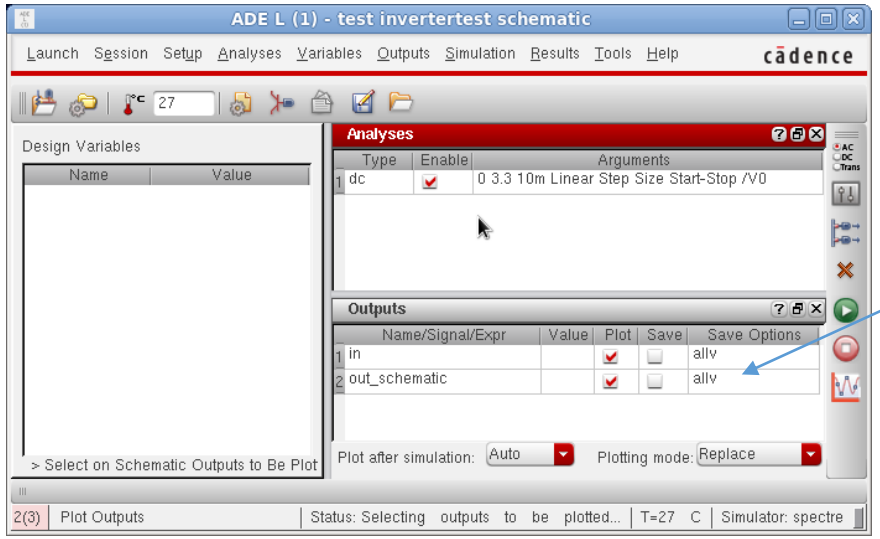


Create/Edit analyses
Global or Design Variables
Simulation Outputs
Delete selected analyses
Run enabled analyses
Stop
Plot

Simulation ADE-XL/L Choose Outputs

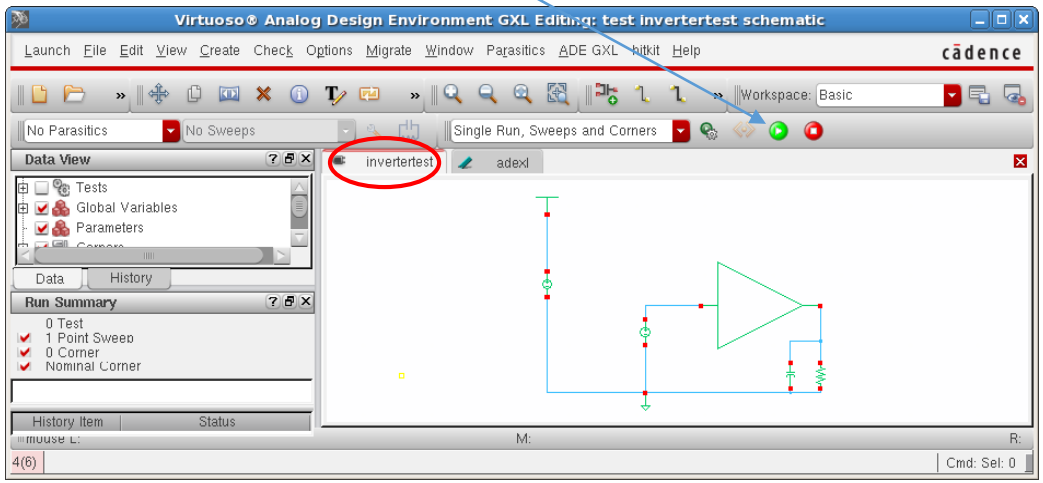






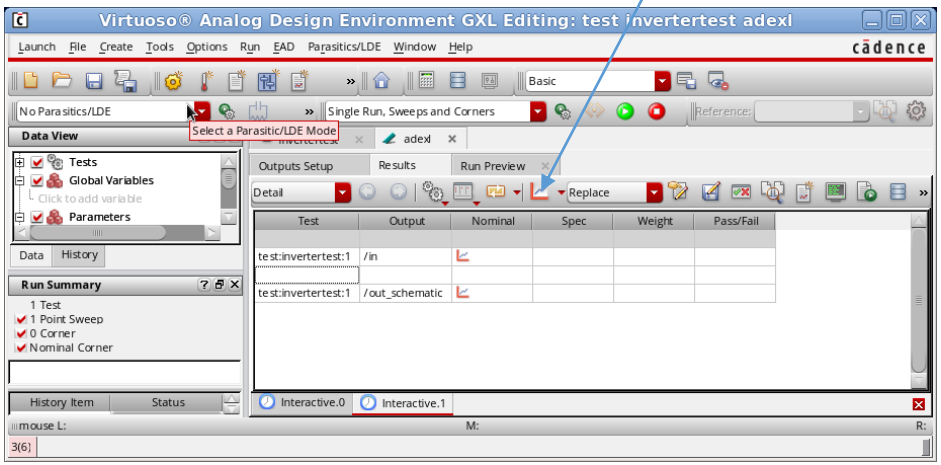
Simulation RUN (in ADE-GXL)

Run Simulation

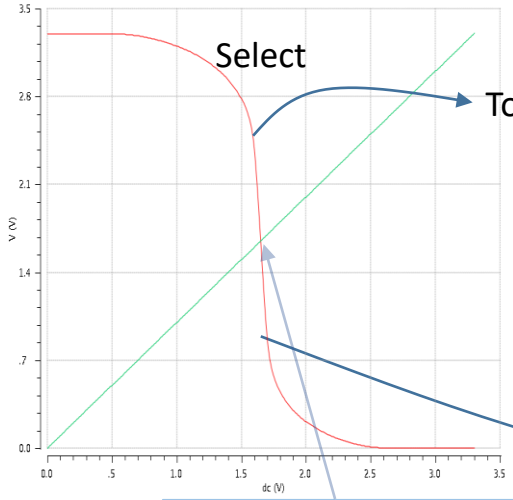


Common Errors stopping execution of simulation:
Design changed and not saved.
Unexpected/unassigned variables due to input errors mostly for component values.
Example: Using "Meg" instaed of "M" for "Mega..
-> Creates a variable "eg"

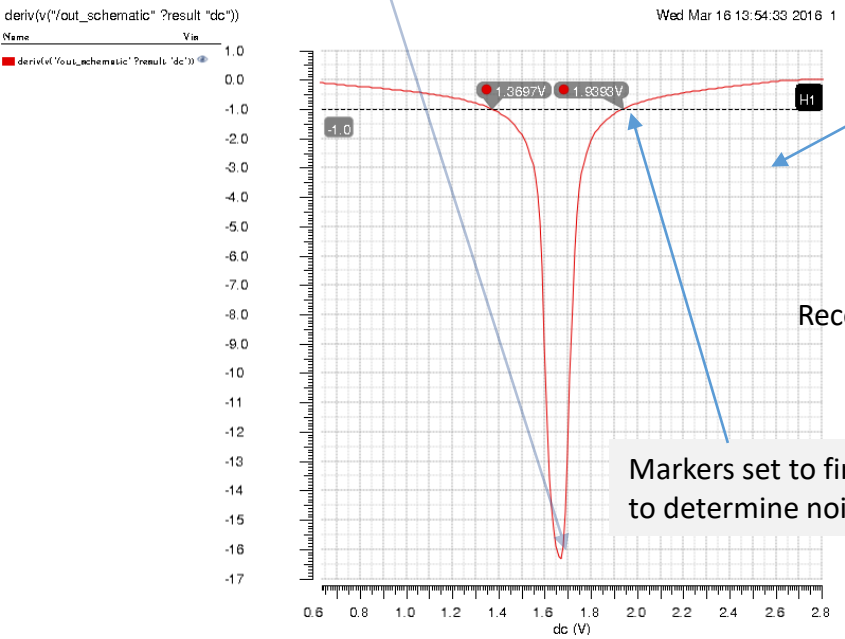
Plot outputs

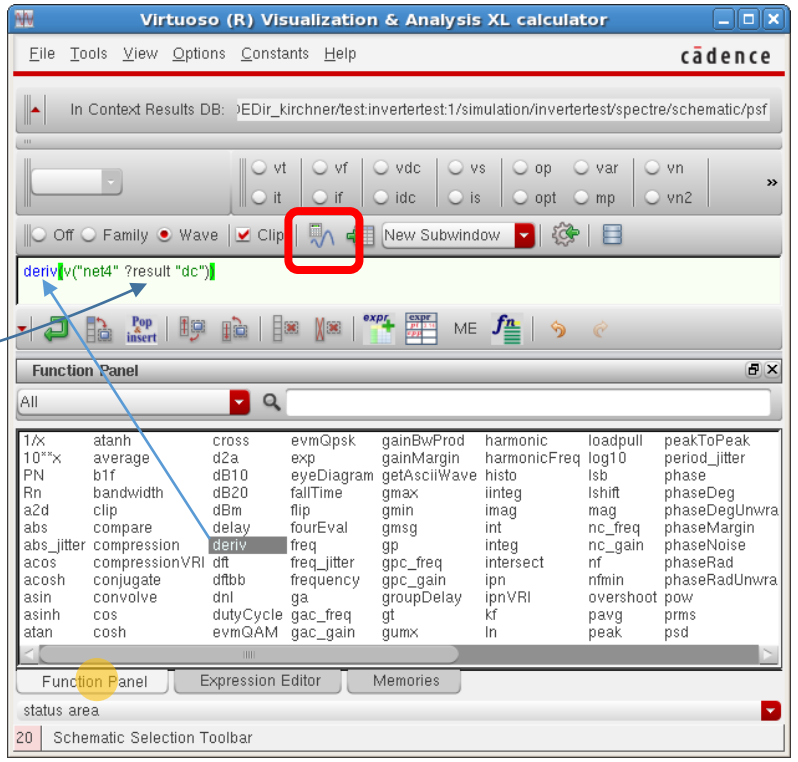


Simulation ADE-L Evaluate Results



Inflexion point (max. abs. gain value)

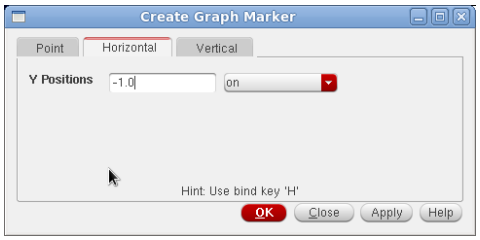




Recommendation: Move derivation plot to new subwindow (RM-> Move to)

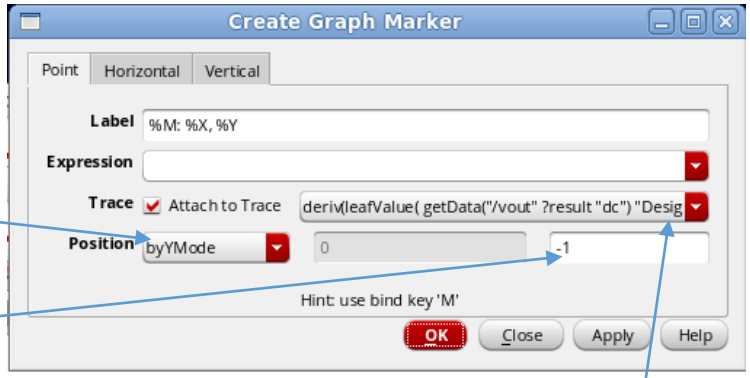
Markers set to find the -1 gain to determine noise margins.

In Visualization&Anlaysis Window -> Marker -> Create Marker



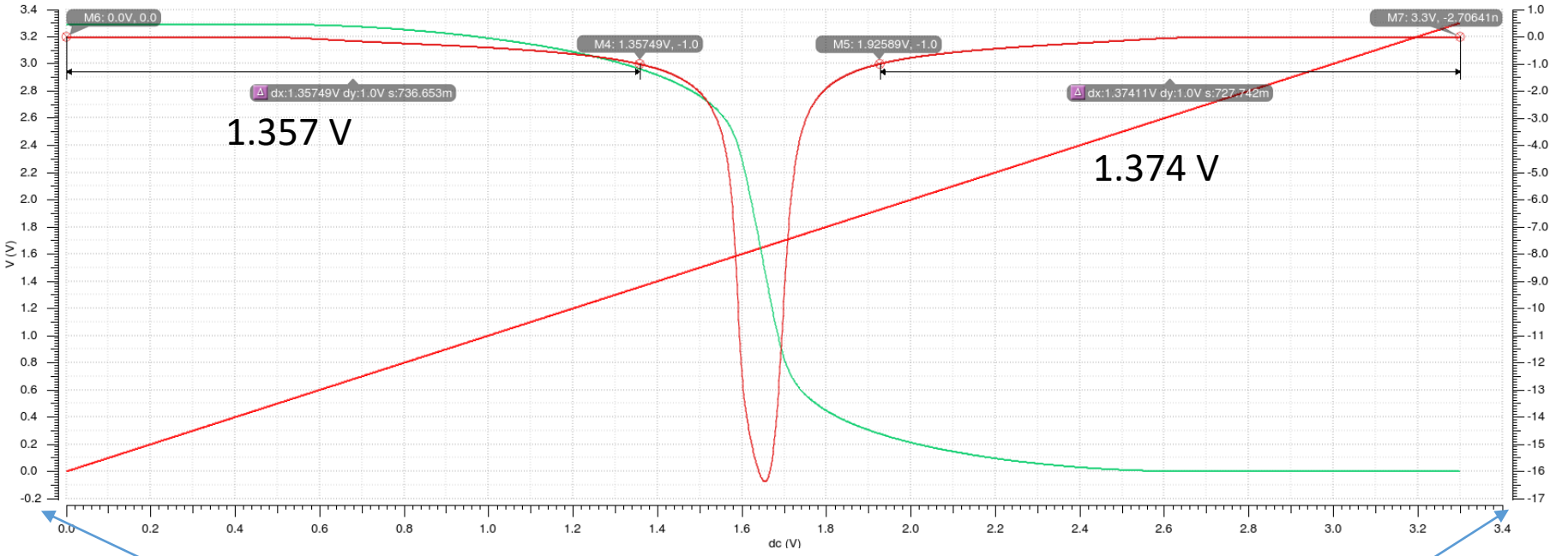
Simulation ADE-L Evaluate Results using Delta Markers

Show the logic margins



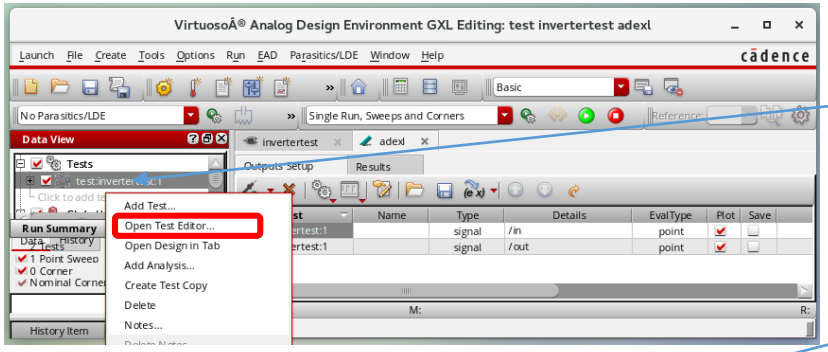
1. Marker -> Create Marker -> Point for $\frac{dv_{out}}{dv_{in}} = -1$
2. Marker -> Create Marker -> Point
   (The two markers overlay at first "y = -1" point]
3. Move and edit second point marker to second "y = -1"
4. Make point markers for x = 0 V and x= 3.3 V
5. Select marker pairs (use Ctrl) and choose Marker -> Create Delta Marker
6. The dx-values are the logic margins

Select derivative trace



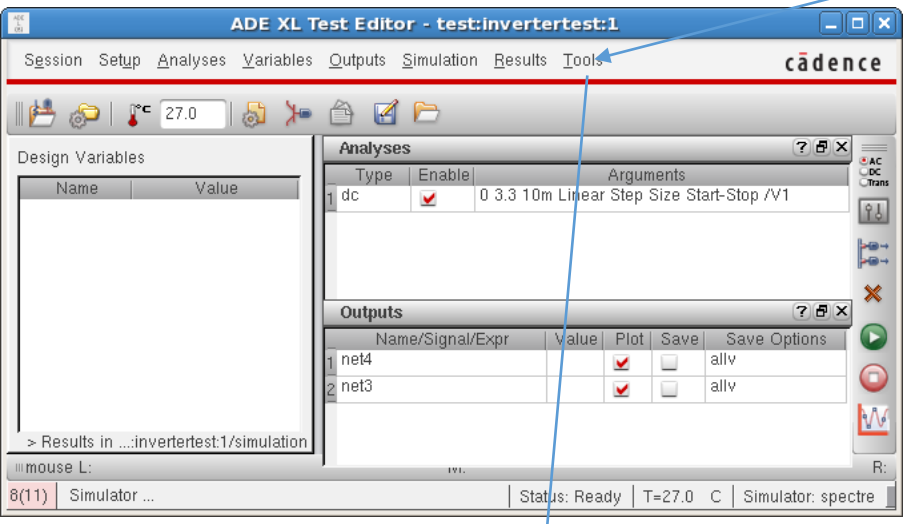
If we have more than one y-axis the markers can be assigned using RM over the marker -> assign to axis

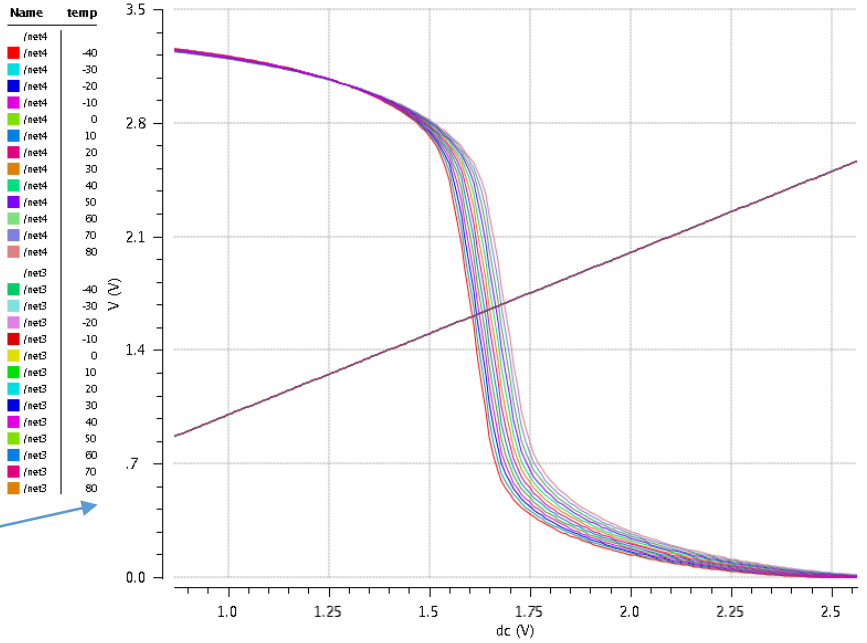
Simulation Parametric Analysis – Temperature (Built in)

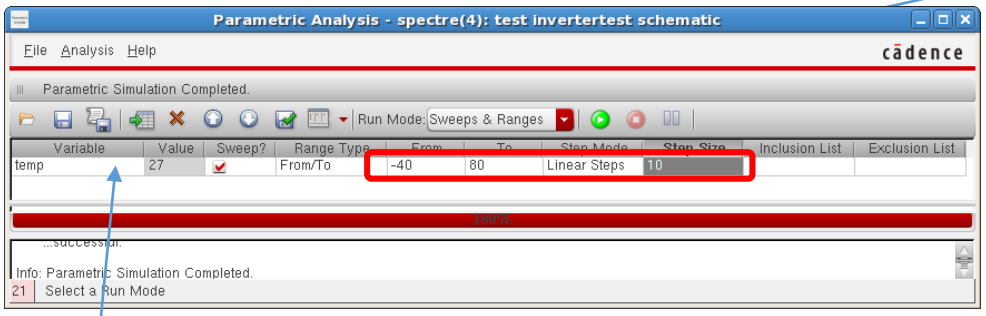


Start ADE Test Editor: with RM over your test

Tools -> Parametric Analysis



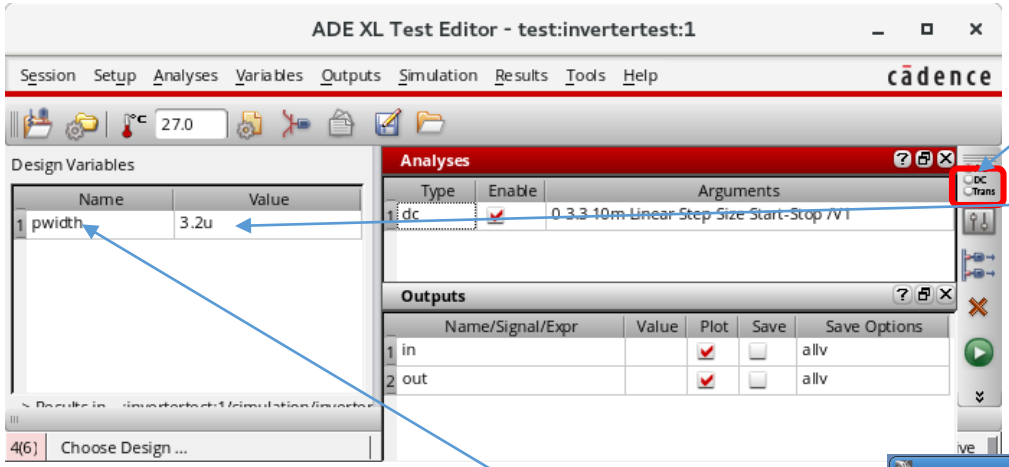




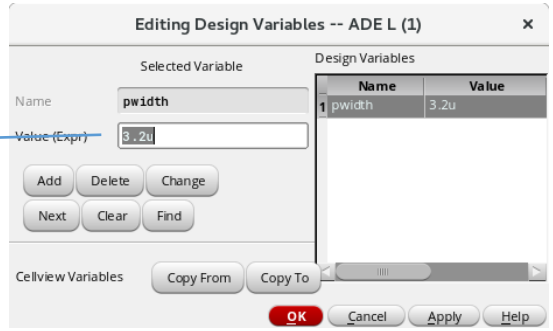
Now we could repeat the logic margin evaluation for the extrem temperatures

Simulation Parametric Analysis – Global and Design Variables

As an example we replace the fixed width of the PMOS transistor by a "Pwidth" in the inverter schematic.
Open the schematic and change the "wtot" of the pmos transistor from fixed value t o "pwith"!

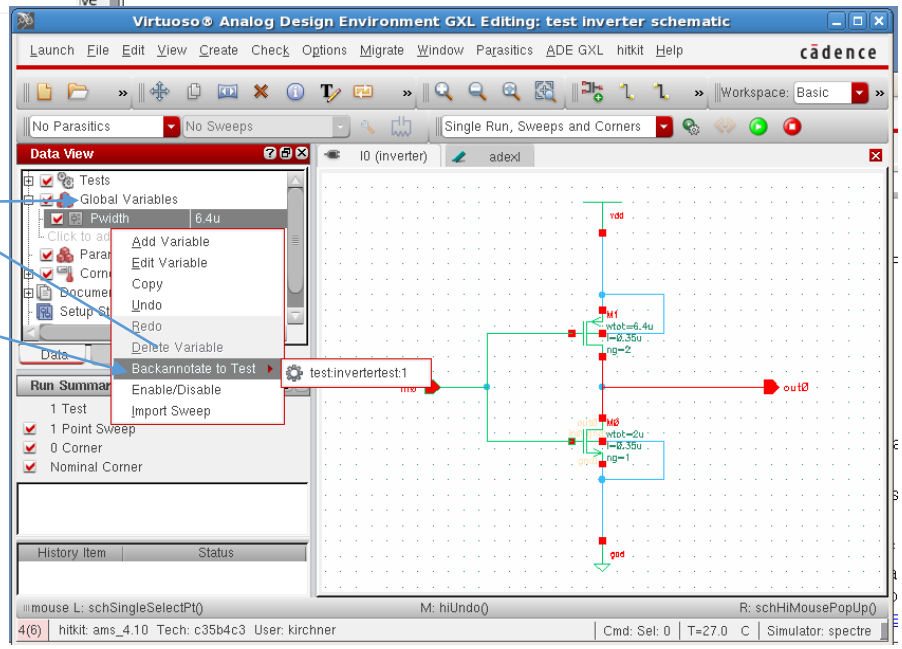


Start here to create a design variable



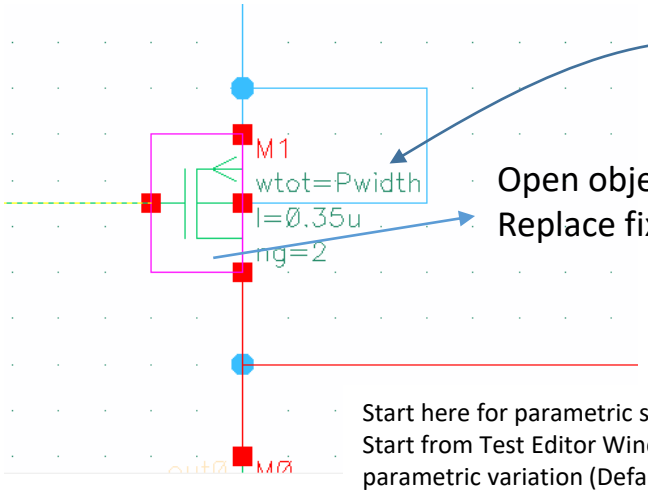
If there is only the testbench schematic open, select inverter and press "E" (descend edit) to open the inverter schematic!

Or start here to create a global variable.
It must be exported/backannotated to appear in test.

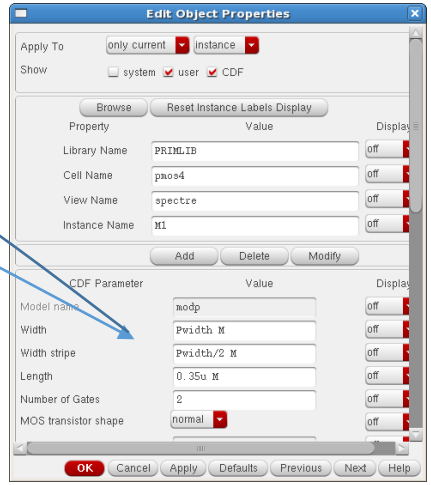


Virtuoso XL uses "Global" and "Design" variables.
Design Variables are valid for the specified test only
Global variables are valid for all tests in the adexl-view
Global variables overwrite design variables with same name
Overwritten design variables are shown with a horizontal strike
It is possible (→RM over design variable) to update a global variable from a design variable

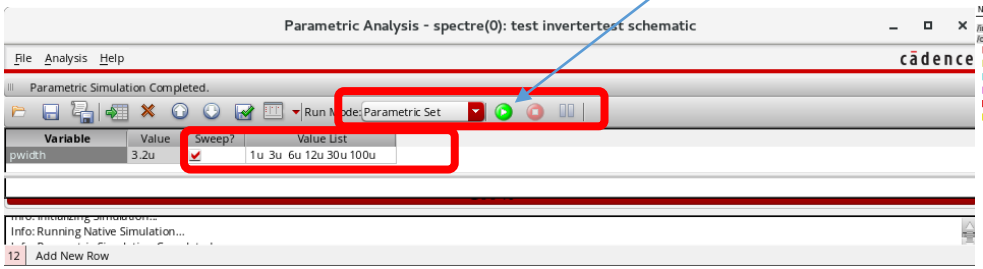
Simulation Parametric Analysis – Using Variables

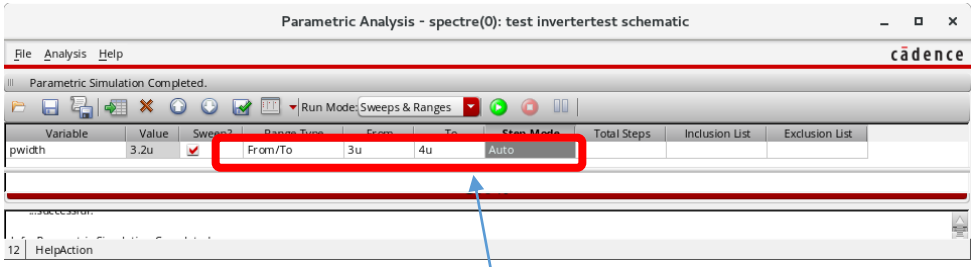


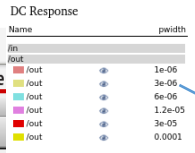
Open object parameters (q)!
Replace fixed value by parameter!

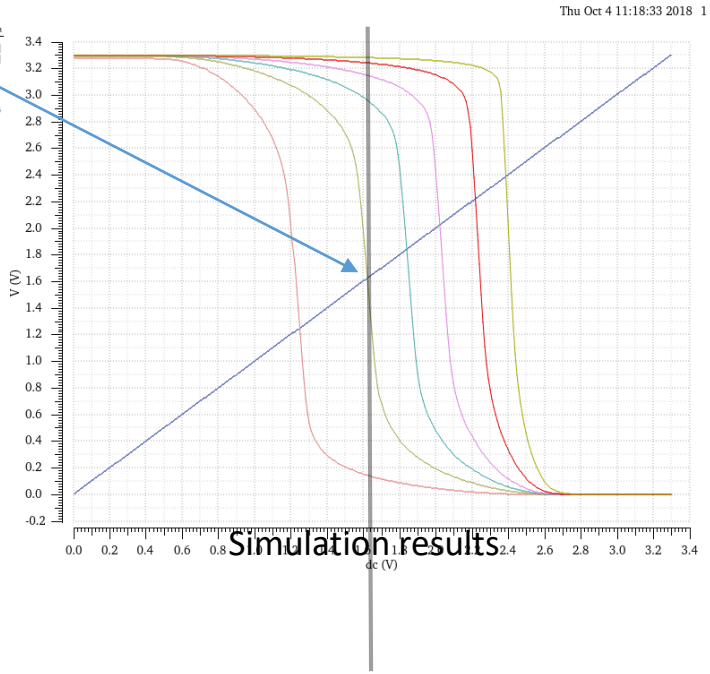


Start here for parametric simulation!
Start from Test Editor Window runs without parametric variation (Default values used).









Simulation results

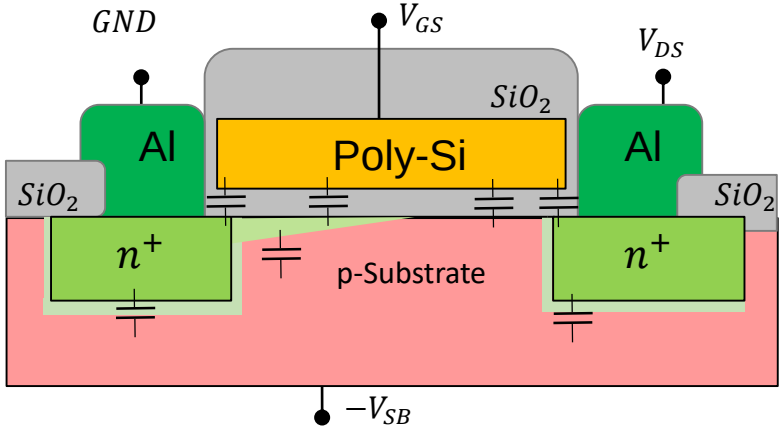
You may refine the simulation with a new set or range of pwidth-values

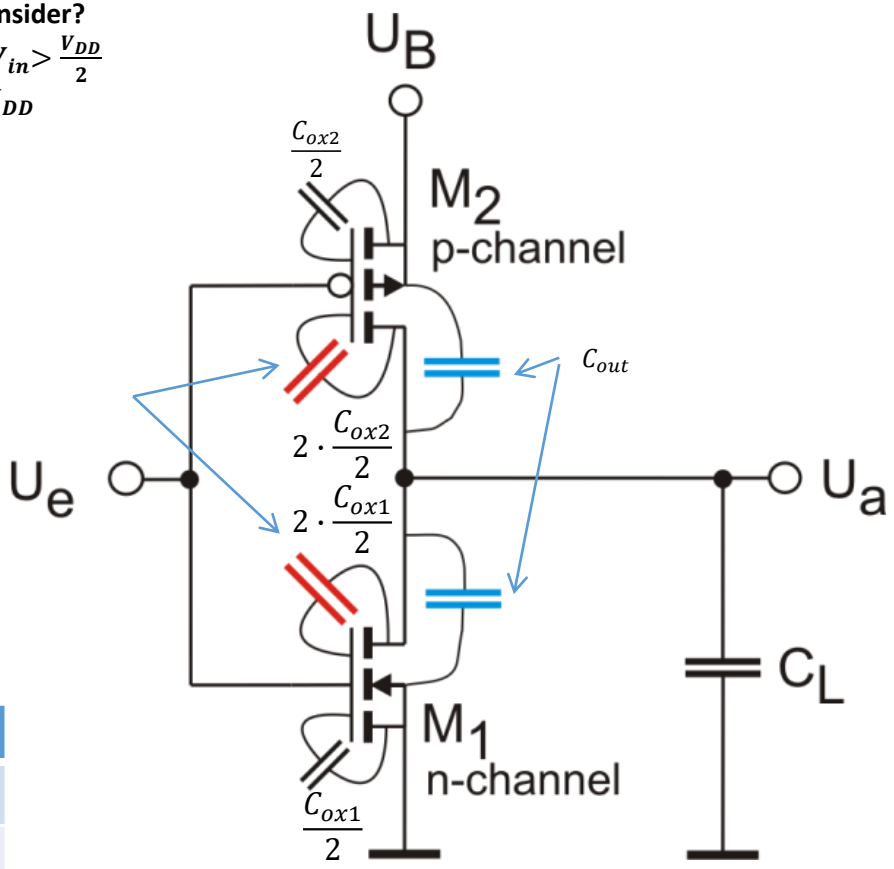
1,65 V

CMOS Inverter Capacitances and Delay

$$C_{in} = \frac{3}{2}(C_{ox1} + C_{0x2})$$

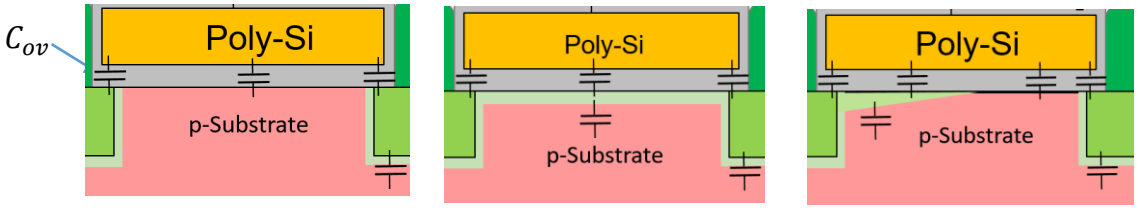
Miller-Capacitor When to consider?
→ only, if $V_{in} > V_{SP}$, resp. $V_{in} > \frac{V_{DD}}{2}$
Voltage change over C: $2 \cdot V_{DD}$





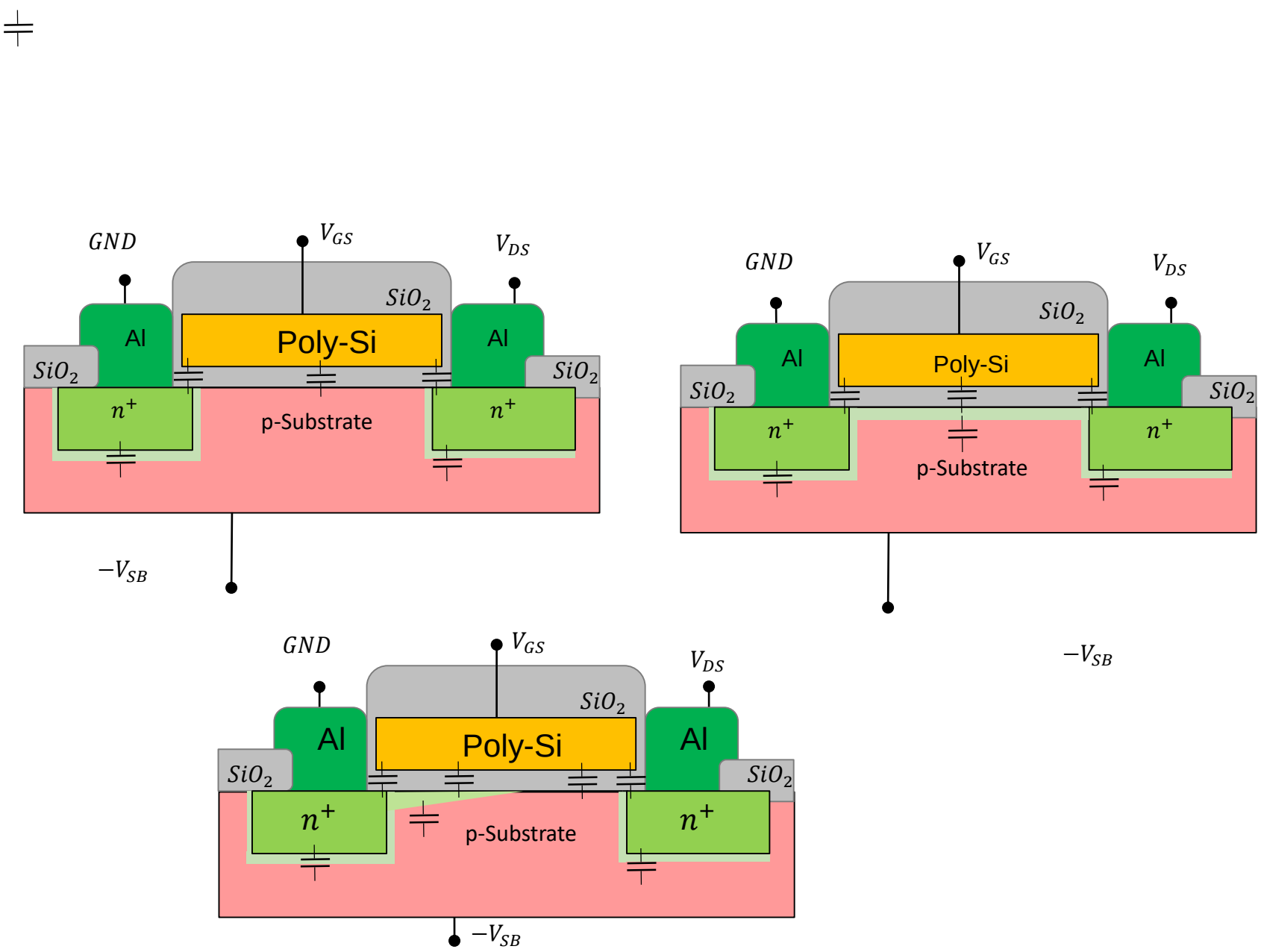
Real circumstances more complex:
Gate capacitances to drain, source, channel, bulk ->
additional $C_{Overlap}$, C_{in} nonlinear:

Region	C_{GB}	C_{GS}	C_{GD}	C_{in}
off	C_{ox}	0	0	$C_{ox} + 2 \cdot C_{ov}$
NPO	0	$\frac{1}{2} \cdot C_{ox}$	$\frac{1}{2} \cdot C_{ox}$	$C_{ox} + 2 \cdot C_{ov}$
PO	0	-> $\frac{2}{3} \cdot C_{ox}$	-> 0	$\frac{2}{3} \cdot C_{ox} + 2 \cdot C_{ov}$

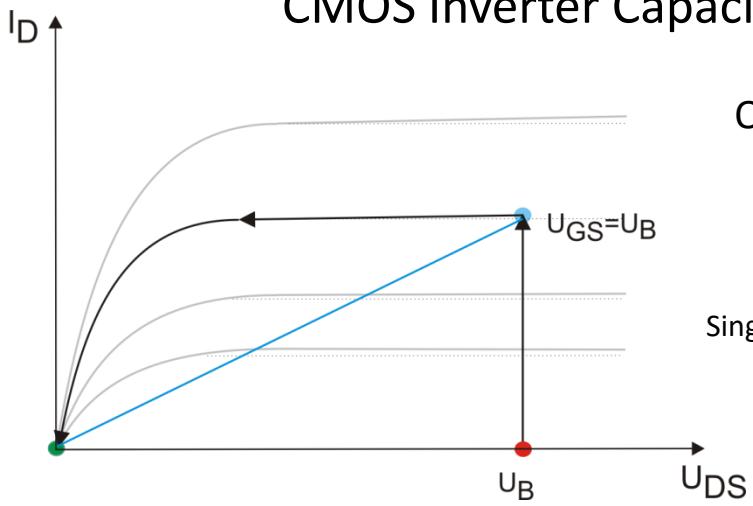


$$C_{out} \approx (C_{ox1} + C_{0x2})$$

Originally the junction capacitance between drain and bulk
In the range of C_{ox} if source and bulk are interconnected
Nonlinear $\sim \frac{1}{\sqrt{V}}$


GND
V_{GS}
V_{DS}
SiO_2
Al
Poly-Si
Al
SiO_2
SiO_2
n^+
p-Substrate
n^+
$-V_{SB}$
GND
V_{GS}
V_{DS}
SiO_2
Al
Poly-Si
Al
SiO_2
SiO_2
n^+
p-Substrate
n^+
$-V_{SB}$
GND
V_{GS}
V_{DS}
SiO_2
Al
Poly-Si
Al
SiO_2
SiO_2
n^+
p-Substrate
n^+
$-V_{SB}$

CMOS Inverter Capacitances, Output Resistance and Delay



Output resistance of FET for charge reversal

Single transistor at V_{DD} with input voltage at V_{DD}

$$I_D = \frac{\beta_n}{2}(V_{DD} - V_{thn})^2 = \frac{KPN}{2}\frac{W}{L}(V_{DD} - V_{thn})^2 = \frac{170\,\mu A}{2\,V^2} \cdot \frac{1\mu m}{0.35\mu m} \cdot (3.3V - 0.5V)^2 = 0.68\,mA$$

$$R_n = R_p = \frac{V_{DD}}{I_D} = \frac{3.3V}{0.68mA} = 4.85\,k\Omega$$

Capacity and time constant-> Delay time (50%-cross distance)

$$C_{in} = \frac{3}{2} W \cdot L \cdot C'_{ox}$$

$$C_{out} = W \cdot L \cdot C'_{ox}$$

$$C_{in} = 4.5\,\frac{fF}{\mu m^2} \cdot \frac{3}{2}(1 + 3.2)\,\mu m^2 = 28.35\ \text{fF}$$

$$C_{out} = 4.5\,\frac{fF}{\mu m^2} \cdot (1 + 3.2)\,\mu m^2 = 18.9\ \text{fF}$$

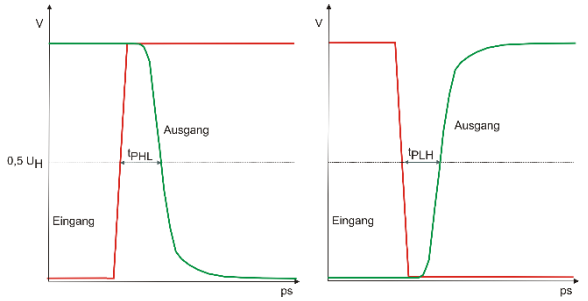
next gate

(+ wire capacitances)

$$t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot (C_{inn} + C_{inp} + C_{outn} + C_{outp})$$

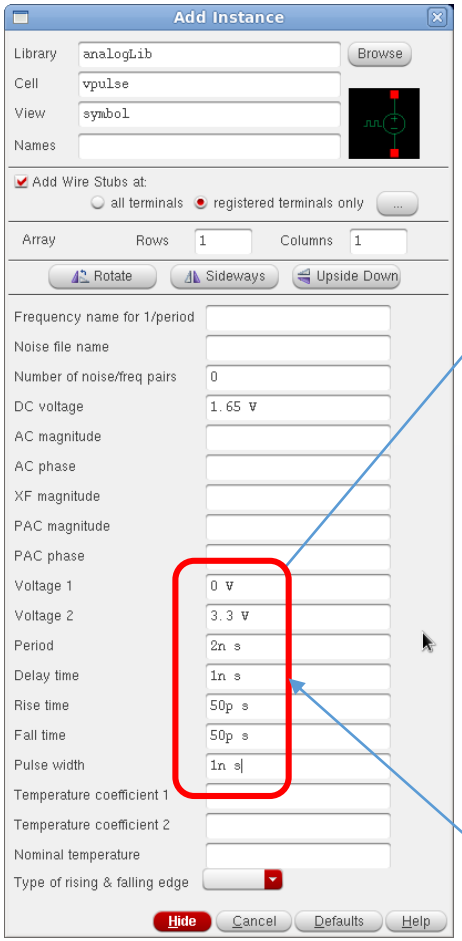
$$t_{pHL} = t_{pLH} = 0.7 \cdot R_a \cdot C'_{ox} \cdot \frac{5}{2}(W_n L_n + W_p L_p)$$

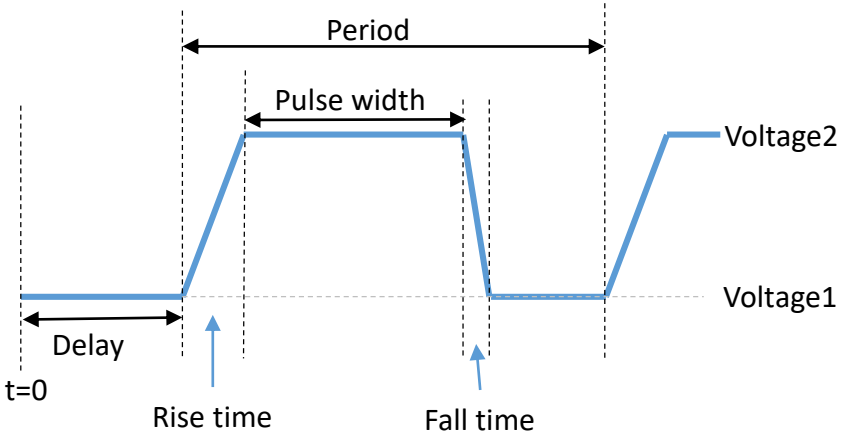
$$t_{pHL} = t_{pLH} = 0.7 \cdot 4.85k\Omega \cdot 4.5\,\frac{fF}{\mu m^2} \cdot \frac{5}{2}(1 + 3.2)\mu m^2 = 160\ \text{ps}$$

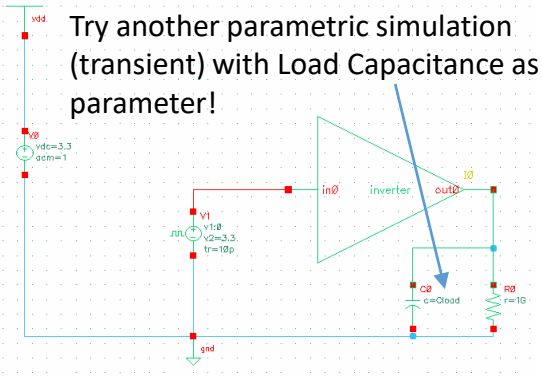


Simulation Transient Analysis

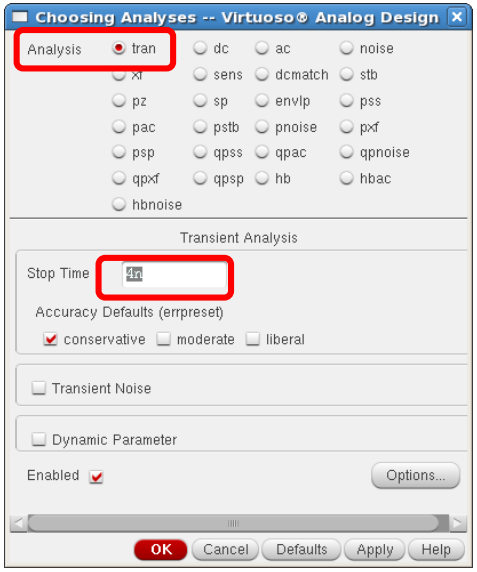
Replace the vdc-source by a vpulse-source. (It would be possible to use this from scratch even for dc-simulation!)



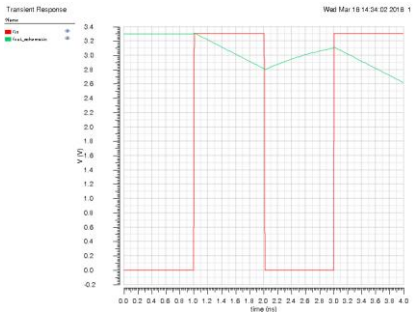




How to find proper time values?

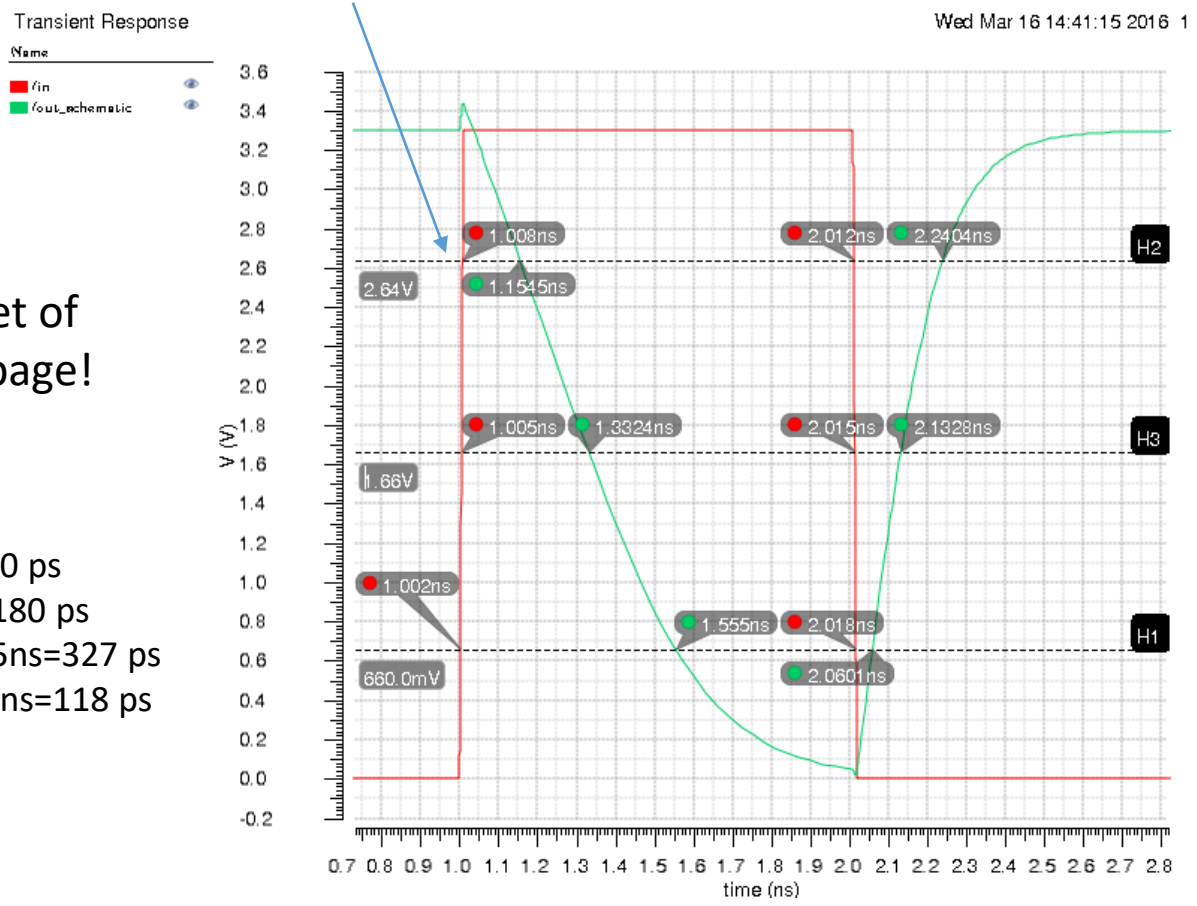


Simulation Transient Analysis



Oops!, looks strange …
1pF load is too much for our small gate

To display cross points: RM on marker line > Intercepts -> On

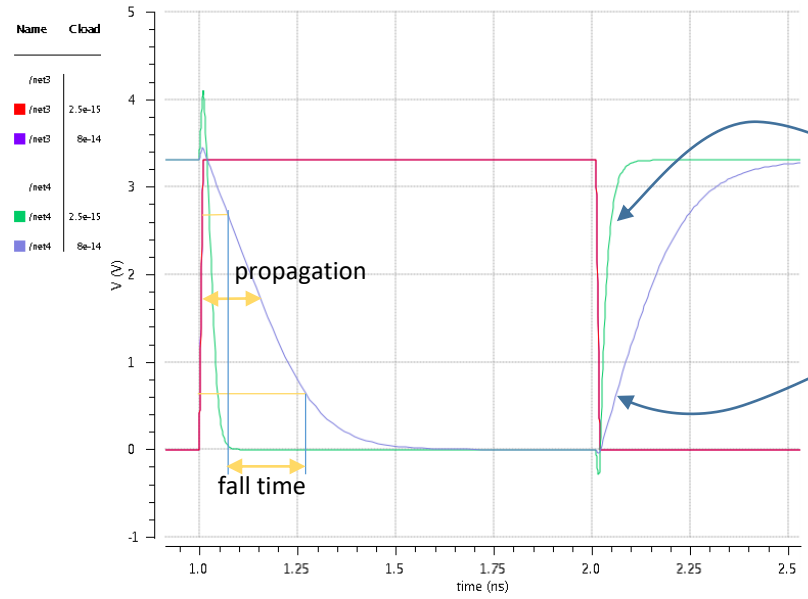


Changed load to 80 fF
Compare with data sheet of ams standard cell next page!

falltime: 1.555ns-1.1545ns=400 ps
risetime: 2.2404ns-2.0601ns=180 ps
delay(inp rise): 1.3324ns-1.005ns=327 ps
delay(inp fall): 2.1328ns-2.015ns=118 ps

Simulation Transient Analysis

Try another parametric simulation with
Load Capacitance as a parameter!
Compare results with a given cell from AMS!



NANGATE INV0 www.ams.com

Databook Build Date: Wednesday Jun 18 17:26 2014 Copyright © 2004-2013 Nangate Inc.
Conditions for characterization library **c35_CORELIB_TYP**, corner **c35_CORELIB_TYP_typical**: Vdd= **3.30**V, Tj= **25.0** deg. C .
Output transition is defined from **20%** to **80%** (rising) and from **80%** to **20%** (falling) output voltage.
Propagation delay is measured from **50%** (input rise) or **50%** (input fall) to **50%** (output rise) or **50%** (output fall).

Cell Area	36.400 um^2
Equation	Q = "!A"
Type	Combinational
Input	A
Output	Q

State Table	
A	Q
L	H
H	L

Propagation Delay [ns]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	0.05	0.53	-0.20	1.07
	rise	0.08	0.94	0.86	2.24

Output Transition [ns]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	0.05	0.71	0.56	1.48
	rise	0.10	1.39	0.54	1.87

Capacitance [fF]	
A	3.8210

Leakage [pW]
0.21

Dynamic Power Consumption [nW/MHz]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		2.50	80.00	2.50	80.00
A to Q	fall	5.98	6.28	160.14	131.01
	rise	34.83	35.09	256.12	205.46

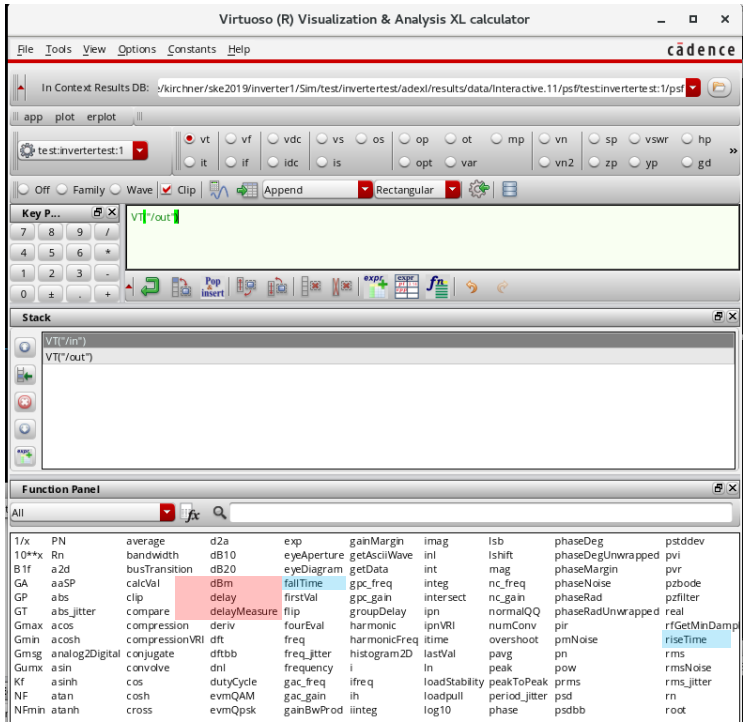
Uups!, explain the negative value!

Simulation Transient Analysis

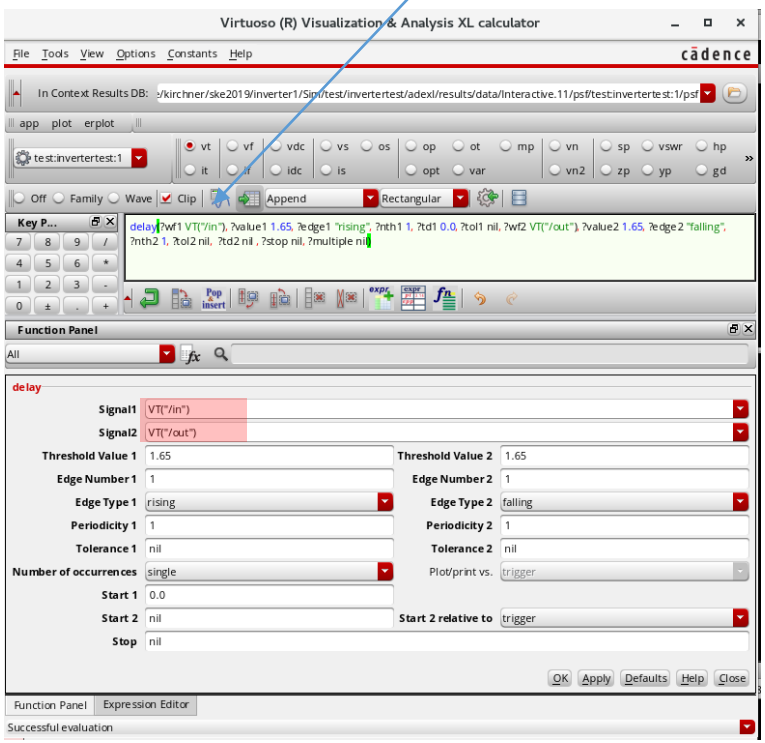
Using Calculator and functions to show delay, fall time, rise time

Calculator works with stack in RPN

Input and output from voltages transient simulation
VT("/in"), **VT**("/in") used in the function "delay"

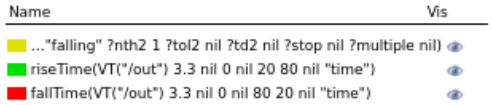


To wave



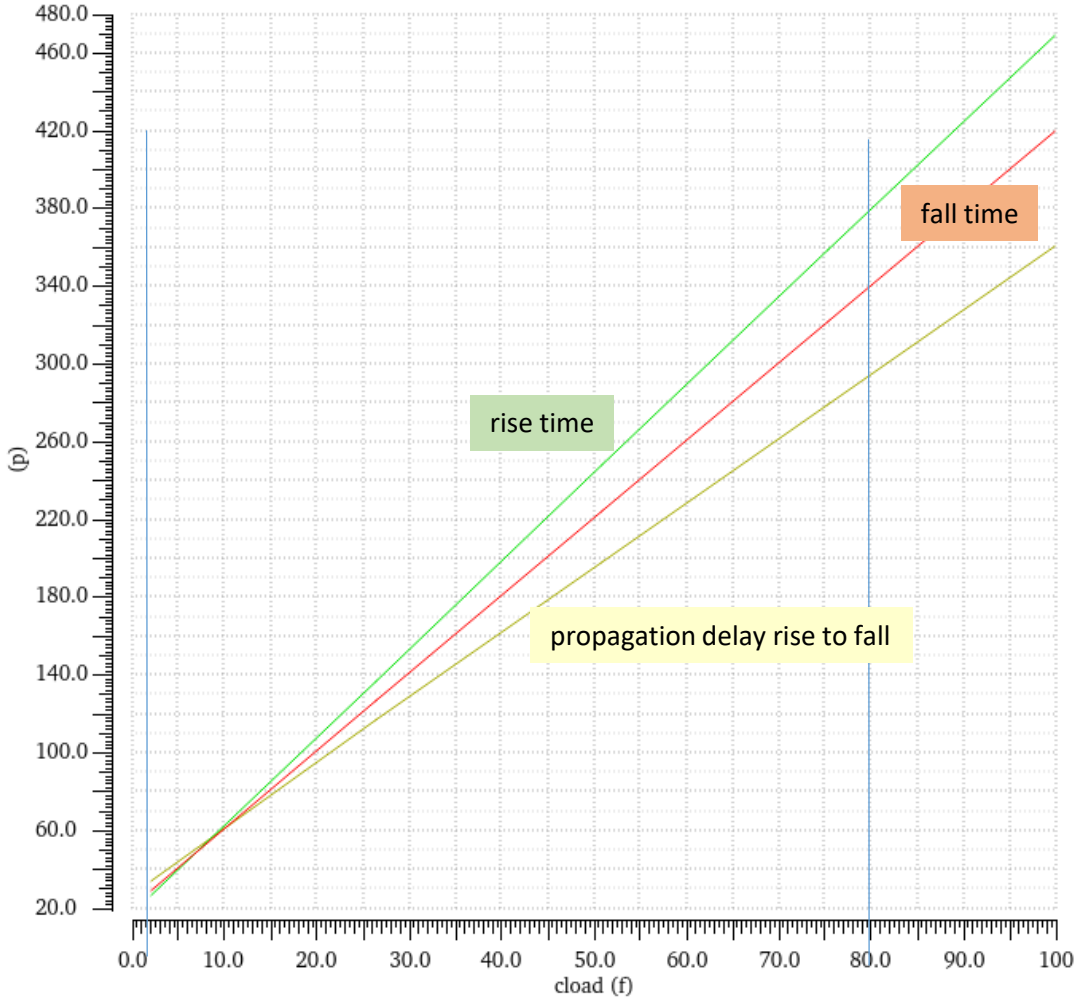
Simulation Transient Analysis

Similar to the input-output-delay you may use the risetime and falltime functions



falltime: 1.555ns-1.1545ns=400 ps
risetime: 2.2404ns-2.0601ns=180 ps
delay(inp rise): 1.3324ns-1.005ns=327 ps
delay(inp fall): 2.1328ns-2.015ns=118 ps

Parametric simulation of delays vs. load capacity
Input transition time 10 ps



Layout Start and Generate from Schematic

Replace all the Variables in the design with fixed values.

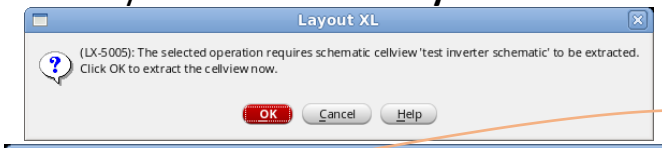
Fold the PMOS (2 gates)

Variables have their scope in simulation only.

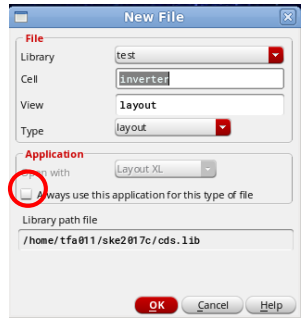
Variables in the testbench are not affected, because they will not be involved in the layout.

In Schematic Editor: **Launch -> Layout XL**

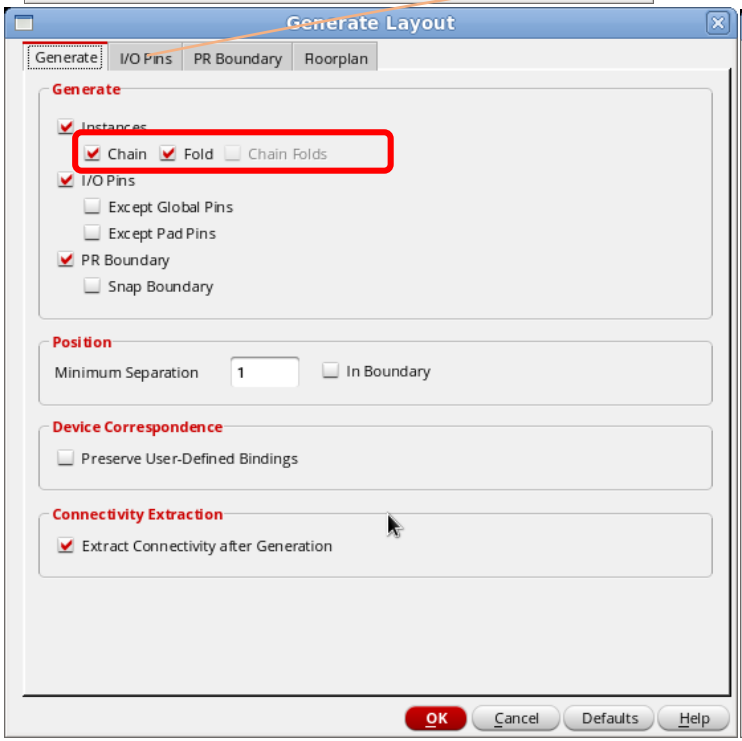
In Layout XL: C**onnectivity -> Generate ->All From Source**

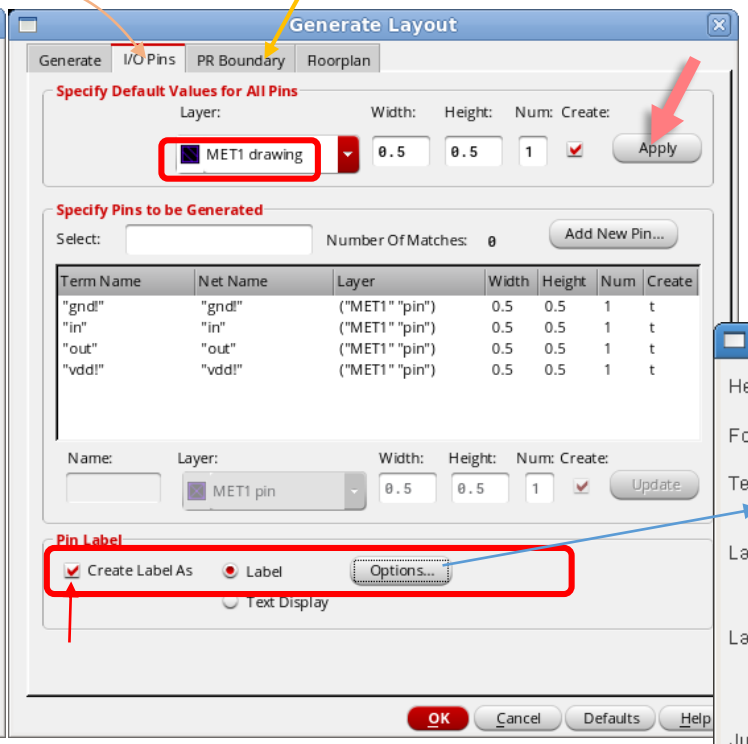


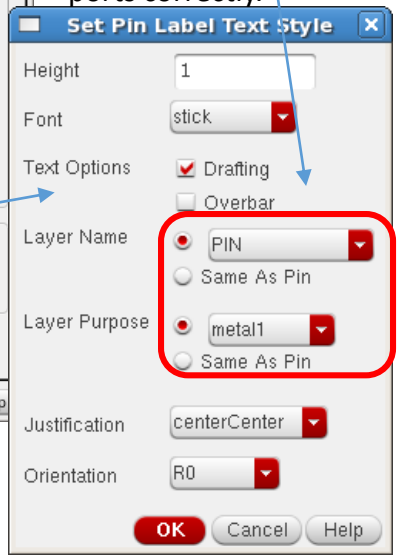
Here we may select the cell boundary: origin, width, height (0:0, 6, 20]



Text is used to recognize ports correctly.







Generates a layout with all instances placed outside a rectangle (estimated cell boundary)

Layout Floorplaning

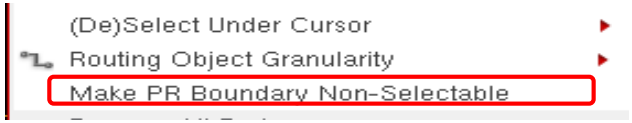
To see all layers: Options -> Display -> Display Levels -> Set "stop" to 32 (Shift-f)

Save to ~/.cdsenv

Suggested cell area

20µm x6 µm cell

Fix it using RM ->
In Layout-XL,
not in Layout-L !



Edit -> Stretch
Tools-> Create Measurement*

Tools -> Clear All Measurements*m
Create -> Shape -> Rectangle

***Ruler** in older versions

Point 0,0

When moving pins include all parts.
Best practice: Snap to the little "+"!

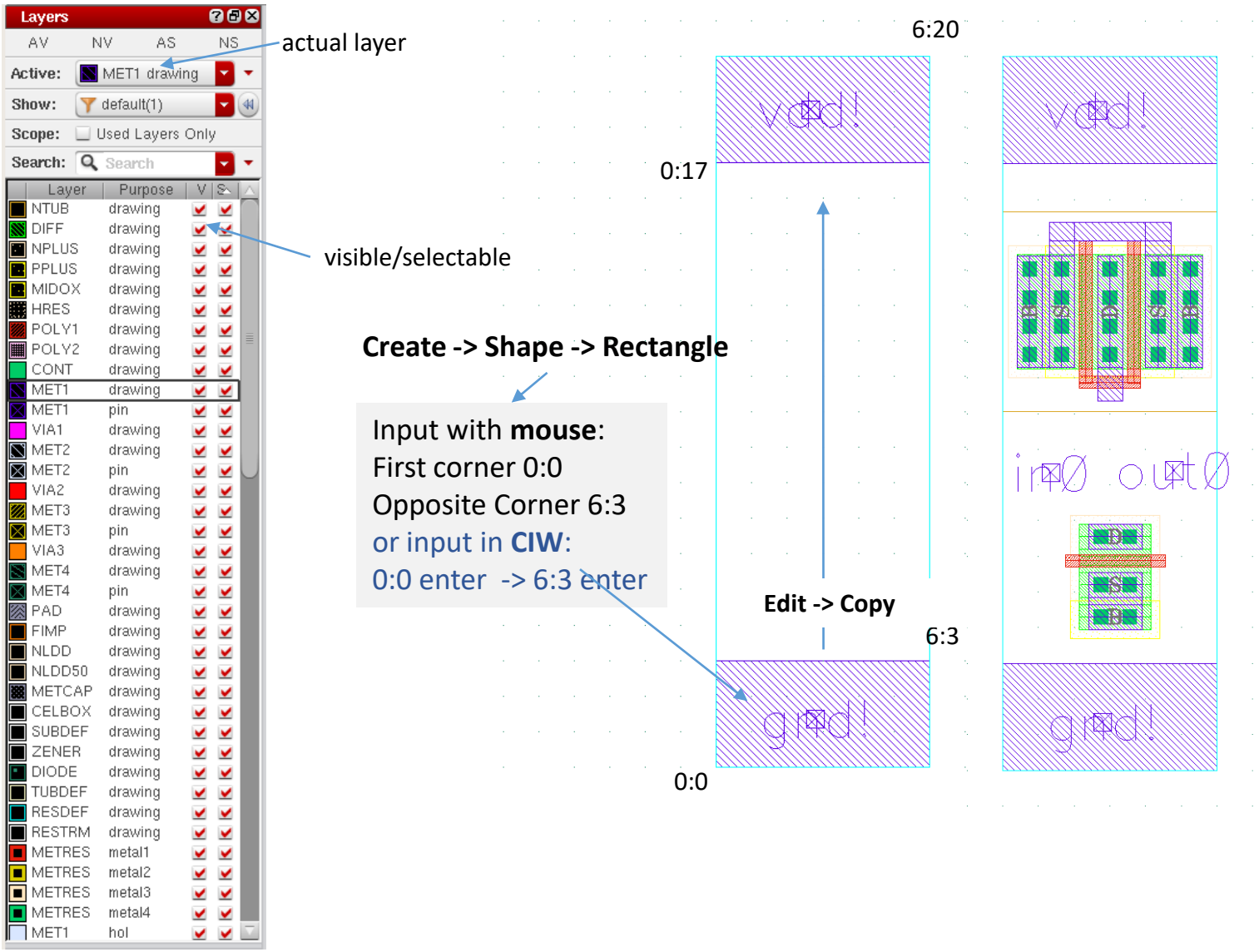
F3 opens move options (e.g. orthogonal, all angels etc.)
(F3 opens options for all commands)

If you have lost prBoundary you can generate a new one by:
Create -> P&R Objects -> P&R Boundary
(prBoundary is an object, not a simple shape!)

Don't have Bulk ?
Delete both transistors in layout.
Open schematic and change transistor property there (add substrate contact).
In Layout XL use Connectivity -> Update Components and Nets.

Way to change something in the schematic and make it actual in Layout

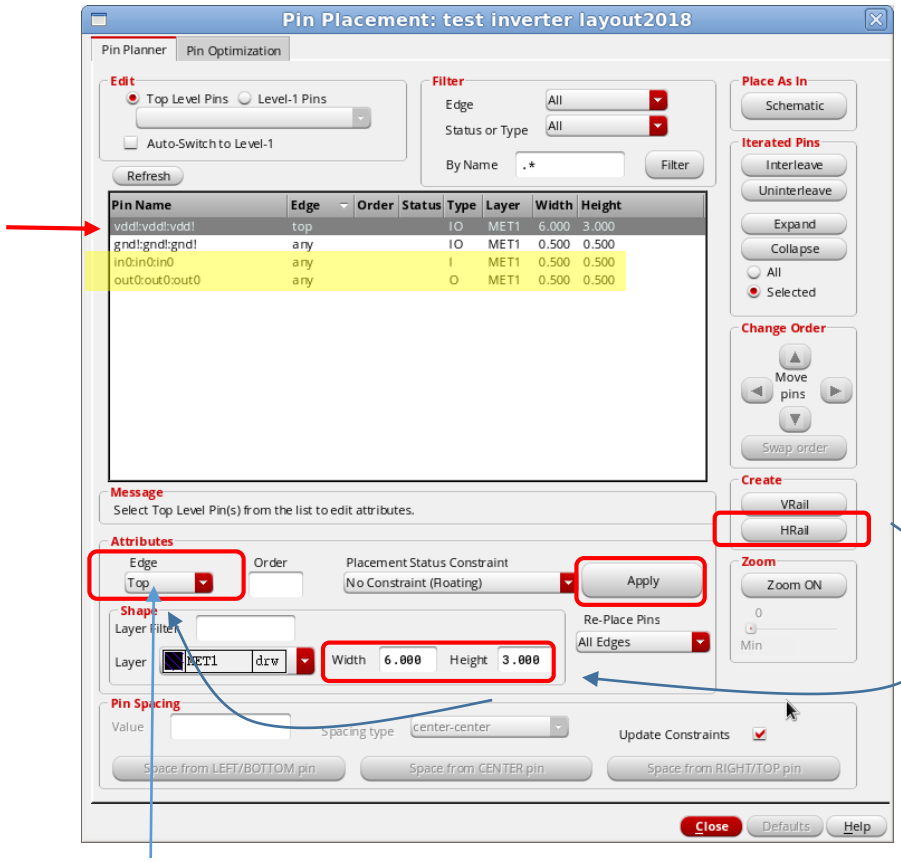
Layout Edit

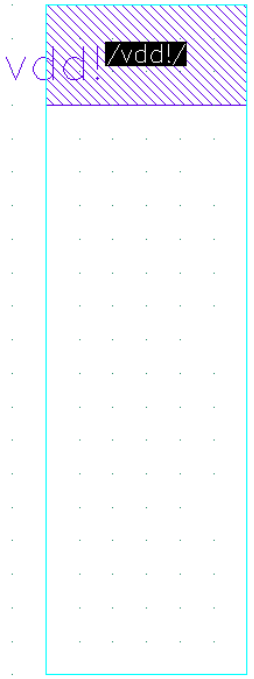

Layers
AV NV AS NS
Active: MET1 drawing
Show: default(1)
Scope: Used Layers Only
Search: Search
Layer Purpose V S
NTUB drawing
DIFF drawing
NPLUS drawing
PPLUS drawing
MIDOX drawing
HRES drawing
POLY1 drawing
POLY2 drawing
CONT drawing
MET1 drawing
MET1 pin
VIA1 drawing
MET2 drawing
MET2 pin
VIA2 drawing
MET3 drawing
MET3 pin
VIA3 drawing
MET4 drawing
MET4 pin
PAD drawing
FIMP drawing
NLDD drawing
NLDD50 drawing
METCAP drawing
CELBOX drawing
SUBDEF drawing
ZENER drawing
DIODE drawing
TUBDEF drawing
RESDEF drawing
RESTRM drawing
METRES metal1
METRES metal2
METRES metal3
METRES metal4
MET1 hol
actual layer
visible/selectable
Create -> Shape -> Rectangle
Input with mouse:
First corner 0:0
Opposite Corner 6:3
or input in CIW:
0:0 enter -> 6:3 enter
6:20
0:17
Edit -> Copy
6:3
0:0
vdd!
gnd!
in
out
vdd!
gnd!

Layout (Automatic) Pin Placement (optional)

In Layout **XL**: Place -> Pin Placement

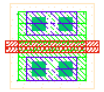
Form offers a chice to place pins at top (vdd!) bottom (gnd!) left (inputs) and right (outputs)
For top (vdd!) and bottom (gnd!) the pins can be extended to rails with the width up to the cell width and a defined hight.

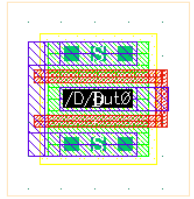




Pin 6x3µm top of the cell

Select Rail **first** then define size then egde



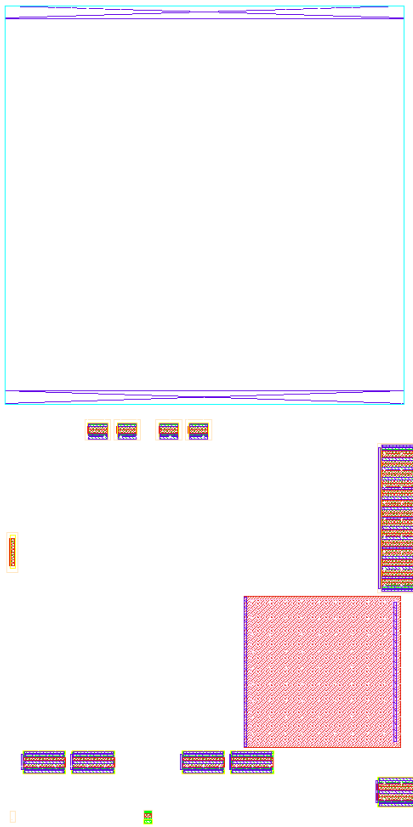


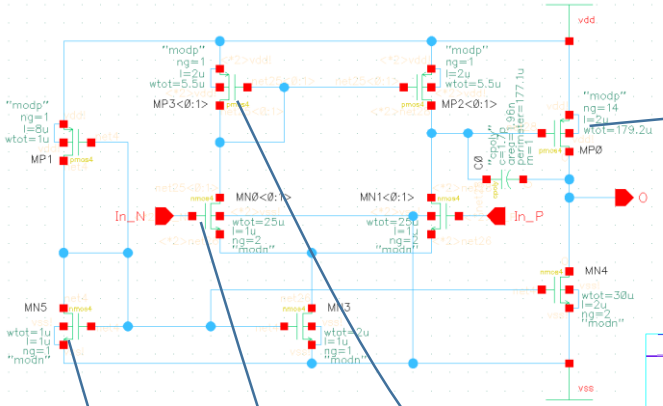
Signal pins may be placed left or right first, then change the placement to "any" and move to the appropriate location. As long as they have the attribute "left" or "right" they are locked to the edge.
Other way : Properties -> Placement Status -> Unplaced

Layout (Automatic) Placement of Instances (optional)

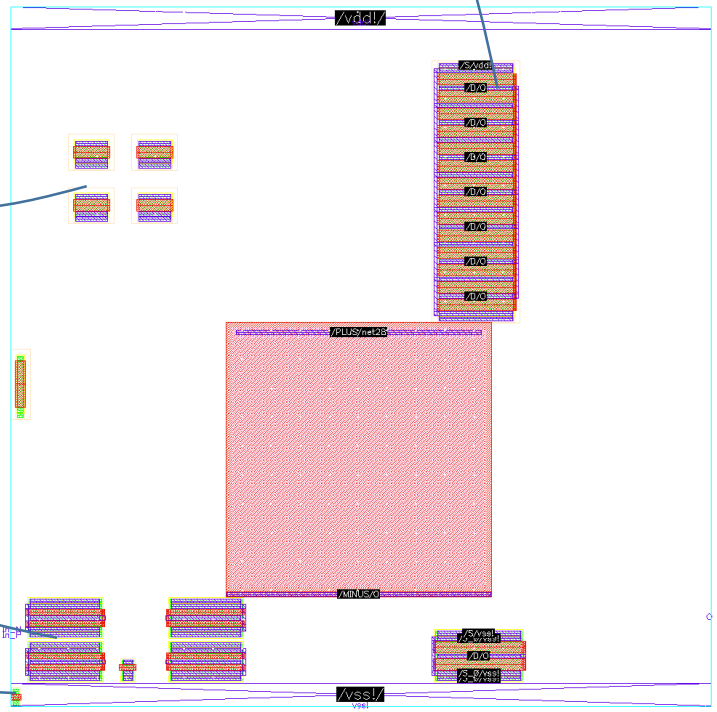
For a simple inverter with two tansistors it is easy to identify the transistors and to place them in an appropriate pattern in the layout. Fore more complex designs some kind of automatic placement may be used. Here shown for an operational amplifier (OPA) and the placement option "like schematic". Helps to identify the instances/parts.

Instances unplaced
(Pins already placed

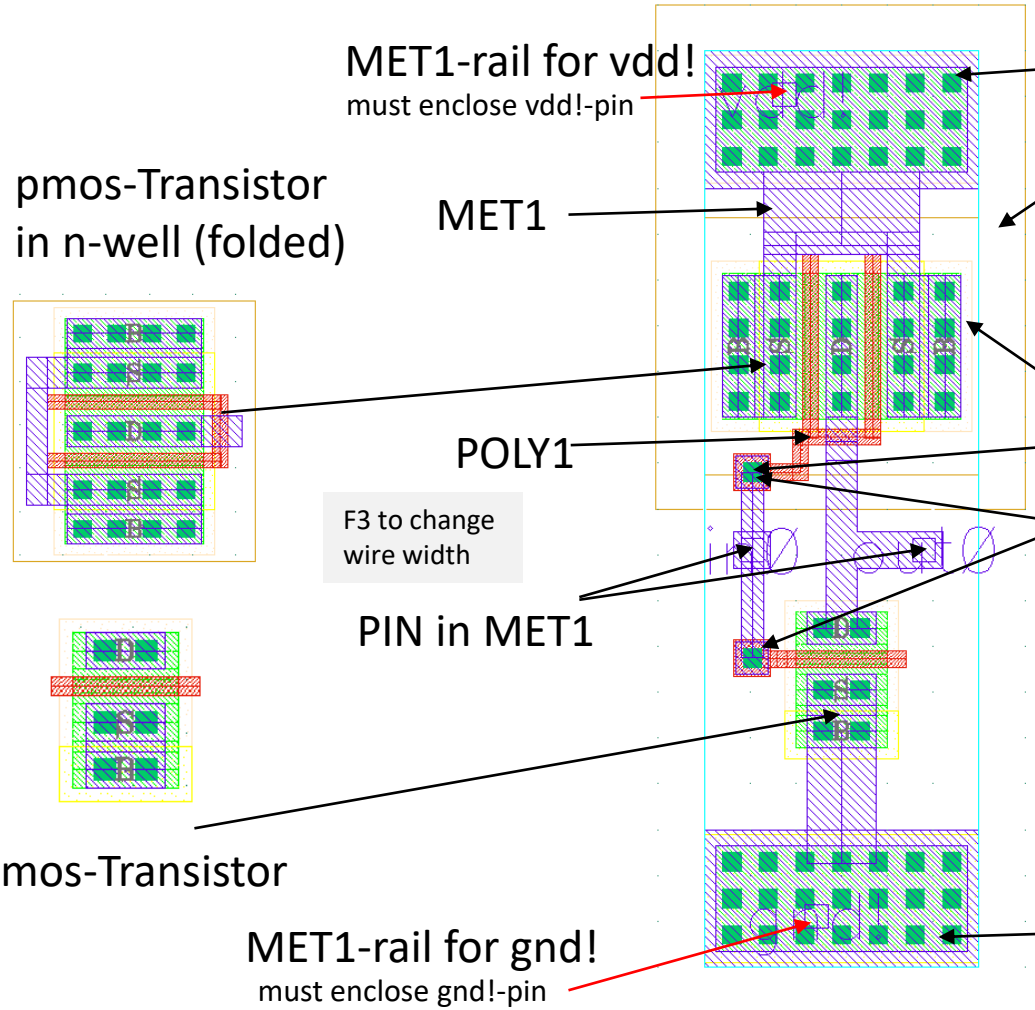




Place -> Analog -> Place Like Schematic



Cell Layout



To consider (design rules):
Poly1: width ≥ 0.35µ, space ≥ 0.45µ
Metal1: width ≥ 0.5µ, space ≥ 0.45µ
Metal2: width ≥ 0.6µ, space ≥ 0.5µ

gnd!, vdd! -> Exclamation marks:
Global signal names valid through design hierarchy

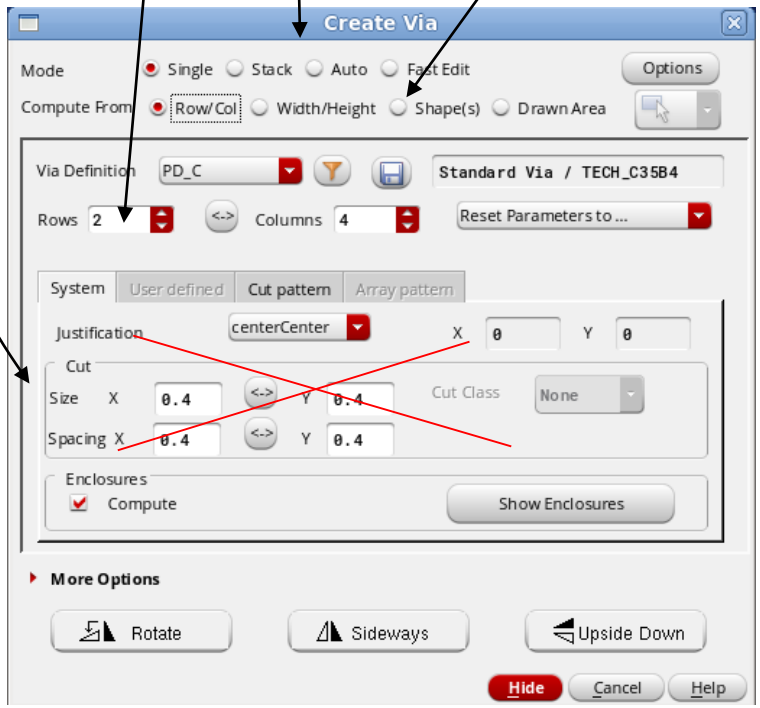
Layout - VIAs

Creating VIAs:

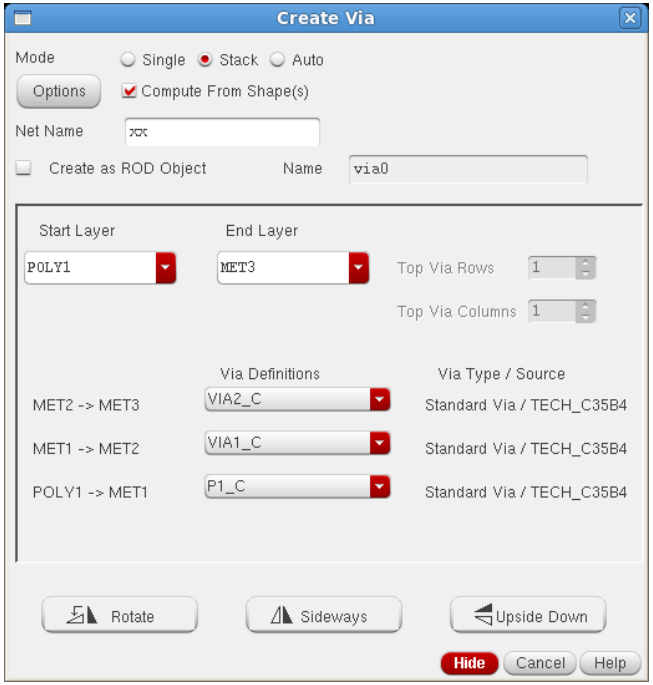
PD_C : p-Substrat-Metal1
ND_C : n-Well-Metal1
P1_C : Poly1-Metal1
P2_C : Poly2-Metal1
VIA1_C : Metal1-Metal2
VIA2_C : Metal2-Metal3
VIA3_C : Metal3-Metal4

Make them for the power stripes before routing of wires.

Layout of single contact predefined. Do not change!
Number and alignment variable. Using "**Compute from Shape(s)**" fills area with appropriate number of contacts.



Stacked VIAs connecting more than two layers available:

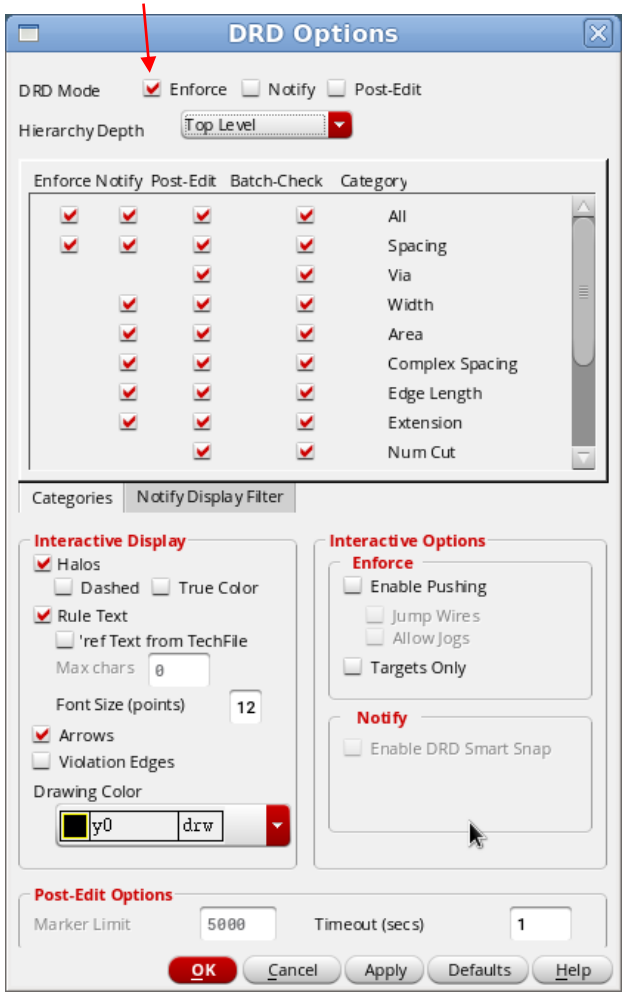


Cell Layout – Design Rule Driven Design -DRD (optional)

To avoid design rule violations when moving instances or wiring we can switch on the DRD.

Options -> DRD-Edit

You must select one mode here!



"Enforce" stops edit action (route a wire, move an element) if a design rule is violated.

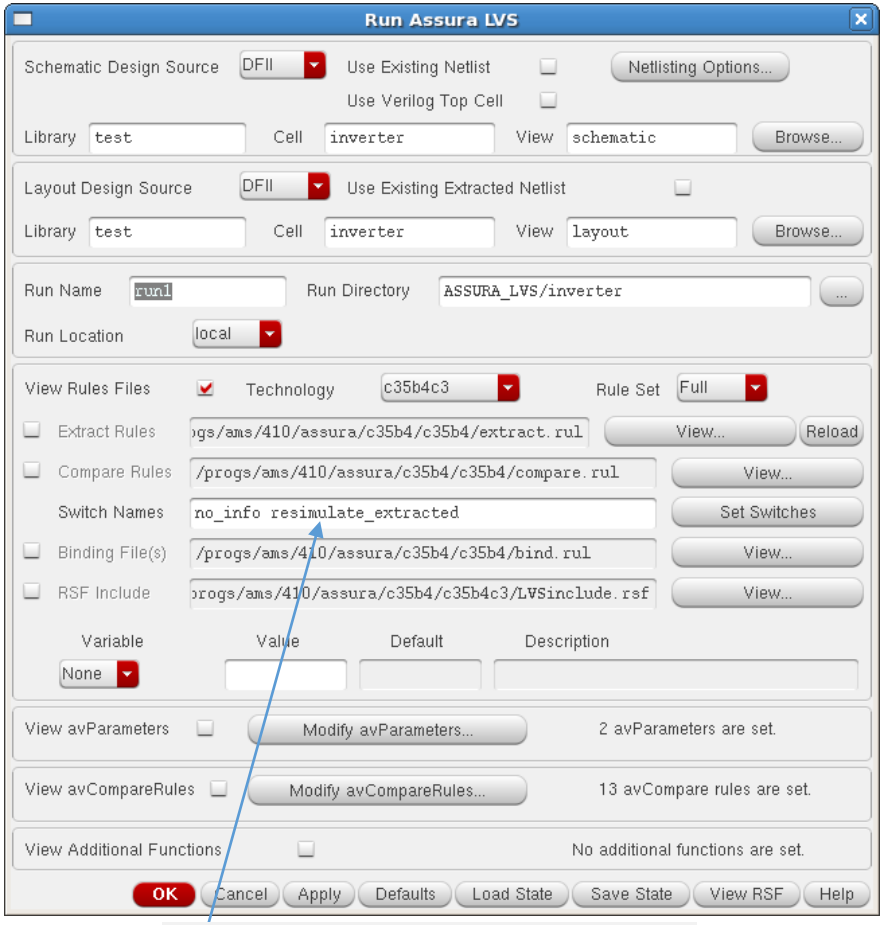
"Notify" writes a warning if a design rule is violated.

"Post-Edit" sets markers only if a design rule is violated.

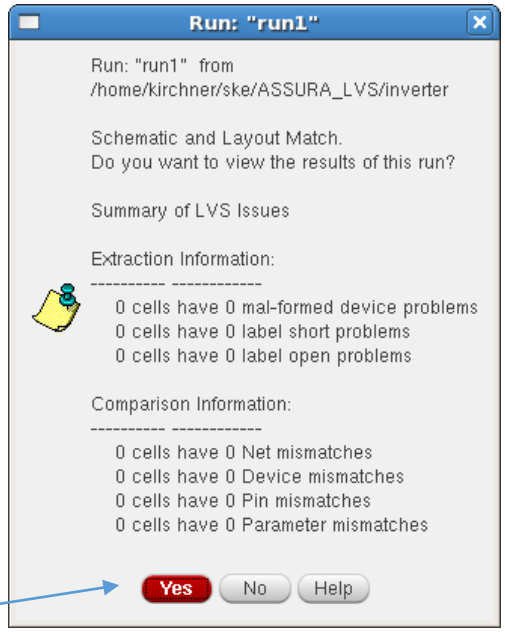
Cadence Layout - LVS

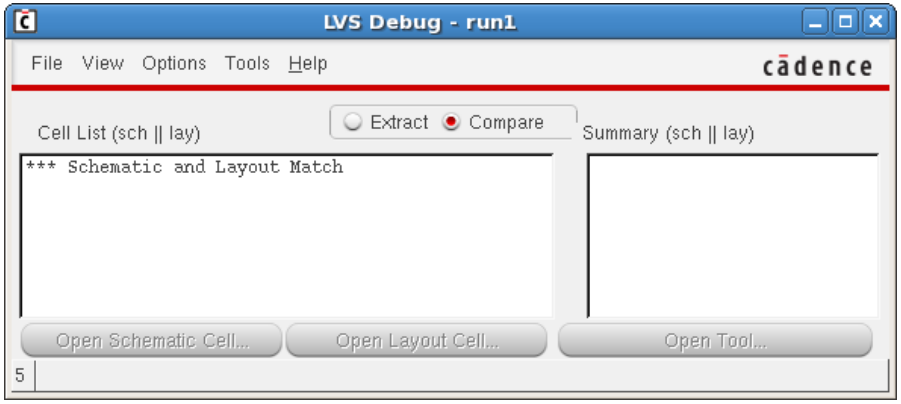
Assura -> Run LVS

Compare Layout Versus Schematic



wait!





That's what we want to see!

Necessary for QRC parasitic extraction

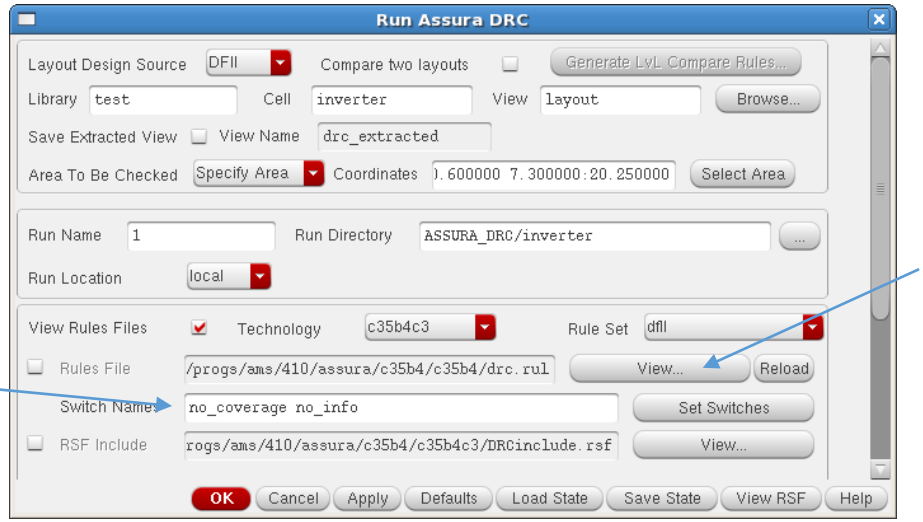
ams says: "**Do NOT use** the **resimulate_extracted** switch because in that case substrate shorts (soft connections between different nets via substrate) might not be found correctly!

→ Dann fehlen im av_extracted die design layer

http://asic.ams.com/hitkit/hk410/assura/assura.html

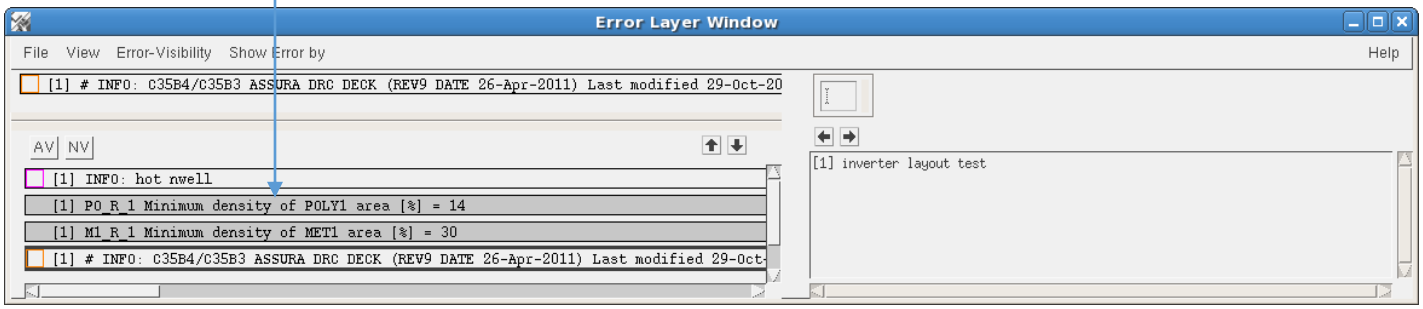
Cadence Layout - DRC

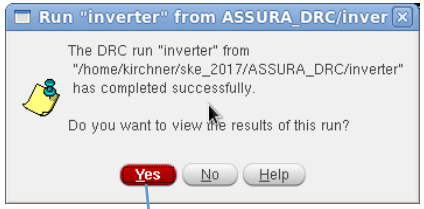
Assura -> Run DRC

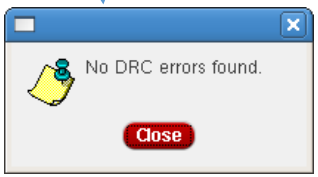


Set these switches to avoid some messages (see below!). What does "Coverage" mean?

Here you may open the rule set file for information. Contains all the rules like distances, overlap, min. width et cetera.







That's what we would like to see!

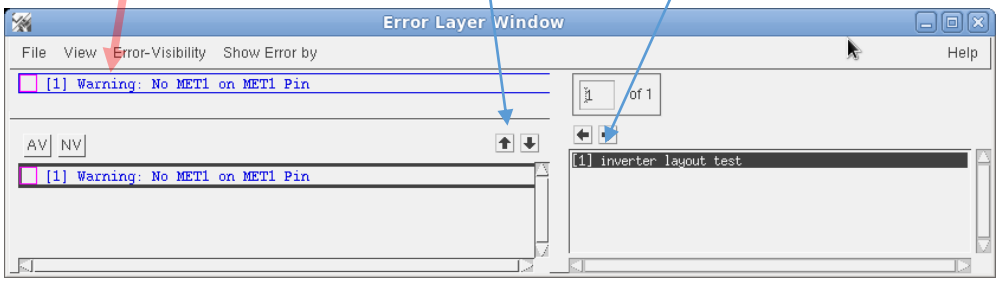
Cadence Layout – DRC with Errors remaining

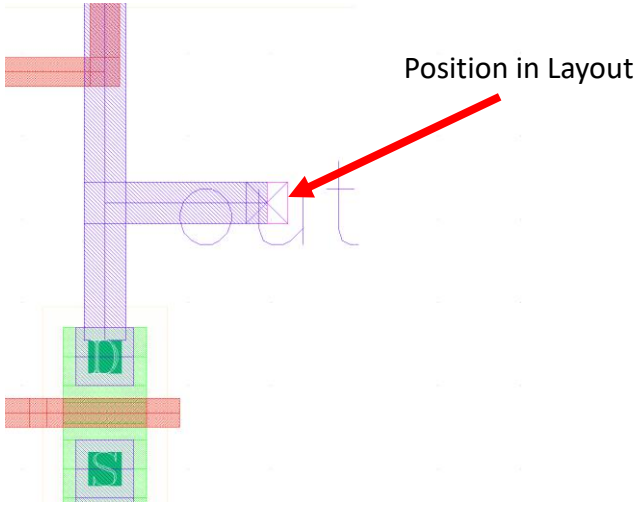
Example for an Error Message:
Here: Pin is not fully covered by metal

Violated Rule

Browse violated rules

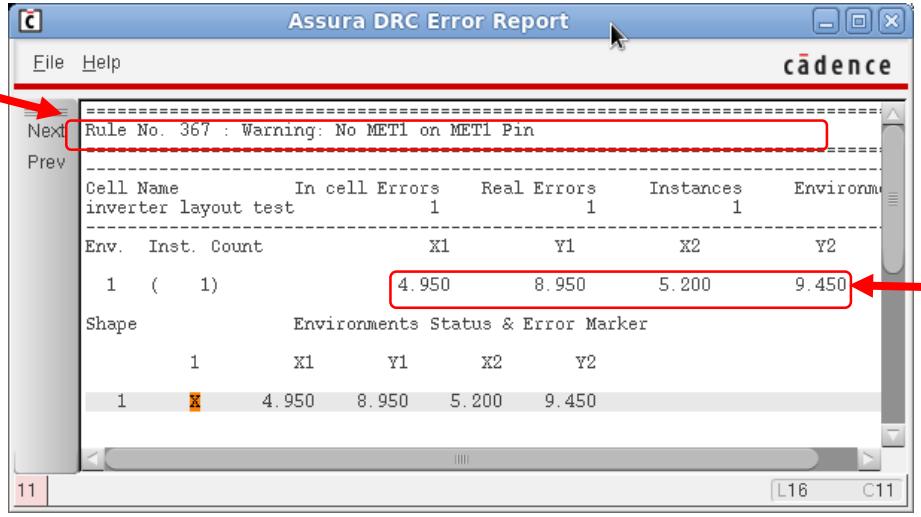
Browse Errors (if multiple)





View -> Error Report

Violated Rule

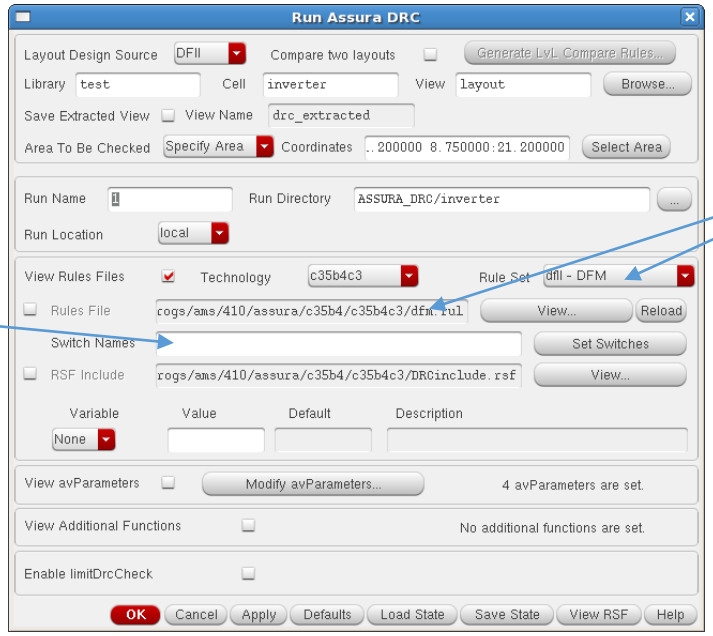


Position in Layout

Solutions:
Extend wire to the right or
add a rectangle in MET1 covering the Pin

Cadence Layout - DFM

Assura -> Run DRC

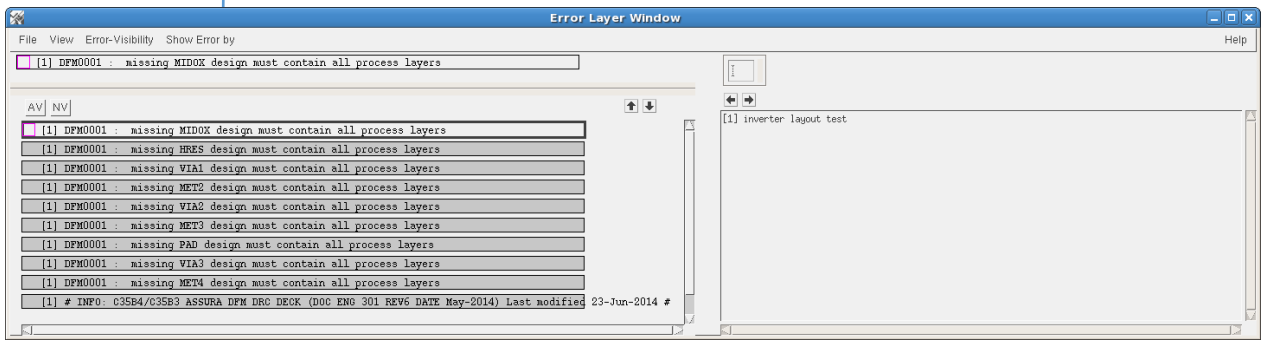


OPtion: extended ruleset DFM:
Design **F**or **M**anufacturing ->

Coverage of all but upper metal layer et cetera.

no switches!

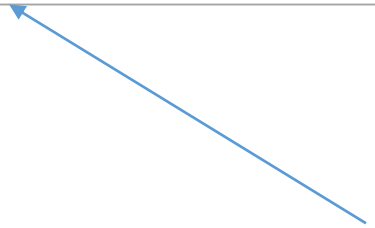
Errors because we did not use some layers.
Interesting for a top layout.



Cadence Layout - ERC

Electrical rule check is included in DRC.
There is no separate rule check in the ams-HITkit.

Starting ERC with Assura -> Run ERC opens a form similar to DRC with no technology selected and either rule files.

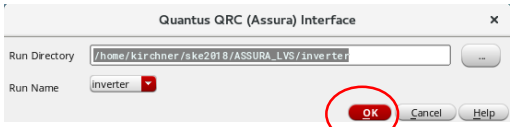


Up to now no verification for this.
Separate ERC-usage found nowhere.

Cadence Layout – QRC – Parametric Extraction

QRC -> Run Assura Quantus -QRC

no changes

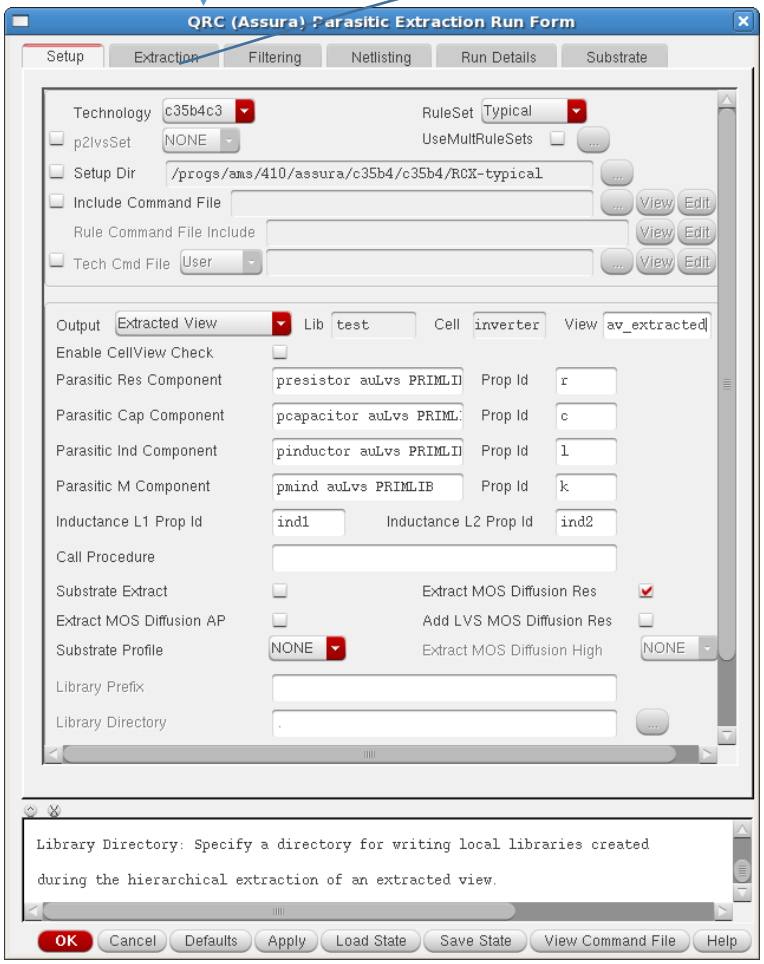


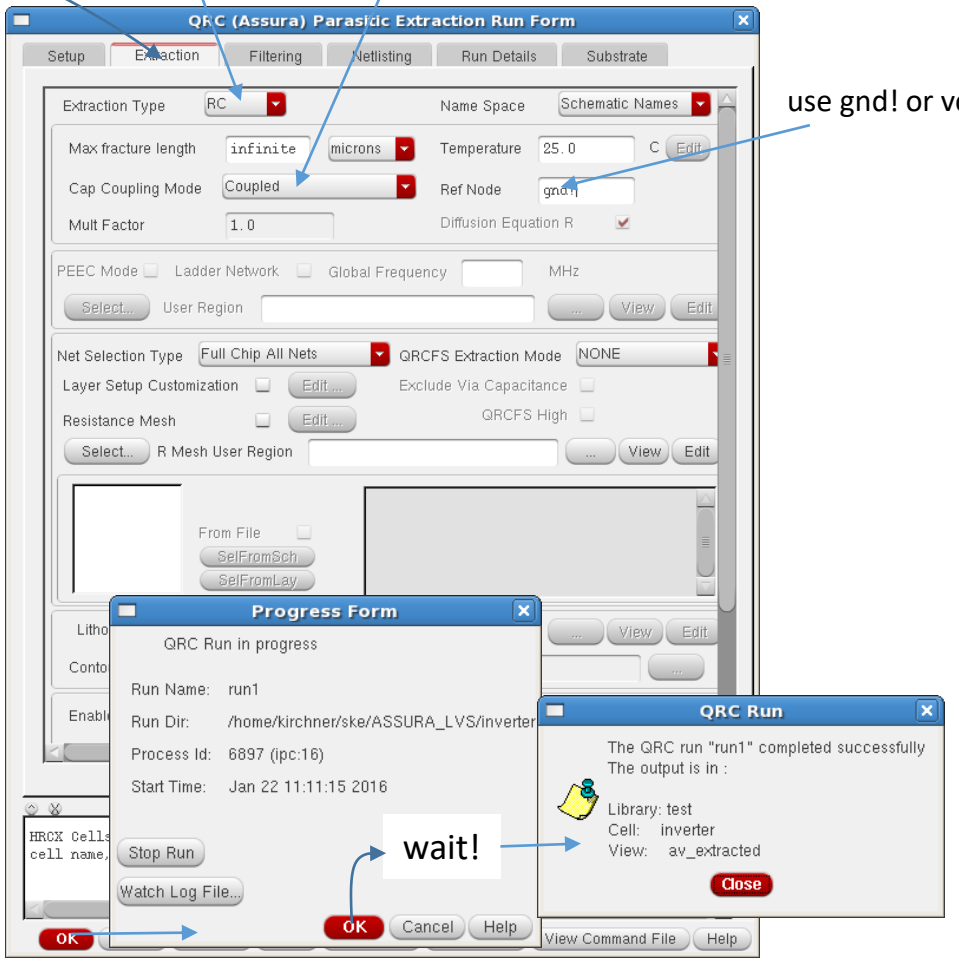
seit 6.1.7 dazwischengeschaltet

Coupled C: net to net (signals)
Decoupled C: net to power and ground only

RC

use gnd! or vcc!



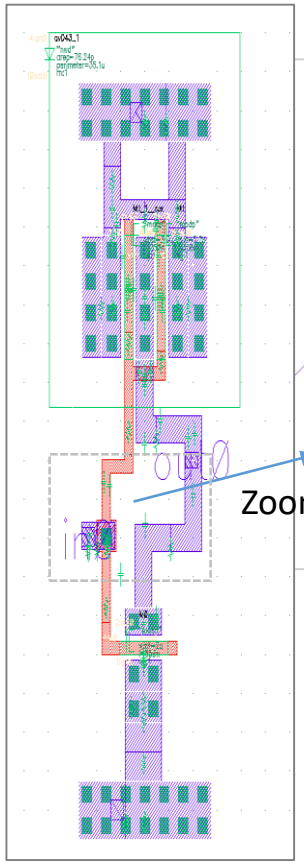


Cadence – QRC – Extracted view

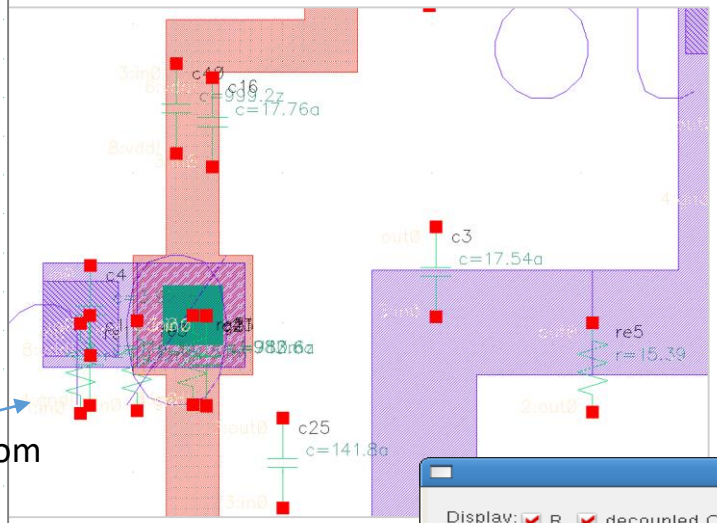
Open View "av_extracted" in Library Manager

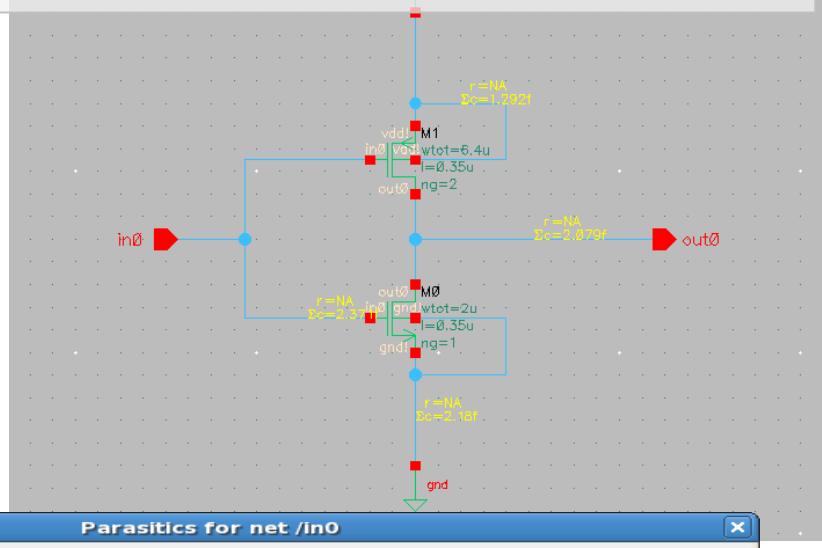
Maybe you must select all layers (up to 32) in Options -> Display once more

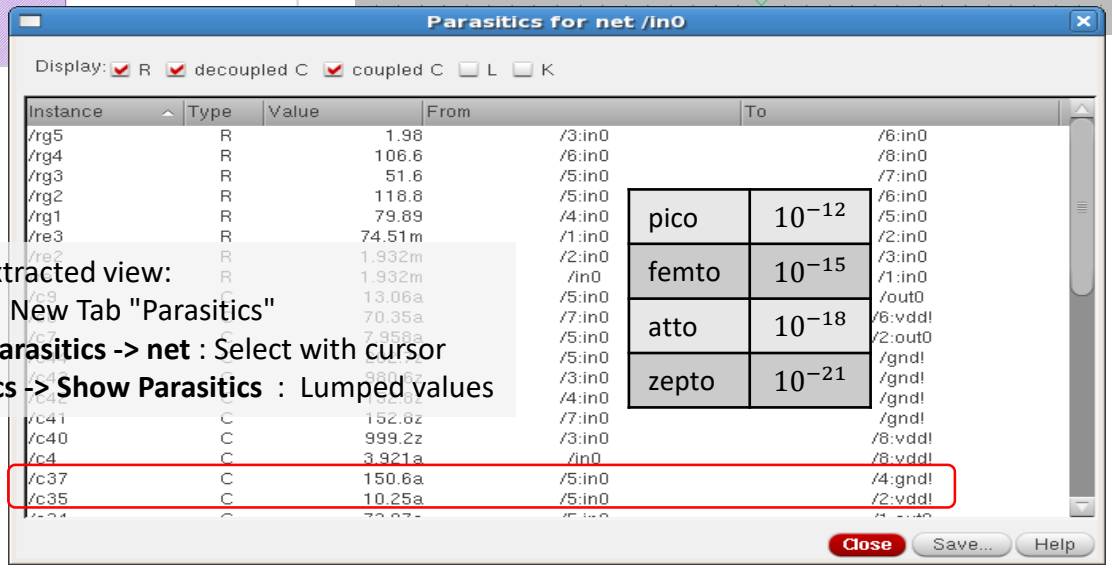
Launch -> Plugins ->Parasitics : New Tab "Parasitics"
Parasitics -> Setup Parasitics (gnd! and vdd! as reference nodes)



Zoom







pico	10^{-12}
femto	10^{-15}
atto	10^{-18}
zepto	10^{-21}

In Schematic or av_extracted view:
Launch -> Parasitics : New Tab "Parasitics"
Parasitics -> Report Parasitics -> net : Select with cursor
In Schematic **Parasitics -> Show Parasitics** : Lumped values

Try also: net to net
terminal to terminal (r)

Viewing parasitics may be interesting.
More important is their use in postlayout simulation.
They will be included in simulation netlists.

Cadence – QRC – Post-Layout Simulation (ADE-L/XL)

Open testbench (schematic)
Save as a new testbench and open it.
Copy the inverter and its load.

We need different models for the UUT (inverter)

- Original schematic
- Netlist with extracted parasitics.

Or in **CIW**:

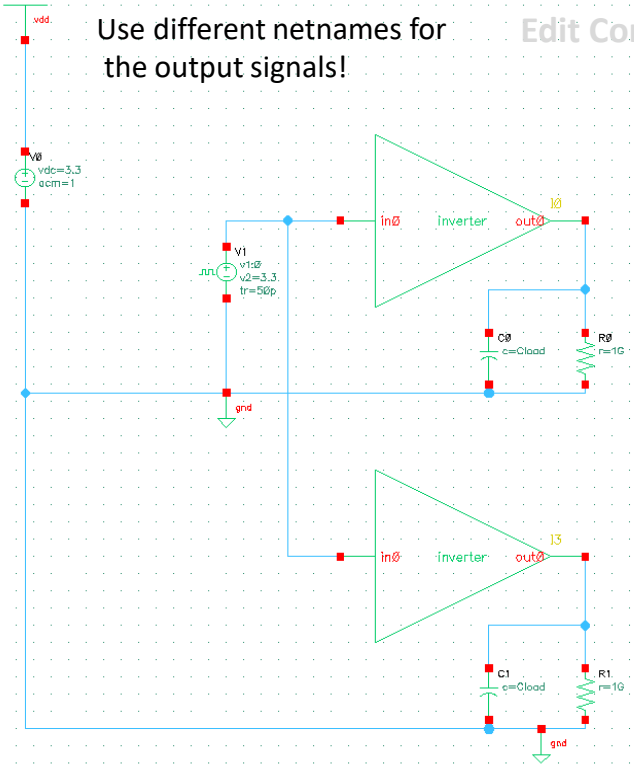
File -> New -> Cellview

In Schematic Editor:

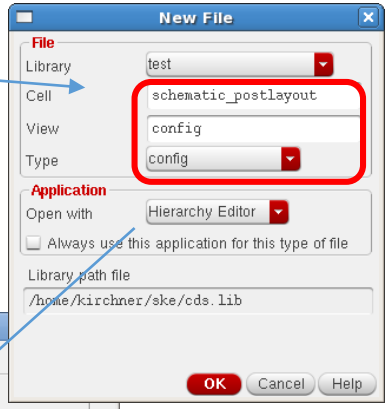
Launch -> Plugins -> Hierachy Editor

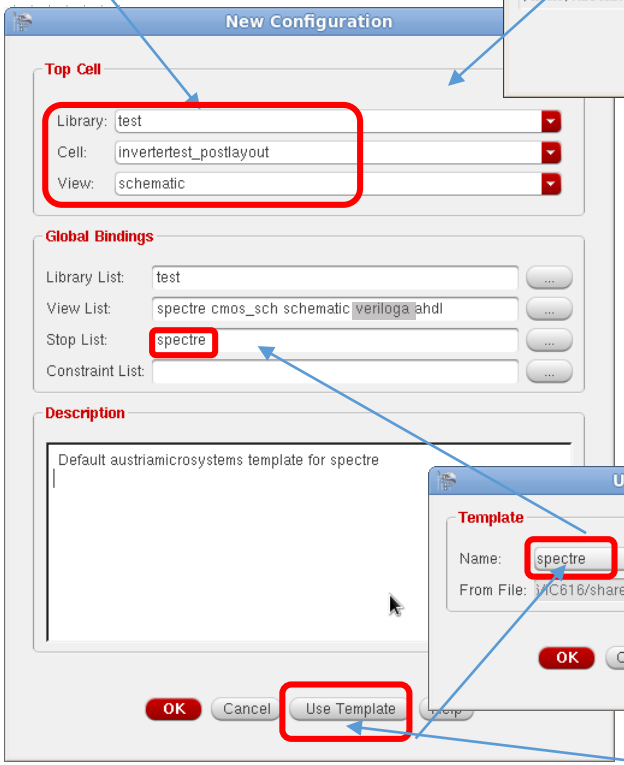
In new Tab "Hierarchy-Editor"

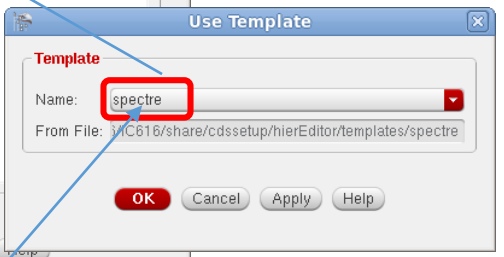
Edit Configuration



Use different netnames for the output signals!

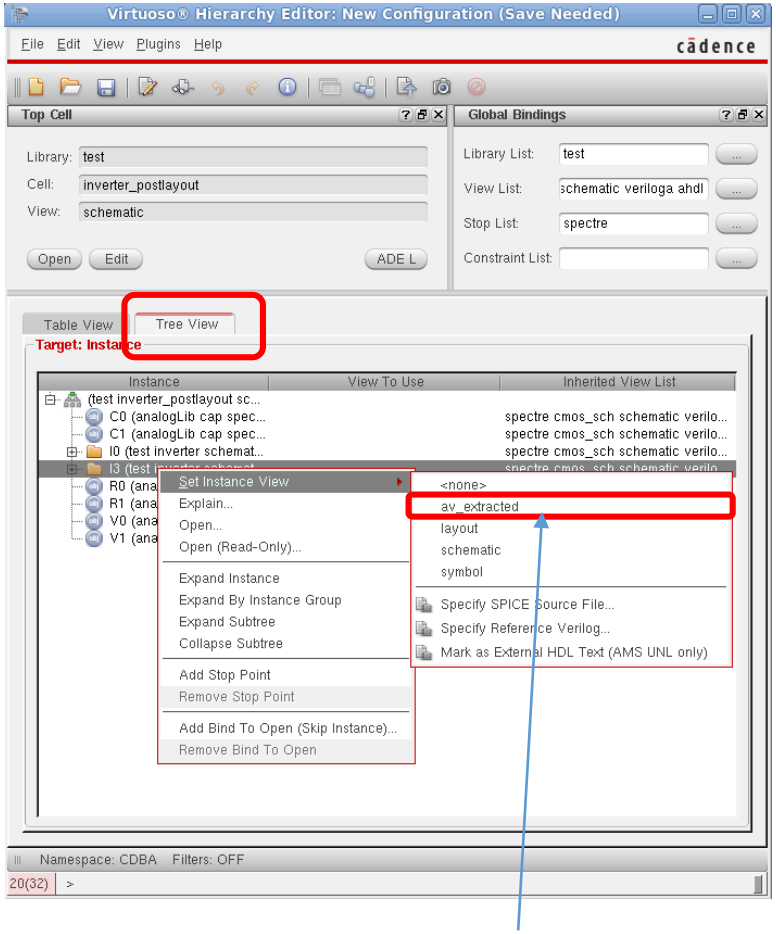


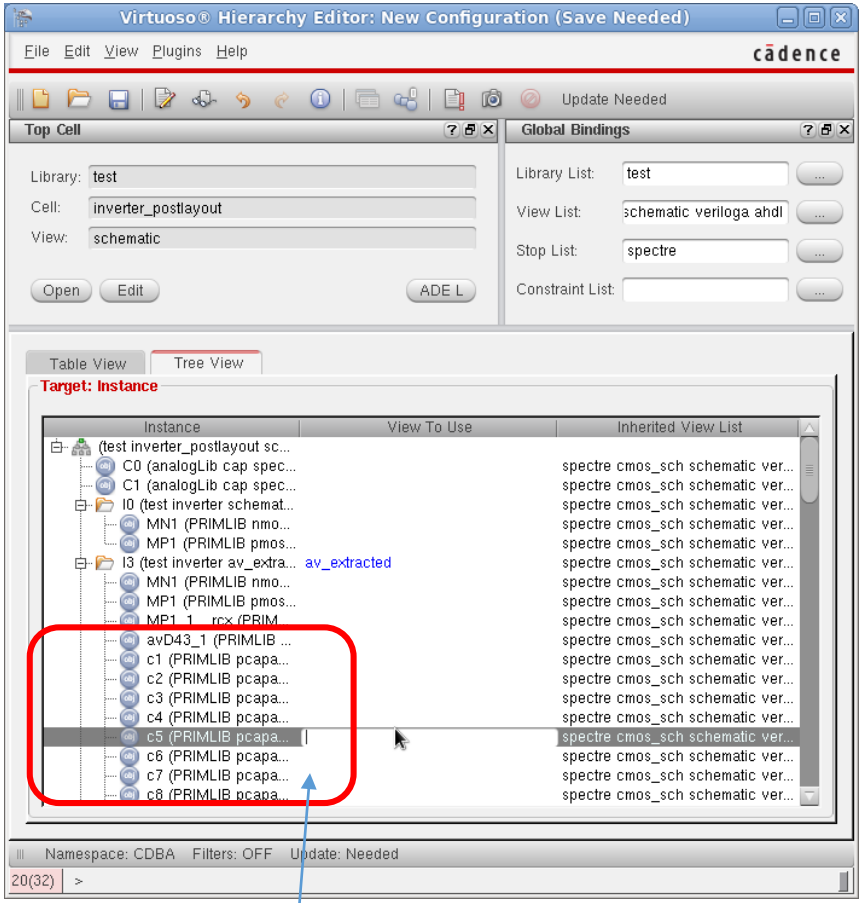




Begin here!
Template will fill the form in background.

Cadence – Post-Layout Simulation (ADE-L/XL)





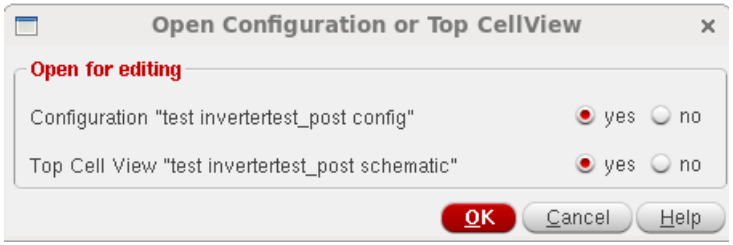
Parasitics

Replace (use RightMouse -> Set Instance View) schematic by av_extracted

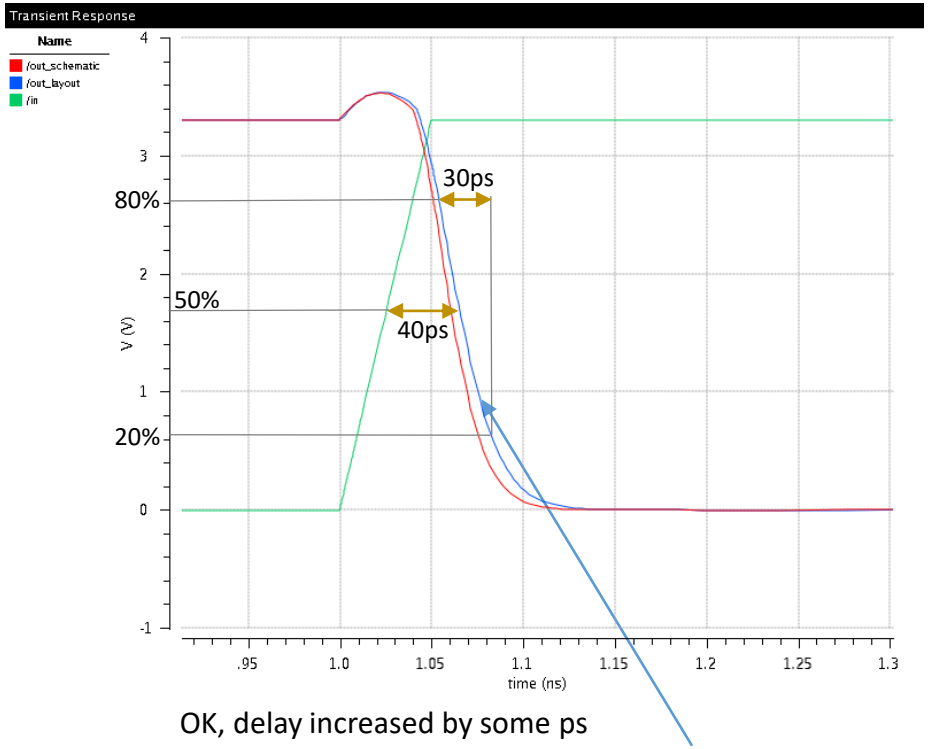
Now we have two different models for the two Inverters.

Cadence – Post-Layout Simulation - Result

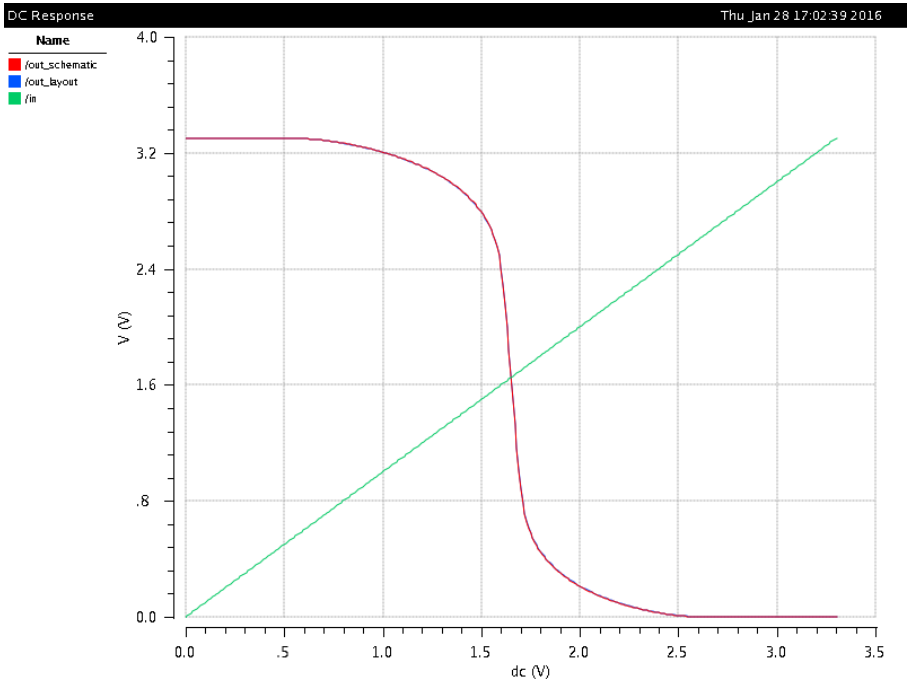
Open the configuration in Library Manager



To perform simulation see slides above from "Simulation ADE GXL Start"



OK, delay increased by some ps



OK, no visible change

Shown for C_{Load}= 4 fF. Less difference for higher load.

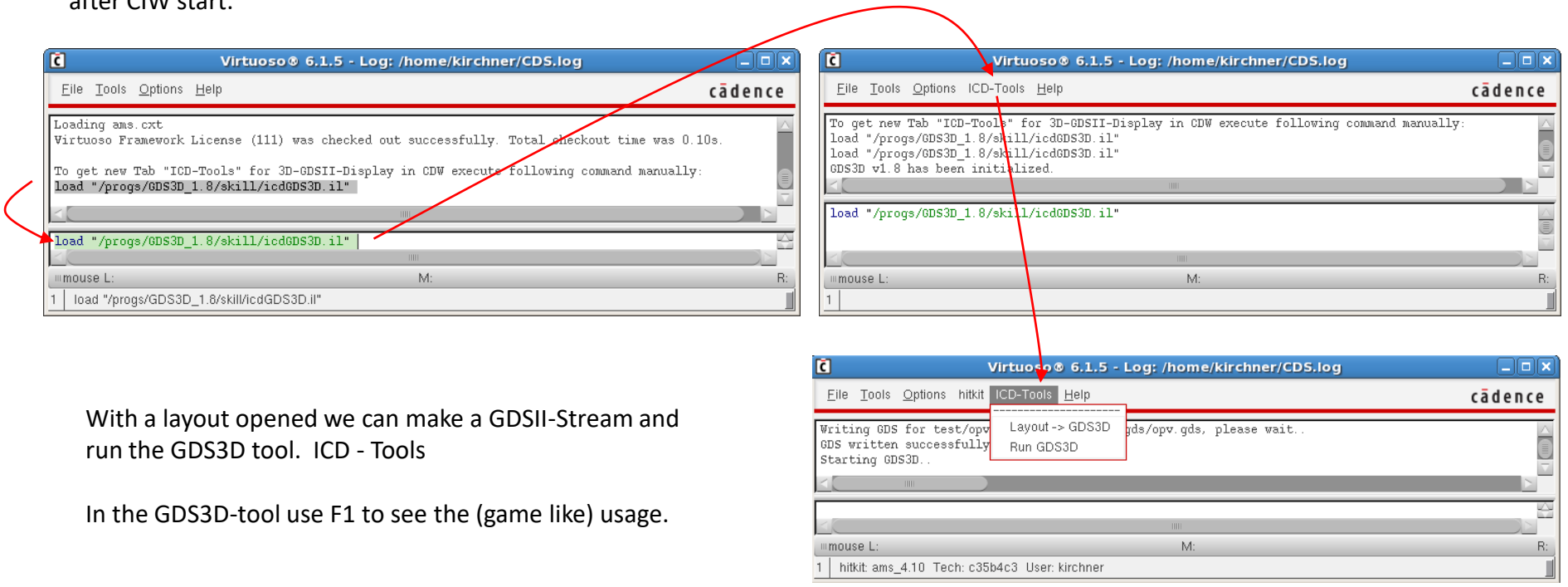
(if C_{Load} is higher parasitic capacitors have less influence)

Layout 3D View

GDS3D from University of Twente, NL

Needs a technology file (layer thickness, pitches). Generated for AMSC35B4 from process parameters.
Needs initialization for Cadence integration, but may be used standalone.

Automatic initialization does not work yet. For manual initialization observe the last output after CIW start.



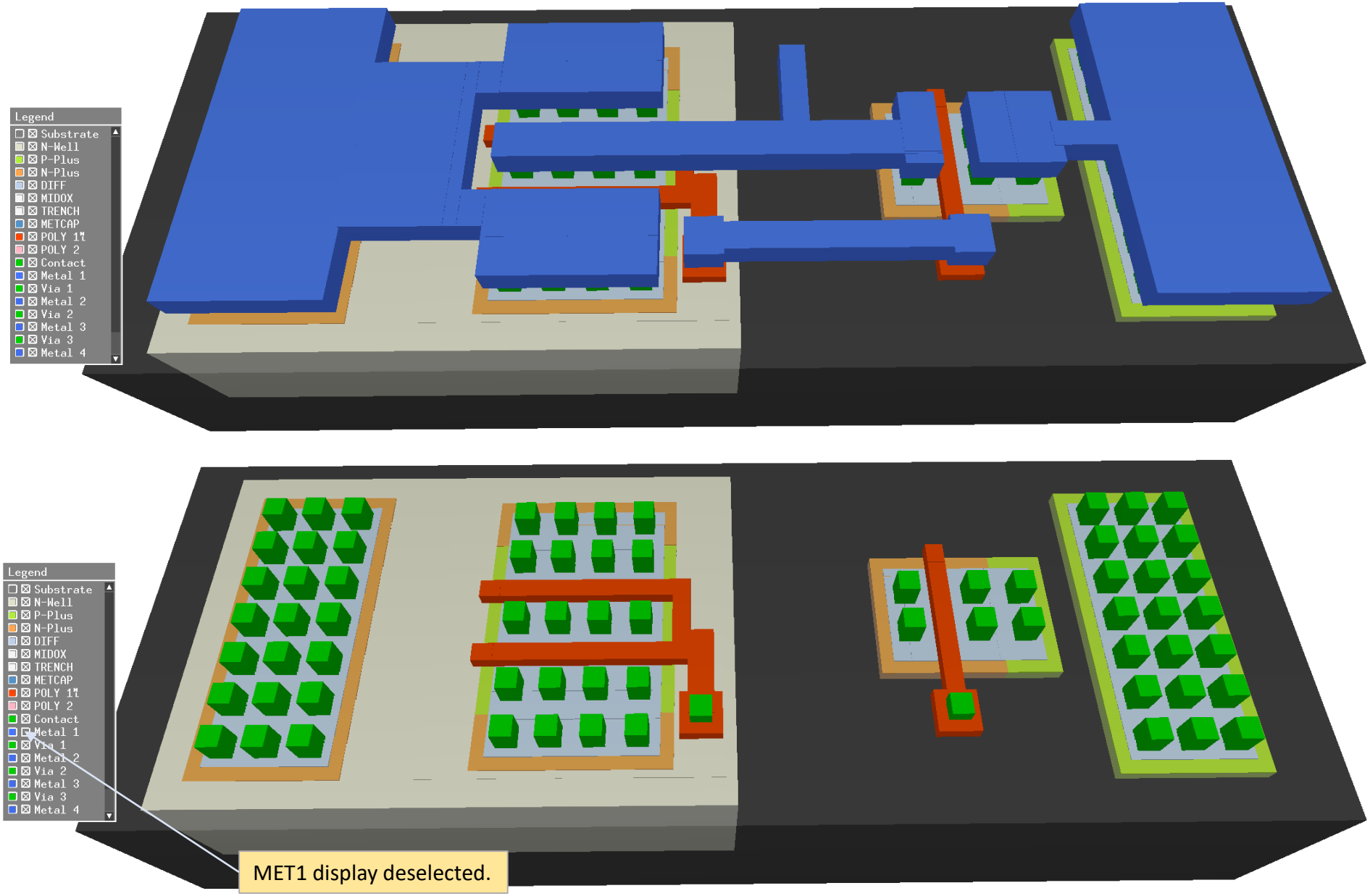
With a layout opened we can make a GDSII-Stream and run the GDS3D tool. ICD - Tools

In the GDS3D-tool use F1 to see the (game like) usage.

Do not use the normal streamout from CDW (File -> Export -> Stream) because GDS3D uses a separate directory for the gds-File!

ICD is simply **I**ntegrated **C**ircuit **D**esign group at Twente University)

Layout 3D View



Advanced Simulation

Monte Carlo simulation using matching parameter

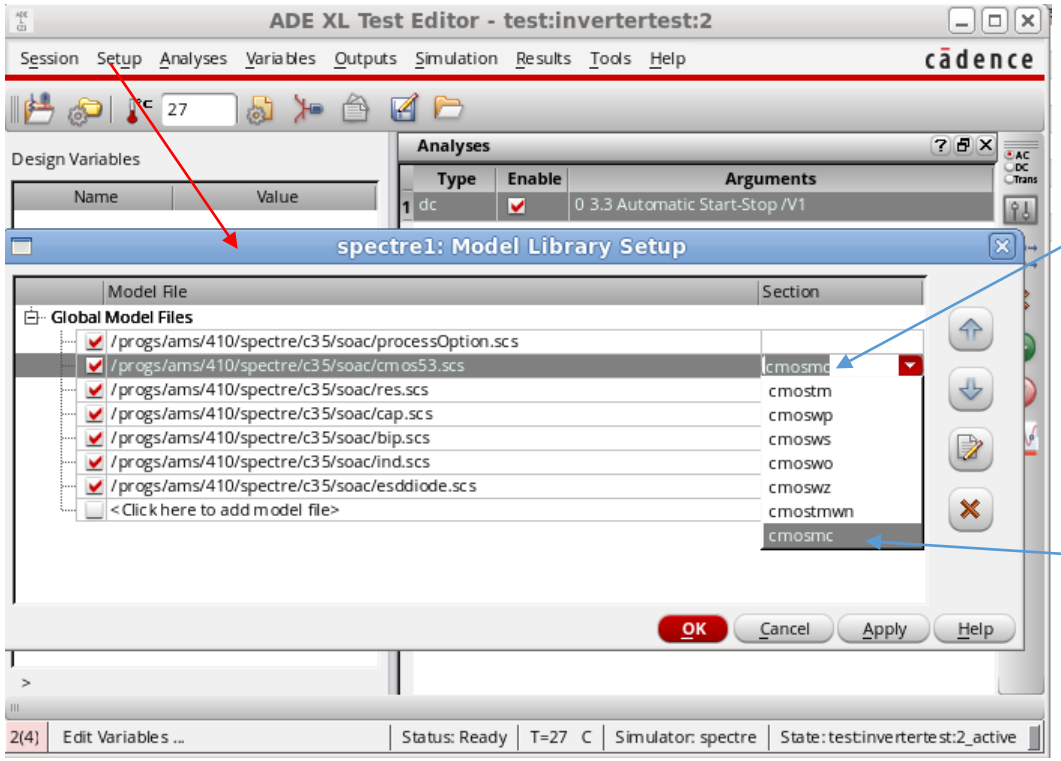
Open testbench schematic -> Launch ADE-XL -> existing view ADE-XL (assuming we have such a view already)

Use one of the tests from the normal schematic simulation

Here we use the dc-analyses to investigate the transfer characteristic.

RM over name of the test (e.g. test:name:19 → "Open Test Editor"

With Setup-> Model Libraries: Select cmosmc for the transistors (we have only transistors here we could select …mc for other parts)



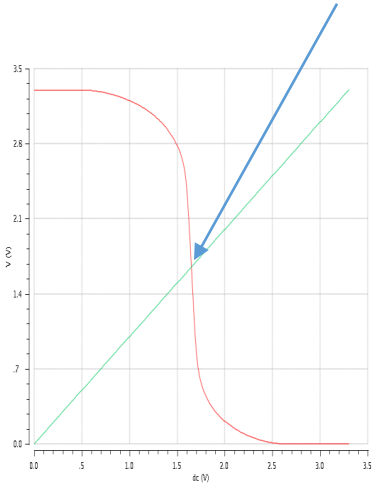
Dubbleclick here to open choices

…mc – Monte Carlo

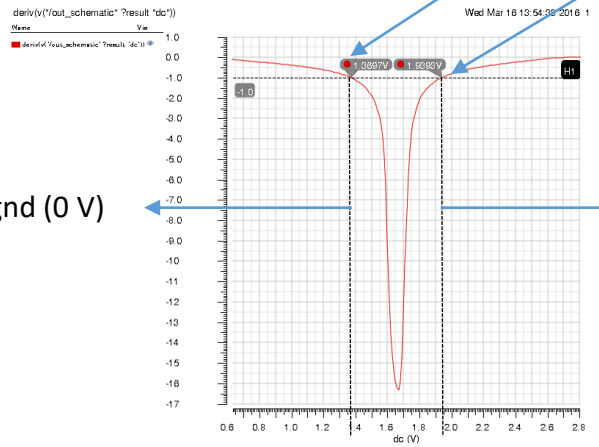
Advanced Simulation

Monte Carlo simulation using matching parameter

We want to see the switching point ($V_{out} = V_{in}$) and the noise margin for "low" and "high" output.



Difference to gnd (0 V)



Difference to vdd (3.3 V)

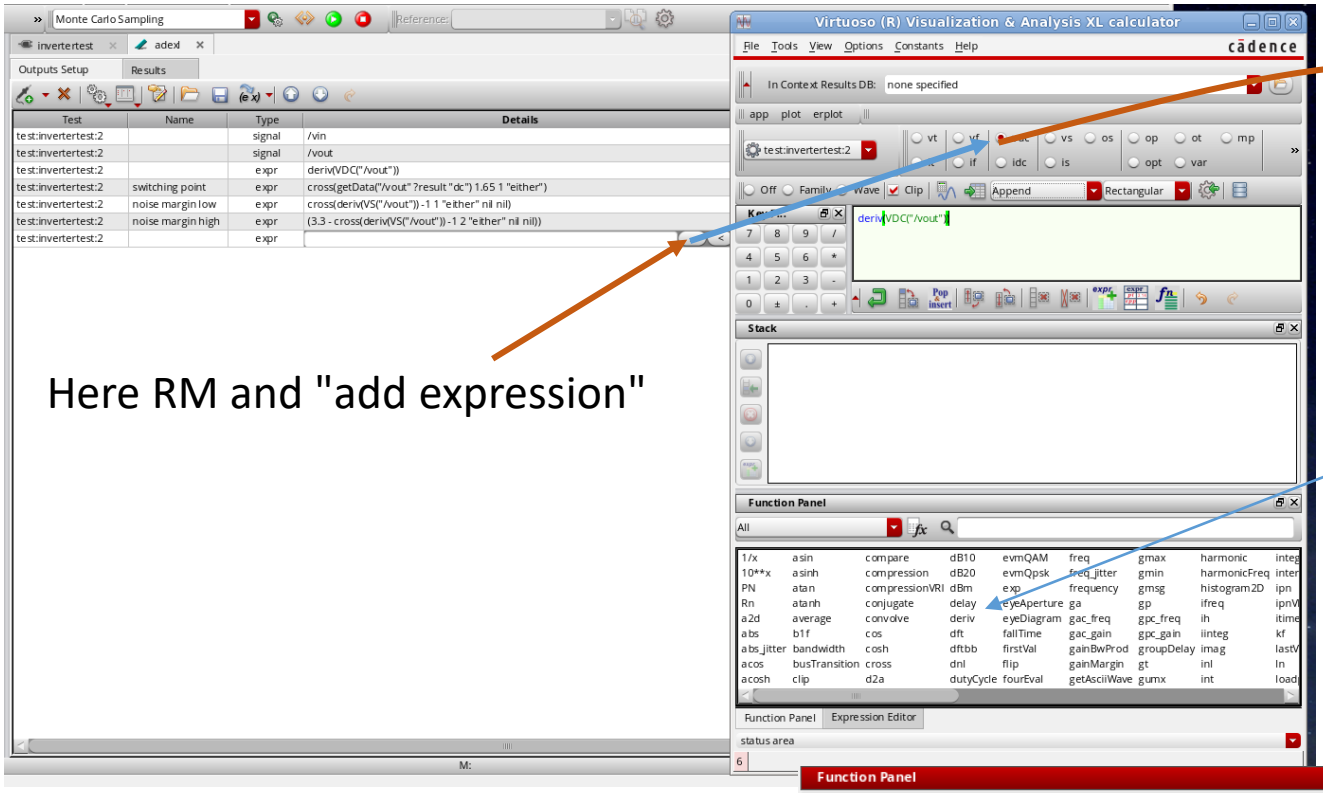
We investigate the following expressions:

Switching point:	cross(VDC("/vout") 1.65 1 "either" nil)
Low logic value noise margin:	cross(deriv(VDC("/vout")) -1 1 "either" nil)
High logic level noise margin:	(3.3 - cross(deriv(VDC("/vout")) -1 2 "either" nil))

To set the output expressions: "add expression" - > open calculator

Advanced Simulation

Monte Carlo simulation using matching parameter

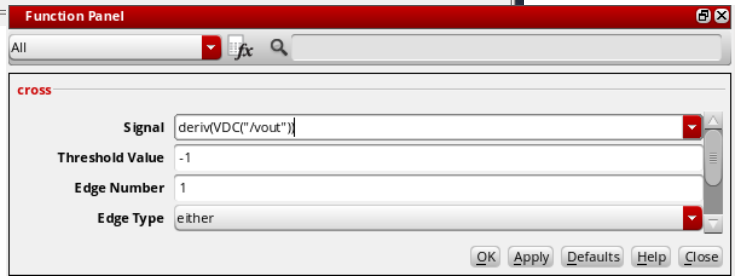


Select DC-signal vout from schematic

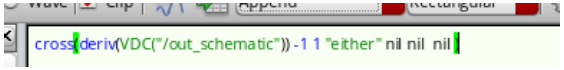
Here RM and "add expression"

Use the **deriv** and **cross** functions

cross gives the vin-value if deriv(vout)= -1 first time

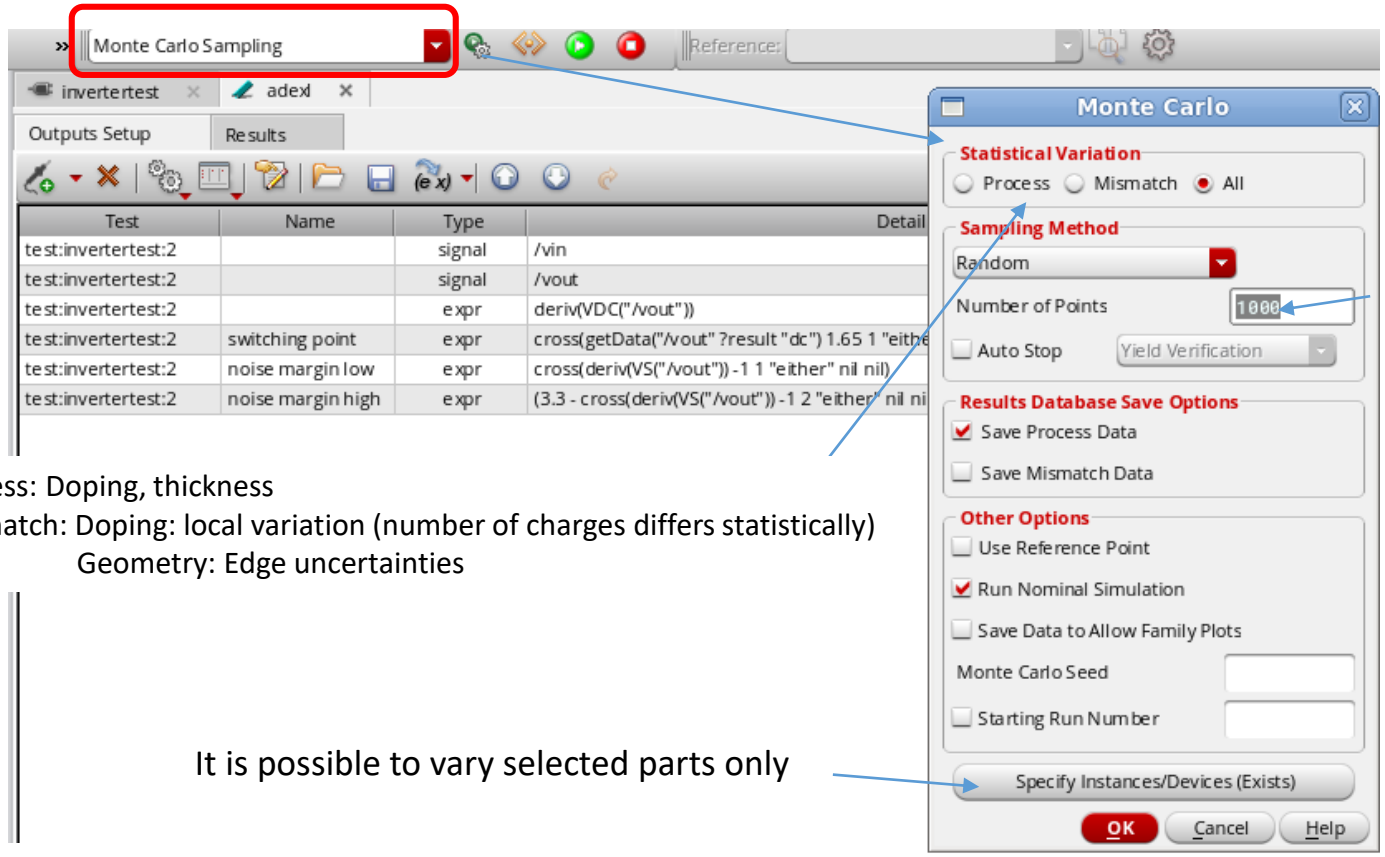


For the LOW noise margin we use the "cross"-value, for the HIGH noise margin we use 3.3-"cross"-value



Advanced Simulation

Monte Carlo simulation using matching parameter



n simulation runs with random values

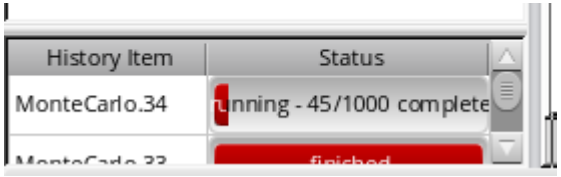
Process: Doping, thickness

Mismatch: Doping: local variation (number of charges differs statistically)

Geometry: Edge uncertainties

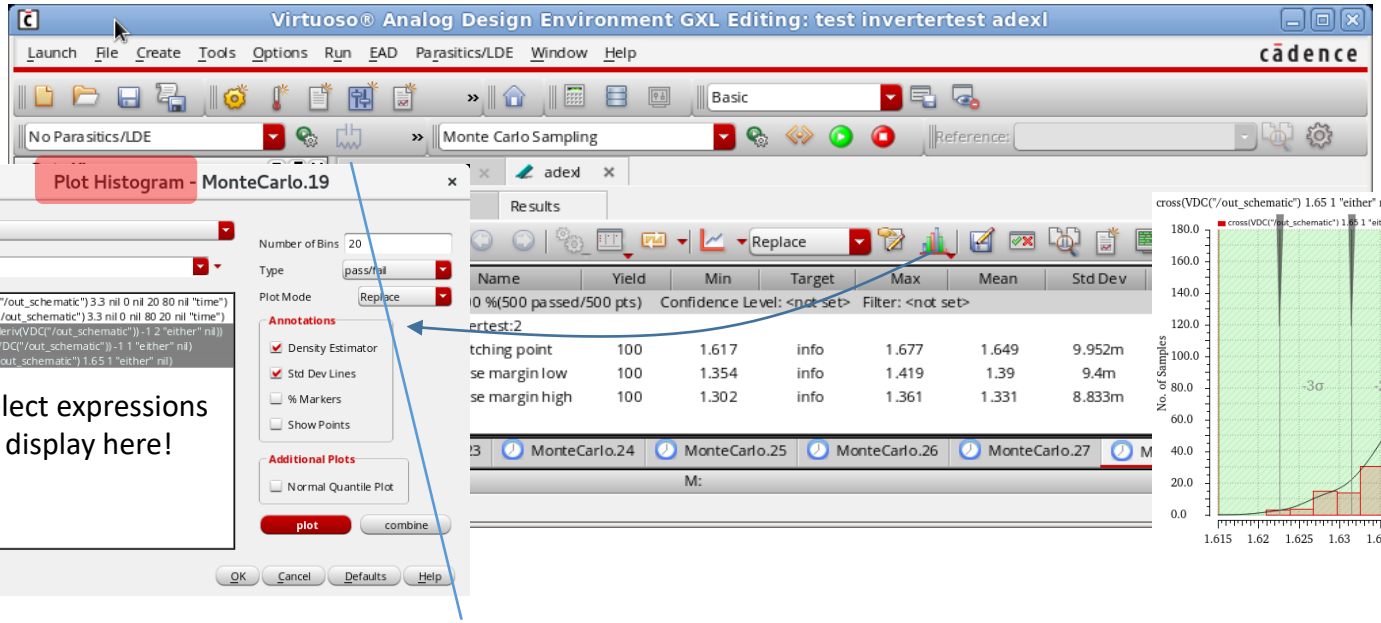
It is possible to vary selected parts only

See it running in the buttom left corner

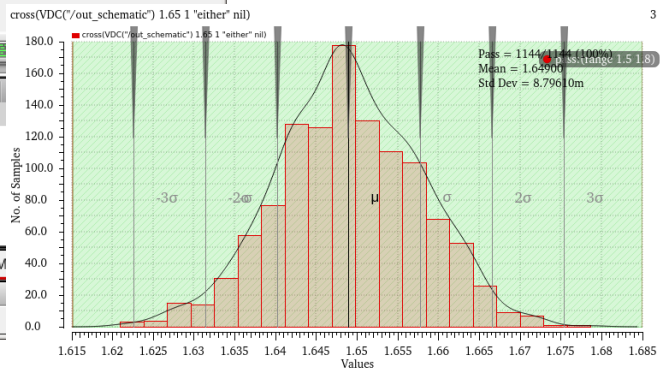


Advanced Simulation

Monte Carlo simulation using matching parameter



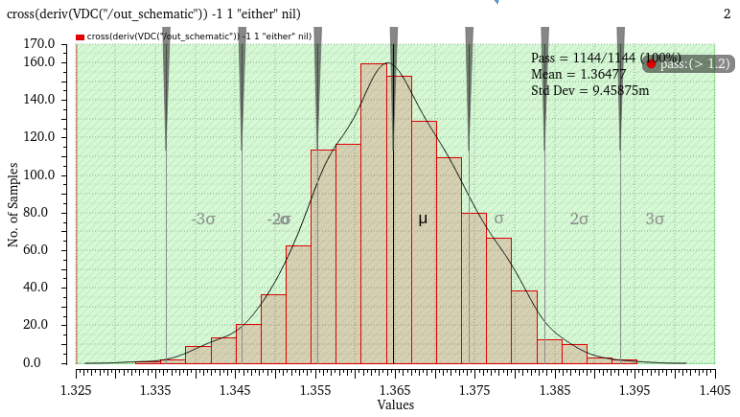
switching point



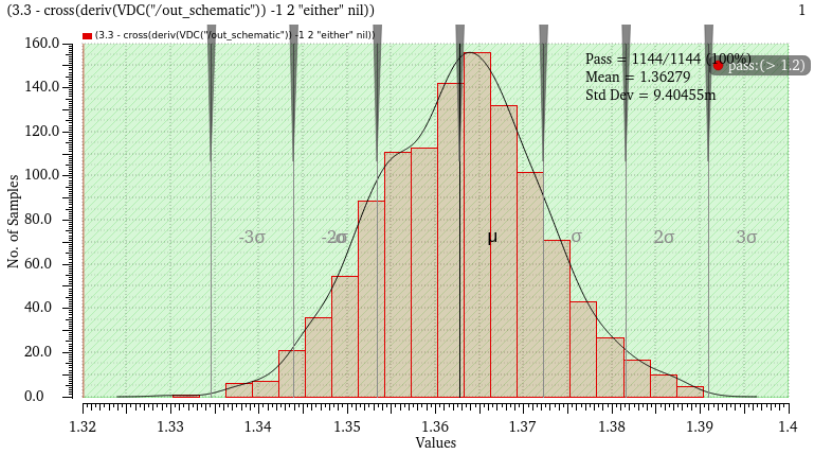
Number of intervals, plots show 20 intervals

Result: Histogram

low level margin



high level margin

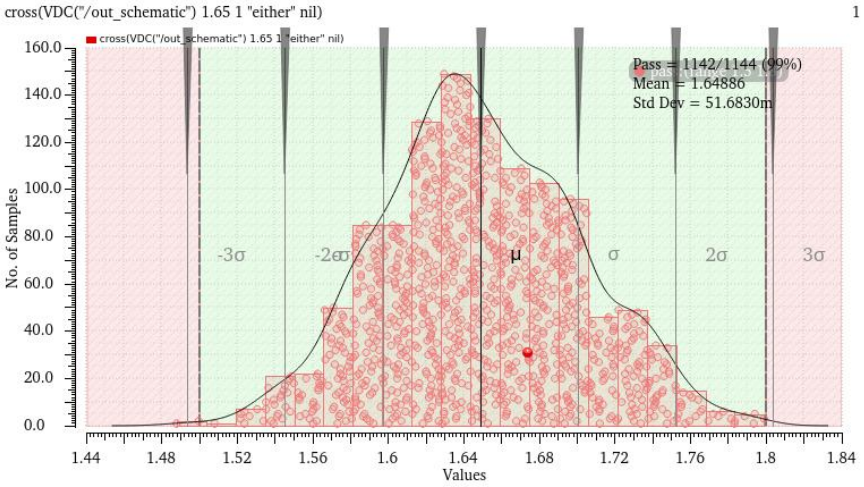


Distribution of noise margins (mismatch only)

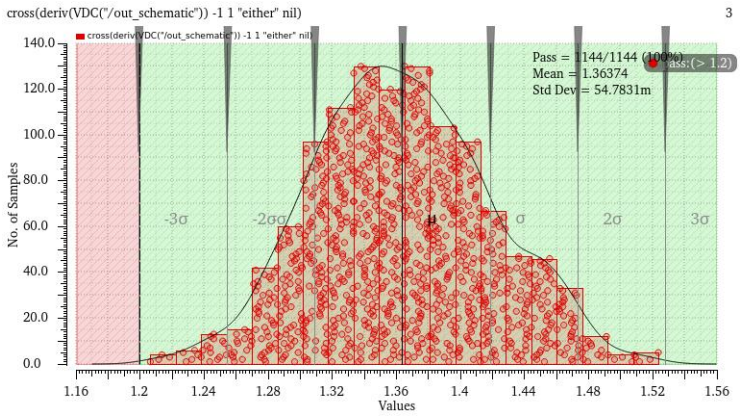
Advanced Simulation

Monte Carlo simulation using matching parameter

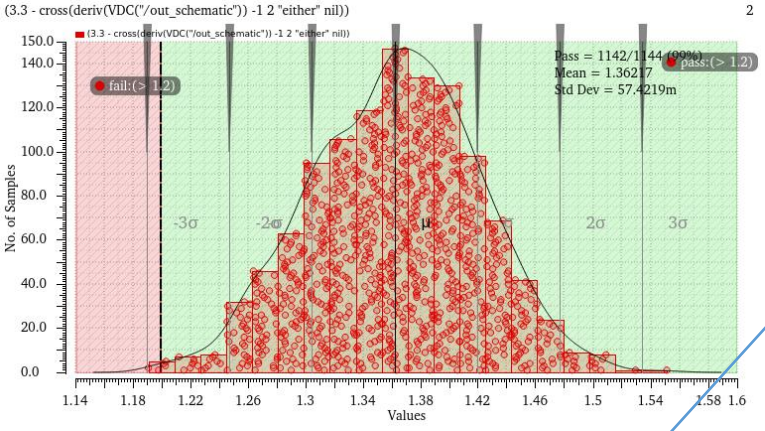
Switching Point

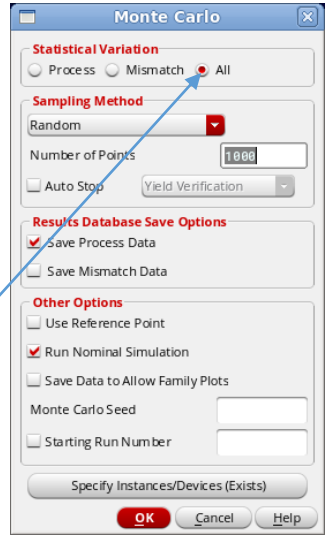


Low level margin



High level margin





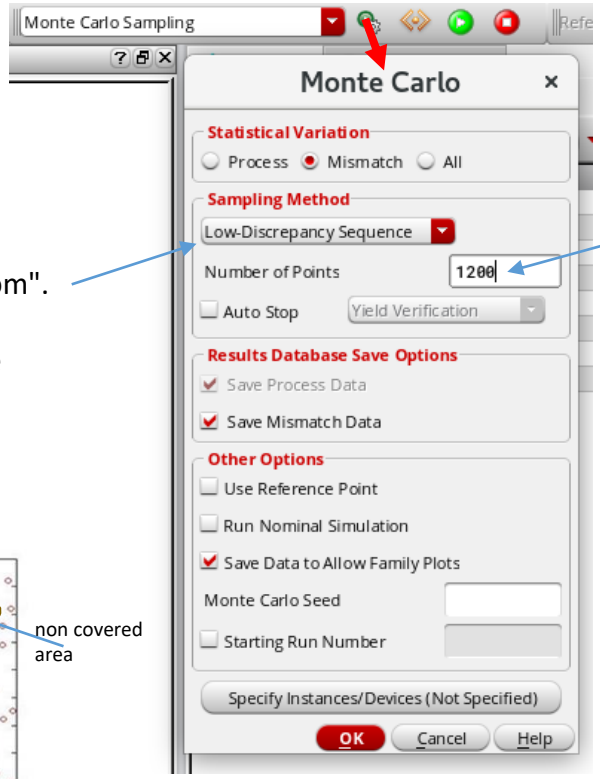
Distribution of noise margins (combined mismatch and process variaton)

Advanced Simulation

Monte Carlo simulation and yield prediction

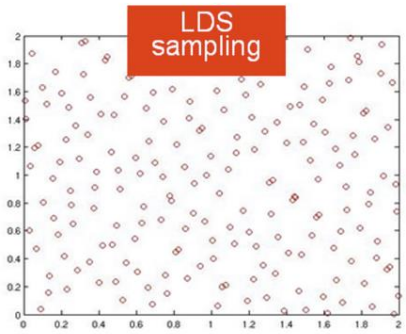
Define (realistic) specs for characteristics: Inverter: $V_{inHL}, V_{mHigh}, V_{mLow}$ ...

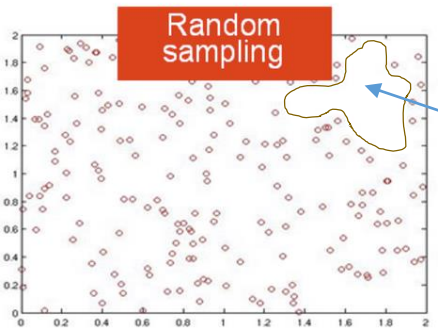
Set Options for Monte Carlo Simulation:



Recommended to have enough samp

Better than simple "Random".
Better covering of the
n-dimensional input scope





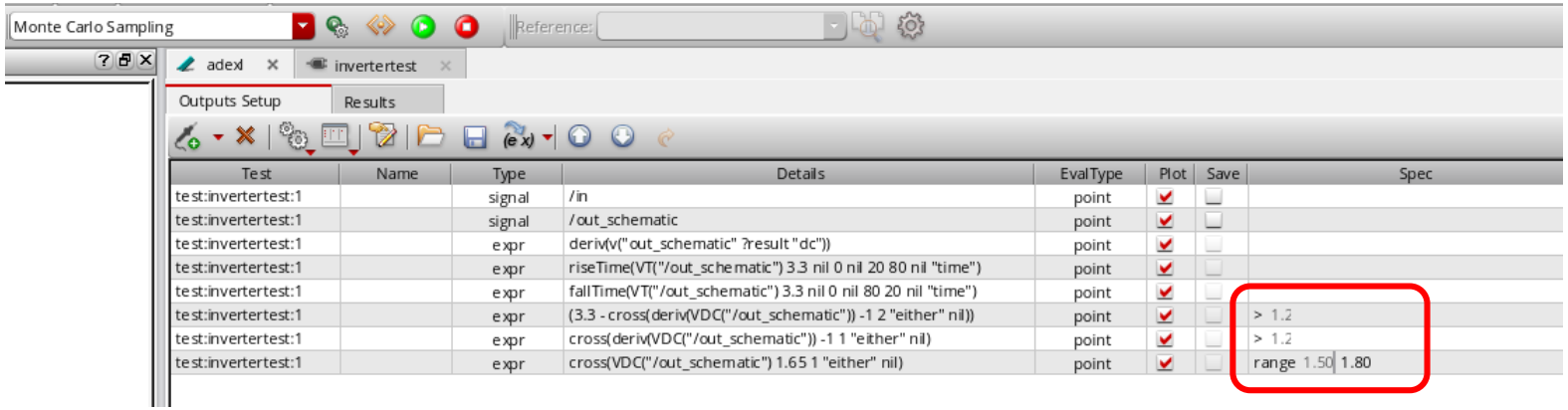
From: https://community.cadence.com/cadence_blogs_8/b/cic/posts/the-art-of-analog-design-part-2-monte-carlo-sampling

Advanced Simulation

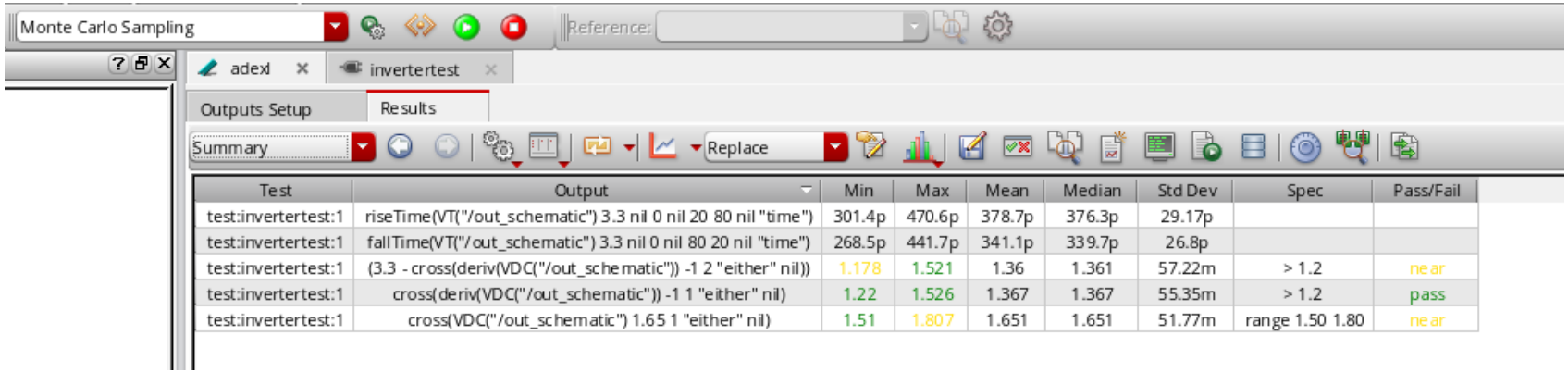
Monte Carlo simulation and yield prediction

Set specs in adexl outputs window:

low level margin > 1.2 V
high level margin > 1.2 V
1.50 V < switching voltage < 1.80 V



Test	Name	Type	Details	EvalType	Plot	Save	Spec
test:invertertest:1		signal	/in	point	✓		
test:invertertest:1		signal	/out_schematic	point	✓		
test:invertertest:1		expr	deriv(v("out_schematic" ?result "dc"))	point	✓		
test:invertertest:1		expr	riseTime(VT("/out_schematic") 3.3 nil 0 nil 20 80 nil "time")	point	✓		
test:invertertest:1		expr	fallTime(VT("/out_schematic") 3.3 nil 0 nil 80 20 nil "time")	point	✓		
test:invertertest:1		expr	(3.3 - cross(deriv(VDC("/out_schematic")) -1 2 "either" nil))	point	✓		> 1.2
test:invertertest:1		expr	cross(deriv(VDC("/out_schematic")) -1 1 "either" nil)	point	✓		> 1.2
test:invertertest:1		expr	cross(VDC("/out_schematic") 1.65 1 "either" nil)	point	✓		range 1.50 1.80

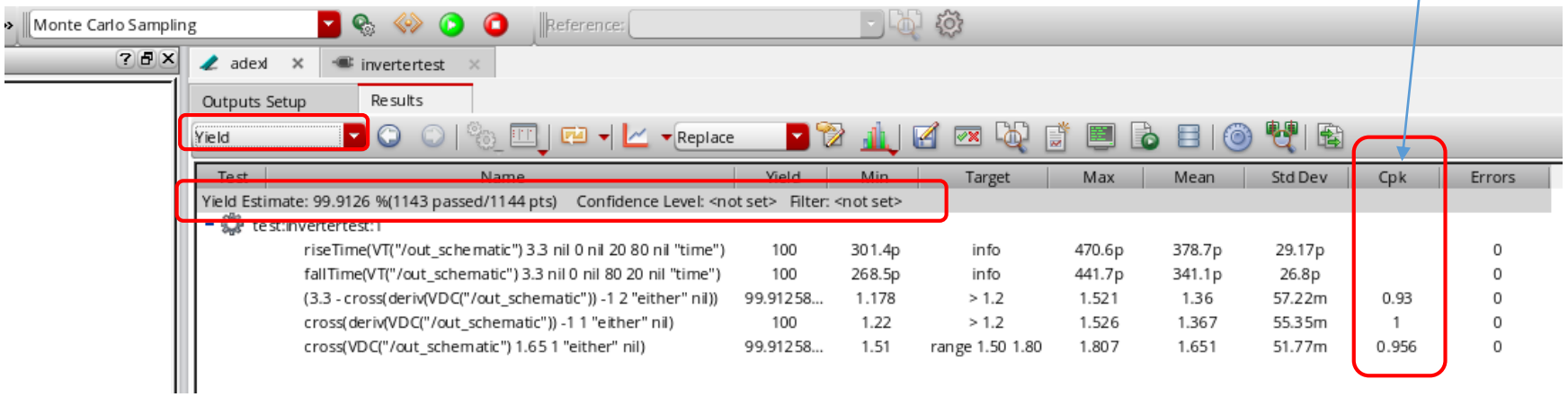


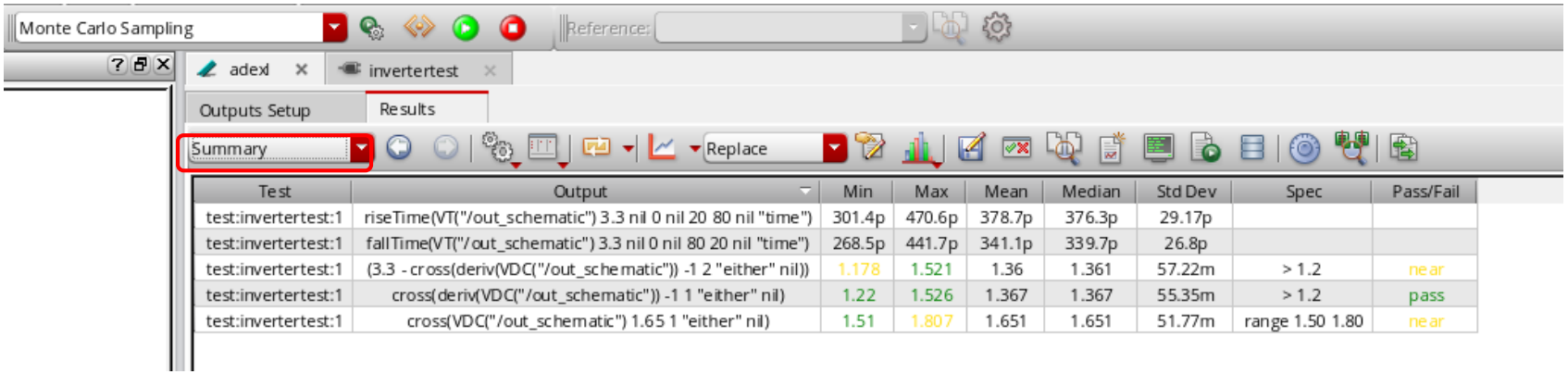
Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
test:invertertest:1	riseTime(VT("/out_schematic") 3.3 nil 0 nil 20 80 nil "time")	301.4p	470.6p	378.7p	376.3p	29.17p		
test:invertertest:1	fallTime(VT("/out_schematic") 3.3 nil 0 nil 80 20 nil "time")	268.5p	441.7p	341.1p	339.7p	26.8p		
test:invertertest:1	(3.3 - cross(deriv(VDC("/out_schematic")) -1 2 "either" nil))	1.178	1.521	1.36	1.361	57.22m	> 1.2	near
test:invertertest:1	cross(deriv(VDC("/out_schematic")) -1 1 "either" nil)	1.22	1.526	1.367	1.367	55.35m	> 1.2	pass
test:invertertest:1	cross(VDC("/out_schematic") 1.65 1 "either" nil)	1.51	1.807	1.651	1.651	51.77m	range 1.50 1.80	near

Advanced Simulation

Monte Carlo simulation and yield prediction

Next slide!





Be aware that we did not change opereating environment (temperature, supply voltage)

Monte Carlo simulation and yield prediction

C_p und C_{pk} Process Capability Statistics

C_p shows the relation beetwen Engeneering Tolerance (specs) to the Natural Tolerance (process) for a process with a distribution centered beetween specifications. For the Natural Tolerance the 6σ-interval $\pm 3\sigma$ is commonly used

Upper Spec Limit

Lower Spec Limit

$$C_p = \frac{USL - LSL}{6\sigma}$$

what the designer wants (specs)

what the process can deliver with high certainty

upper or lower limit only

$$C_p = \frac{USL - \mu}{3\sigma}$$

$$C_p = \frac{\mu - LSL}{3\sigma}$$

Mostly the distribution is not centered and the corrected value is used (maybe used for centered distribution as well):

Mittelwert

$$C_{pk} = \frac{minimum(USL - \mu), (\mu - LSL)}{3\sigma}$$

If $C_{pk} = 1$ then 99.73% of the samples will meet specs, for $C_{pk} = 2$: 99.9999998%

"Recommended": Values beetween 1.25 to 2.0 dependend on safety demands
> 2.5 area reduction possible? cost!

Advanced Simulation

Corner Simulation

FEOL (front end of line) Corners: Transistors n-channel , p-channel

all processes used for individual parts (transistors, resistors)

"**Fast**" means "best":

-thin oxide

-smaller length

-higher width

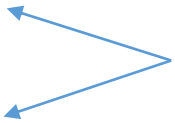
TT : typical n-channel- and p-channel-FETs

SS : slow n-channel-FET, slow p-channel-FET

SF : slow n-channel-FET, fast p-channel-FET

FS : fast n-channel-FET, slow p-channel-FET

FF : fast n-channel-FET, fast p-channel-FET



transistors affected in simila

Corners affect not only speed but also transfer characteristics (dc-dc)

BEOL (back end of line) Corners: Wires

all processes after making parts -> wires, vias

Temperature, Voltage

ams (and others):

TM: typical values - corresponds to TT

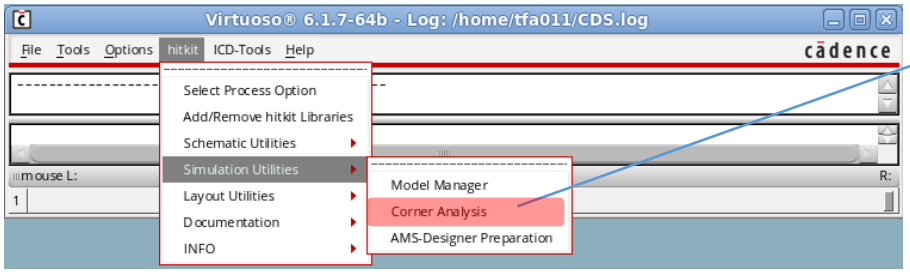
WS : worst slow – slow n and slow p corresponds to SS

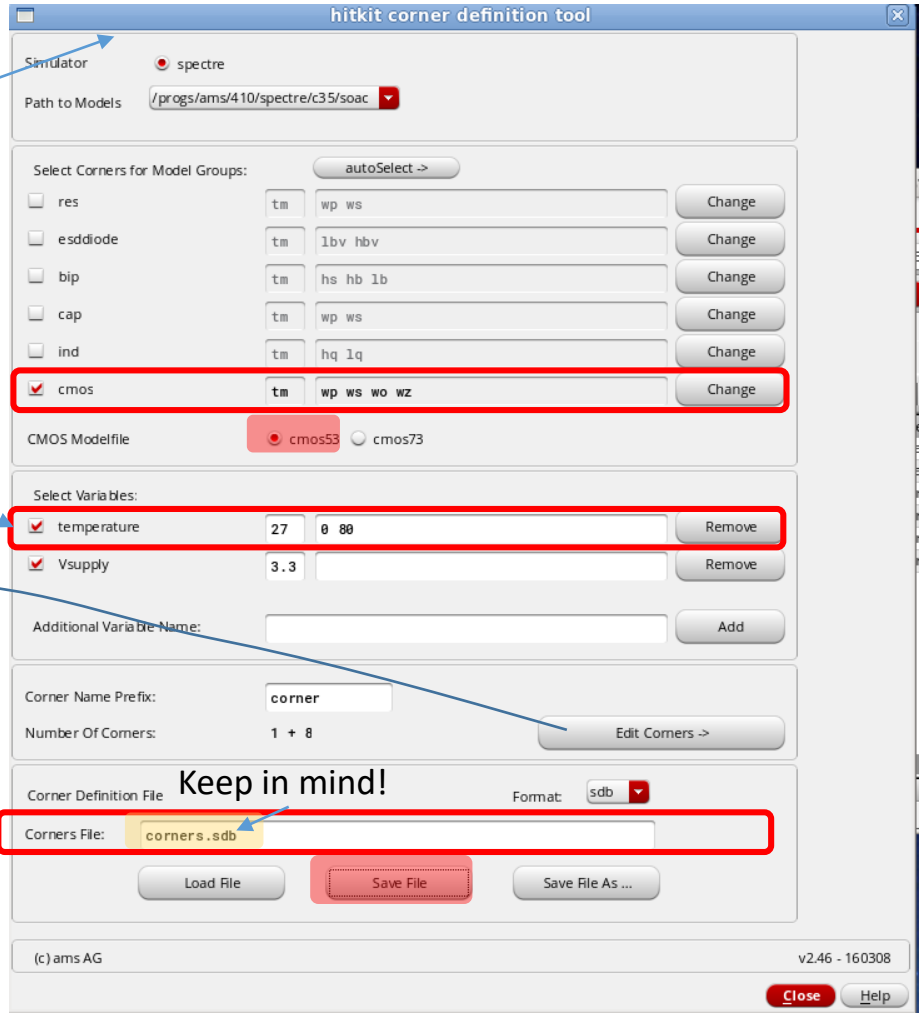
WP: worst power – fast n and fast p corresponds to FF

WO : worst One – slow n, fast p corresponds to SF

WZ: worst Zero – fast n, slow p corresponds to FS

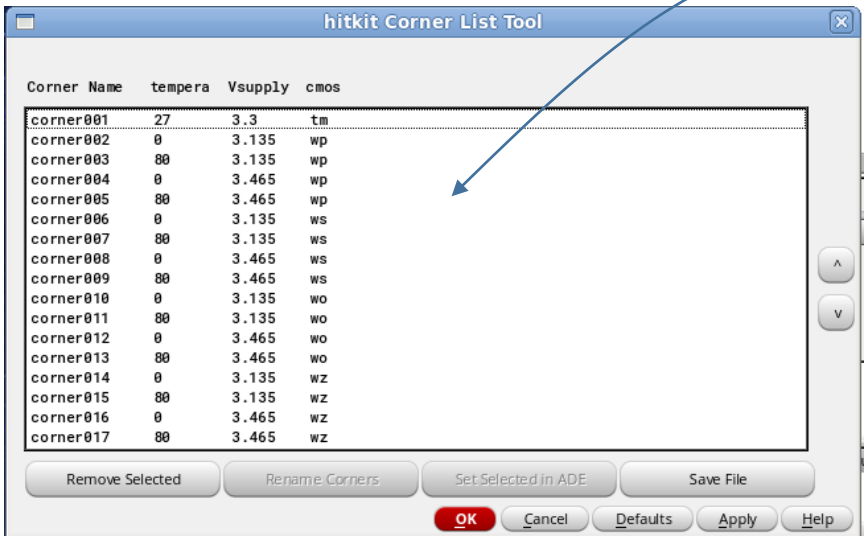
Corner Simulation – Corner Preparation





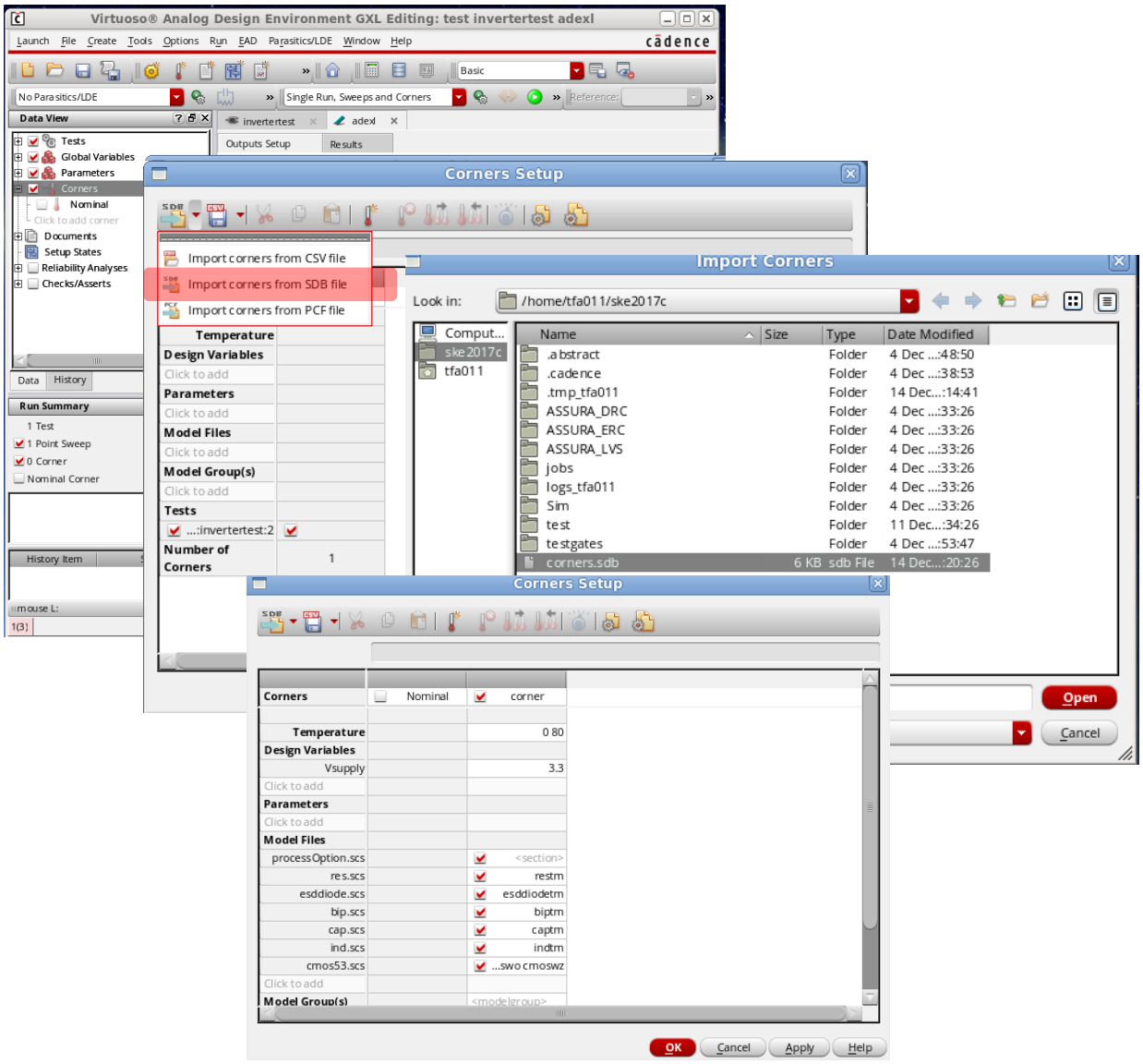
Modification of temperature

Keep in mind!

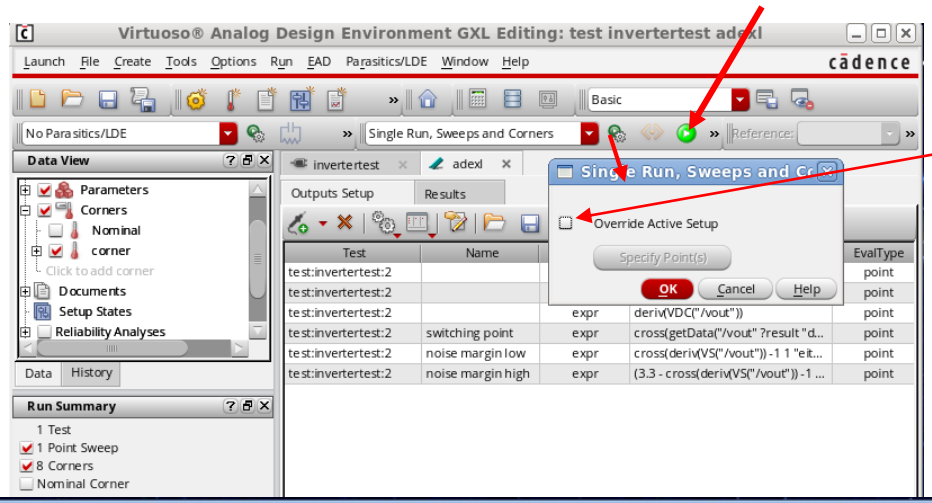


Here we can see all the selected corners

Corner Simulation – Import Corners

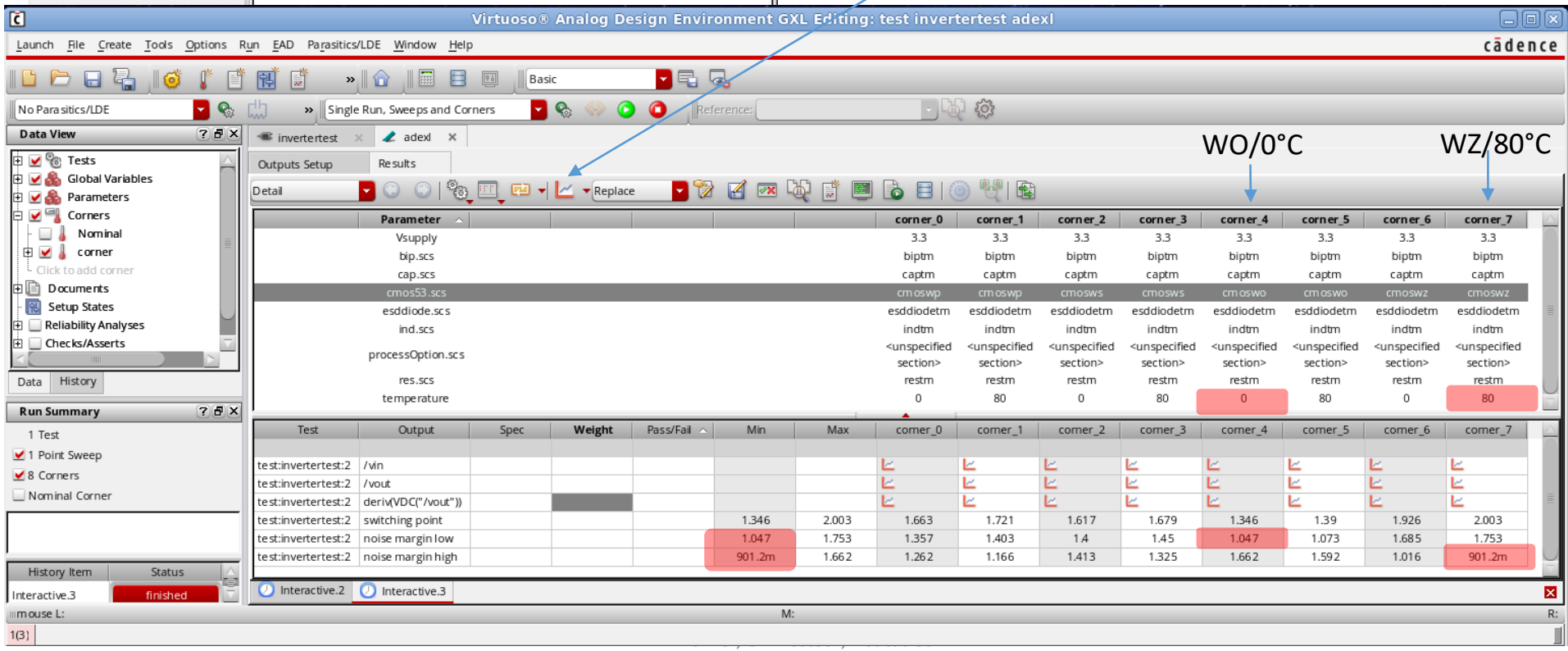


Corner Simulation – Run and Results

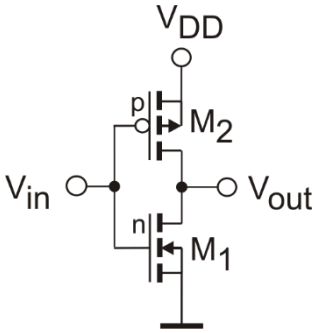


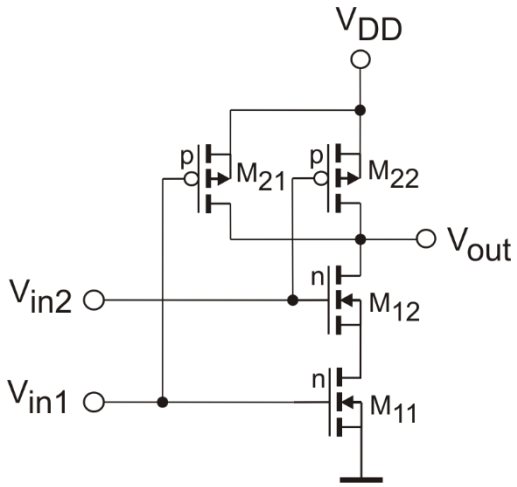
Do NOT select!

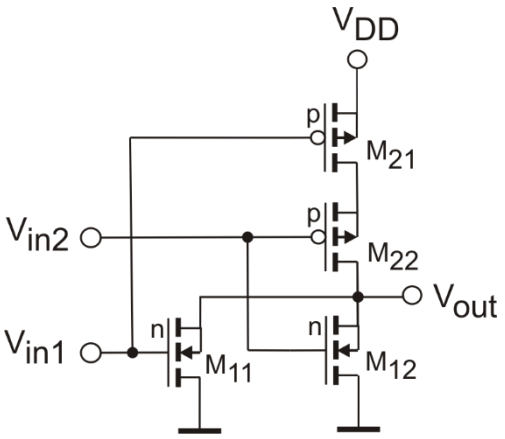
Press to see waveforms!
Not shown here.



Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
Inverter, 2-Input-NAND, 2-Input-NOR







$V_{DD} = 3.3V$
$V_{thn} = 0.48\text{V}$
$V_{thp} = 0.67V$
$KP_n = 170\ \frac{\mu A}{V^2}$
$KP_p = 58\ \frac{\mu A}{V^2}$

$(t_{ox} = 7.6\ nm)$

Calculate the geometry in ($^W/_L$-ratio for p- und n-transistors) so that you get a good compromise for the switching point and noise margin for the cases:

- Both inputs change at the same moment (connected)
- One input is preassigned to a fixed value so that the second one causes output change. (May be different for both inputs!)

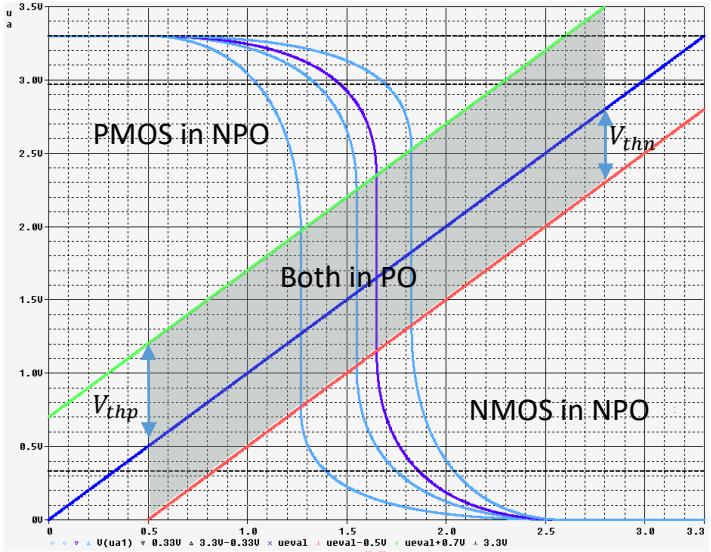
Switching point should be near $\frac{V_{DD}}{2}$ for all cases.

Design (schematic, layout) a 2-Input-NAND or a 2-Input-NOR using short channel length transistors (0.35µ) or long channel length transistors (3.5µm]. Selection of the specific design is done with the tutor.

Cell hight shall be 20 µm.

From Simulation (including postlayout) find out the following values:
Switching points and noise margin for the different cases at the two inputs.
Delay times (50%), falltime, risetime (20%-80%) dependend on load capacitance (4.. 100 fF) and temperature (-40 to 80°C).

Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
Inverter, 2-Input-NAND, 2-Input-NOR



At the switching point both transistor-pairs are in the pinch-off state and passed by the same current :

$$\frac{\beta_n}{2}(V_{inSP} - U_{thn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{inSP} - V_{thp})^2$$

But: There is a difference in the number of involved switching transistors for the different input cases!

Common Equation for **CMOS-Inverter**:

$$\frac{\beta_n}{2}(V_{inSP} - V_{thn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{inS} - V_{thp})^2$$

Dissolve for V_{inSP}:

$$\sqrt{\beta_n}(V_{inSP} - V_{thn}) = \sqrt{\beta_p}(V_{DD} - V_{inSP} - V_{thp})$$

$$V_{inSP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{thn} + V_{DD} - V_{thp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Für $V_{inSP} = \frac{V_{DD}}{2}$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}}\right)^2$$

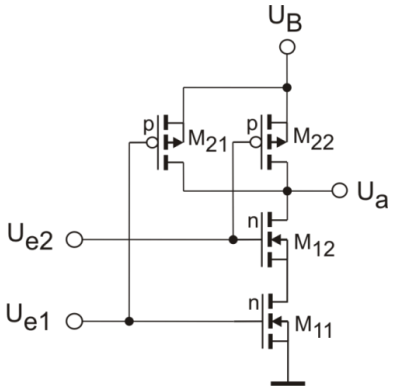
$$\beta = KP \cdot \frac{W}{L}$$

$$mit: \; KPN = 3 \cdot \mathrm{KPP}$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}}\right)^2$$

$$\frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} \approx 3$$

NAND-Gate



For $V_{inSP} = \frac{V_{DD}}{2}$ when both inputs change:

$$\frac{\beta_{nges}}{\beta_{pges}} = \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}}\right)^2$$

$\beta_{nges} = KPN \cdot \frac{1}{2}\left[\frac{W}{L}\right]_n$ One transistor of double length

$\beta_{pges} = KPP \cdot 2\left[\frac{W}{L}\right]_p$ One transistor of double width

$KPN = 3 \cdot \mathrm{KPP}$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{4}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{U_B}{2} - V_{thn}}\right)^2$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{4}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn}}\right)^2 = \frac{4}{3}\left(\frac{1.65 - 0.7}{1.65 - 0.5}\right)^2 = 0.908$$

$$\frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 1.1$$

Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
2-Input-NAND, 2-Input-NOR

$$\frac{\beta_n}{2}(V_{inSP} - V_{thn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{inSP} - V_{thp})^2$$

$$\sqrt{\beta_n}(V_{inSP} - V_{thn}) = \sqrt{\beta_p}(V_{DD} - V_{inSP} - V_{thp})$$

One p-transistor is off and remains off.
One n-Transistor is on and remains on.
Only an inverter is switching.

Lower transistor in NAND during switching phase:

$$U_{eS} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot (V_{thn} + V_{DS11}) + V_{thn_B} - V_{thp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

See if the values are acceptable with regard to noise margin.
Try to change W/L ratios to find a compromise.

For $V_{inSP} = \frac{V_{DD}}{2}$

$$\beta_{nges} = KPN \cdot \frac{W}{L}$$

$$\beta_{pges} = KPN \cdot \frac{W}{L}$$

$$KPN = 3 \cdot \text{KPP}$$

$$\frac{\beta_n}{\beta_p} = \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn} - V_{DS11}}\right)^2$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{\frac{V_{DD}}{2} - V_{thp}}{\frac{V_{DD}}{2} - V_{thn} - V_{DS11}}\right)^2$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1.65 - 0.7}{1.65 - 0.5 - 0.236}\right)^2 = 0.36 \qquad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 2.78$$

$$\frac{\left[\frac{W}{L}\right]_n}{\left[\frac{W}{L}\right]_p} = \frac{1}{3} \cdot \left(\frac{1.65 - 0.7}{1.65 - 0.5}\right)^2 = 0.23 \qquad \frac{\left[\frac{W}{L}\right]_p}{\left[\frac{W}{L}\right]_n} = 4.44$$

Interesting, but we can implement one geometry only and must configure a compromise.

Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
2-Input-NAND, 2-Input-NOR

$$V_{inSP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot (V_{Thn} + V_{DS11}) + V_{DD} - V_{thp}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Using the Relation for switching both transistors $^{W}/_{L} - relation = 1.1$:

KPN/KPP

$$V_{inSPu} = \frac{\sqrt{\frac{3}{1.1}} \cdot 0.5V + 3.3V - 0.7V}{1 + \sqrt{\frac{3}{1,1}}} = 1.29\ V$$

$$\left[\frac{W}{L}\right]_p \Big/ \left[\frac{W}{L}\right]_n$$

$$V_{inSPo} = \frac{\sqrt{\frac{3}{1.1}} \cdot 0.5V + 0.236V + 3.3V - 0.7V}{1 + \sqrt{\frac{3}{1,1}}} = 1.38\ V$$

Not considered:
Conducting NMOS has a resistance ($U_{DS} > 0$)
Body-/Backgate-Effect (U_{Th} dependent of subtrate voltage)

$^{W}/_{L} - Relation$ PMOS/NMOS	V_{inSP} when switching both inputs [Volts] and difference to V_{DD}	V_{inSP} only "upper NMOS" switching [Volts] and difference to V_{DD}	V_{inSP} only "lower NMOS" switching [Volts] and difference to V_{DD}
1.1	1.65 / 1.65	1.36 / 1. 94	1.30 / 2.00
2.2	1.83 / 1.47	1.55 / 1.75	1.47 / 1.83
3.3	1.92 / 1.38	1.66 / 1.64	1.58 / 1.72
4.4	1.98 / 1.32	1.74 / 1.56	1.66 / 1.64

Switching input voltage $\boldsymbol{V_{inSP}}$ for different $^{W}/_{L}$ - relations of the transistors from **Simulation**

Lab: Circuit Design using Cadence and AMS CMOS 0.35µ Technology
2-Input-NAND, 2-Input-NOR

Practical hint to safe time:

Starting from the inverter schematic:

You may open the inverter schematic as the origin for the new design.

Then create a new schematic cellview (from CDW or Library Manager). **File -> New -> Cellview**

When you have the new empty schematic and the inverter schematic side by side you can copy the inverter circuit or parts of it to the new schematic.

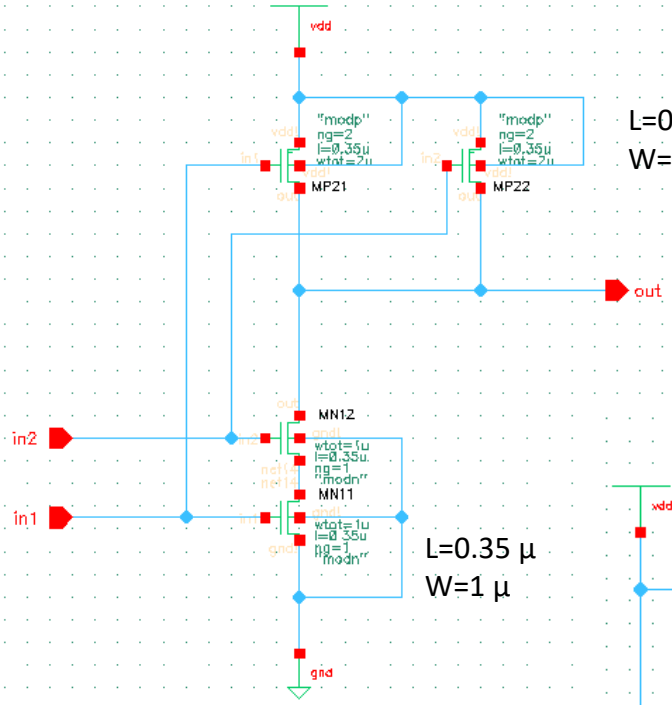
Use copy: "**c**" -> select the desired part using the left mouse button
-> click on the selected part
-> drag to the new place (may be the same schematic window or the new one)

Copy object from one schematic window to another: In target no command should be active! (Use ESC sometimes!)

Edit the new schematic to build the NAND or NOR design.

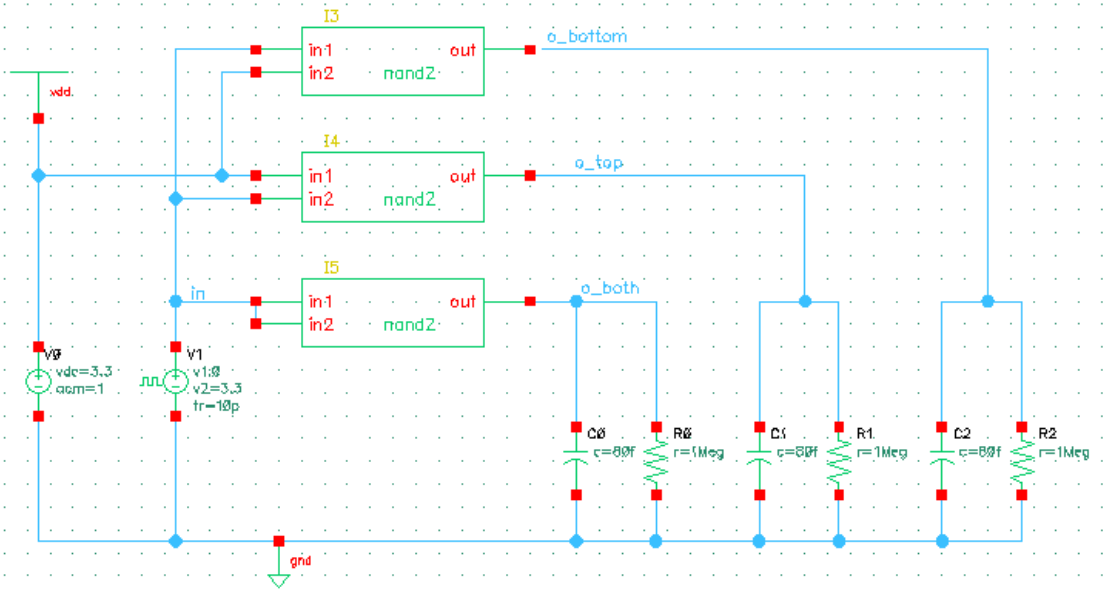
You may proceed in the same manner for the testbench.

2-input-NAND Schematic and associated Testbench

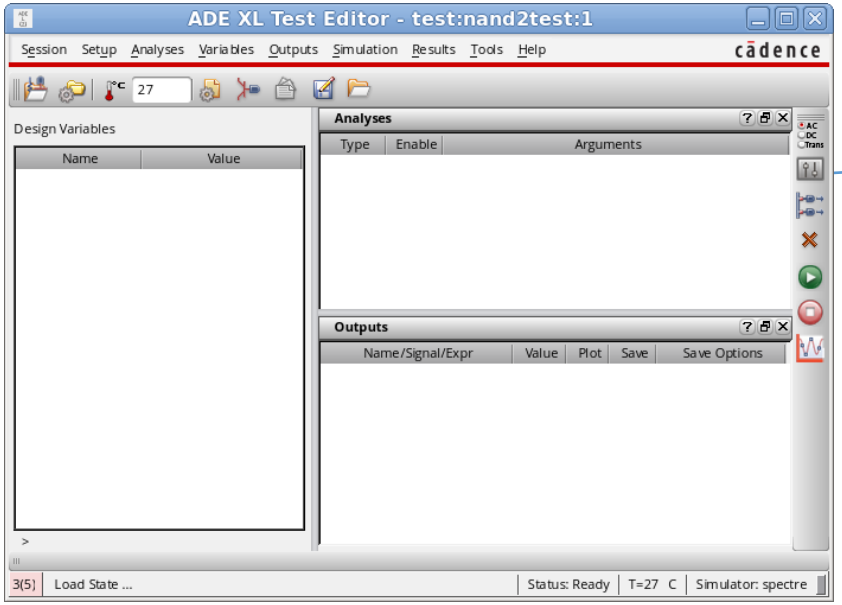


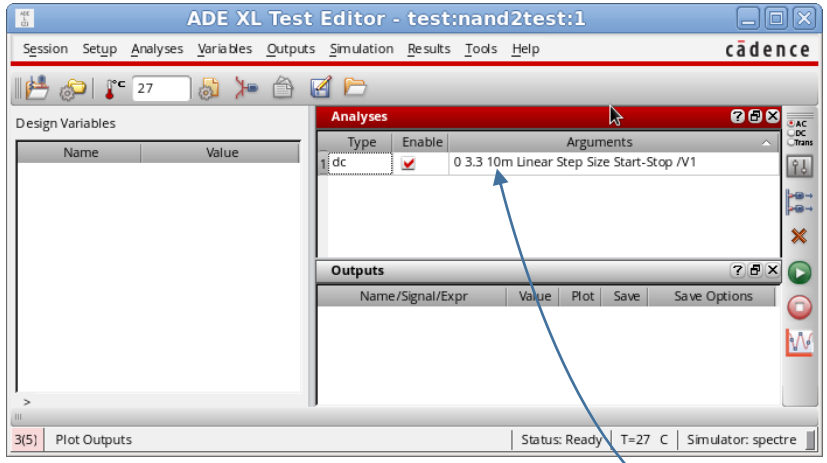
L=0.35 µ
W=2 µ

L=0.35 µ
W=1 µ

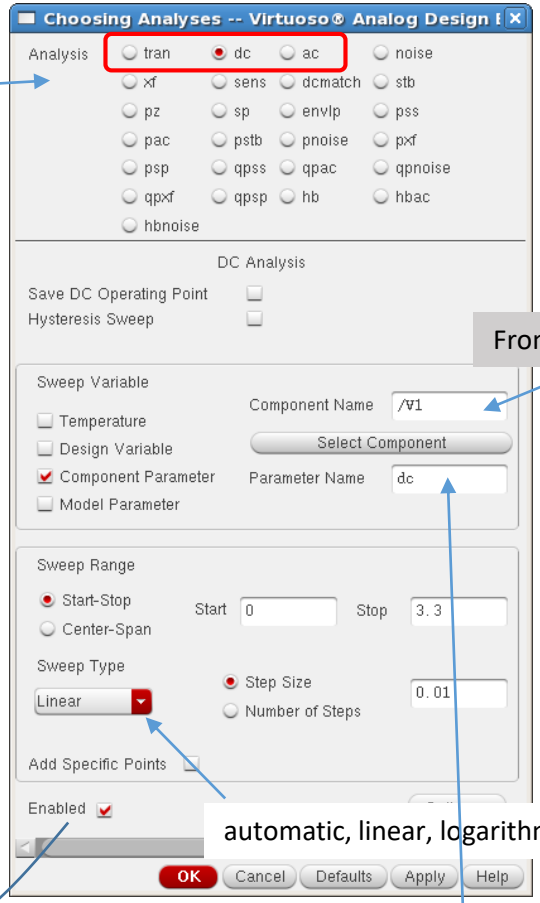


2-Input-NAND, 2-Input-NOR – Use steps as before in inverter simulation



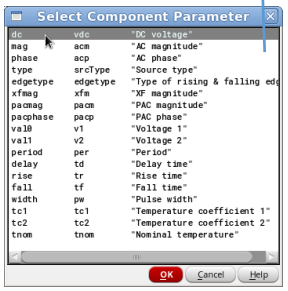


Create/Edit analyses
Design Variables
Simulation Outputs
Delete selected analyses
Run enabled analyses
Stop
Plot

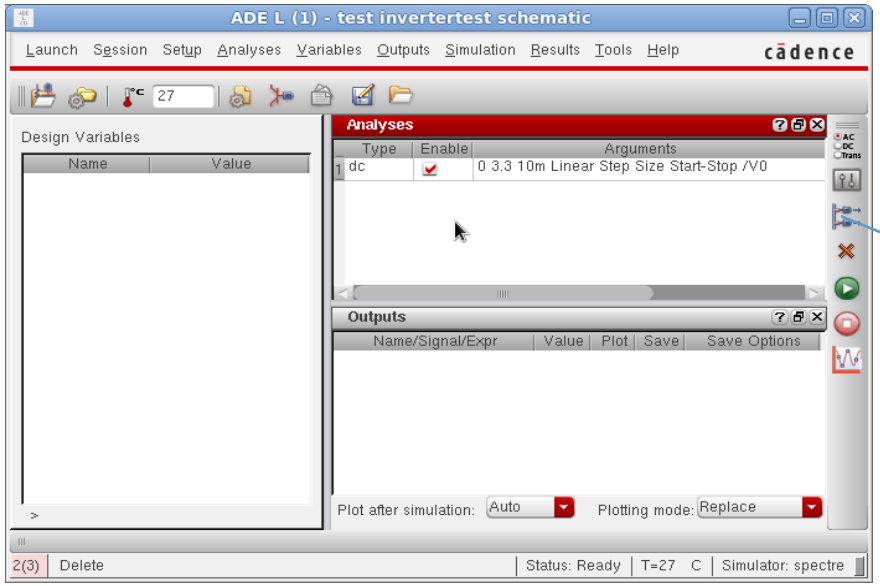


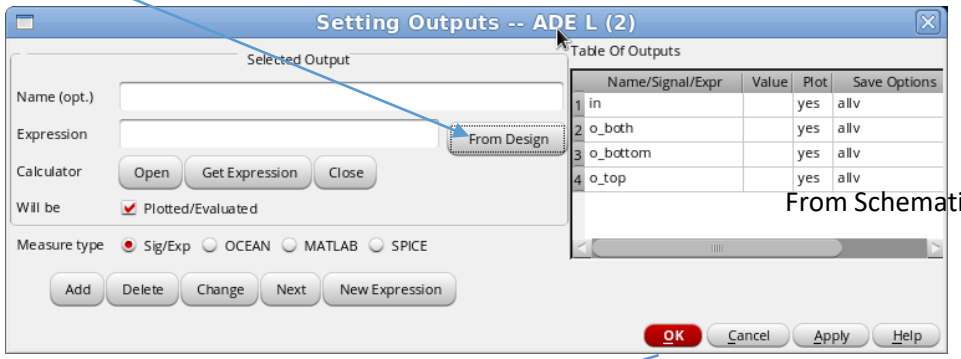
From Schematic

automatic, linear, logarithmic

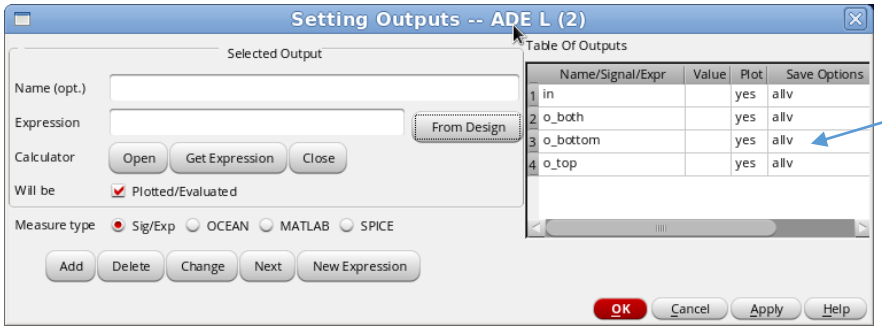


2-Input-NAND, 2-Input-NOR – Use steps as before in inverter simulation

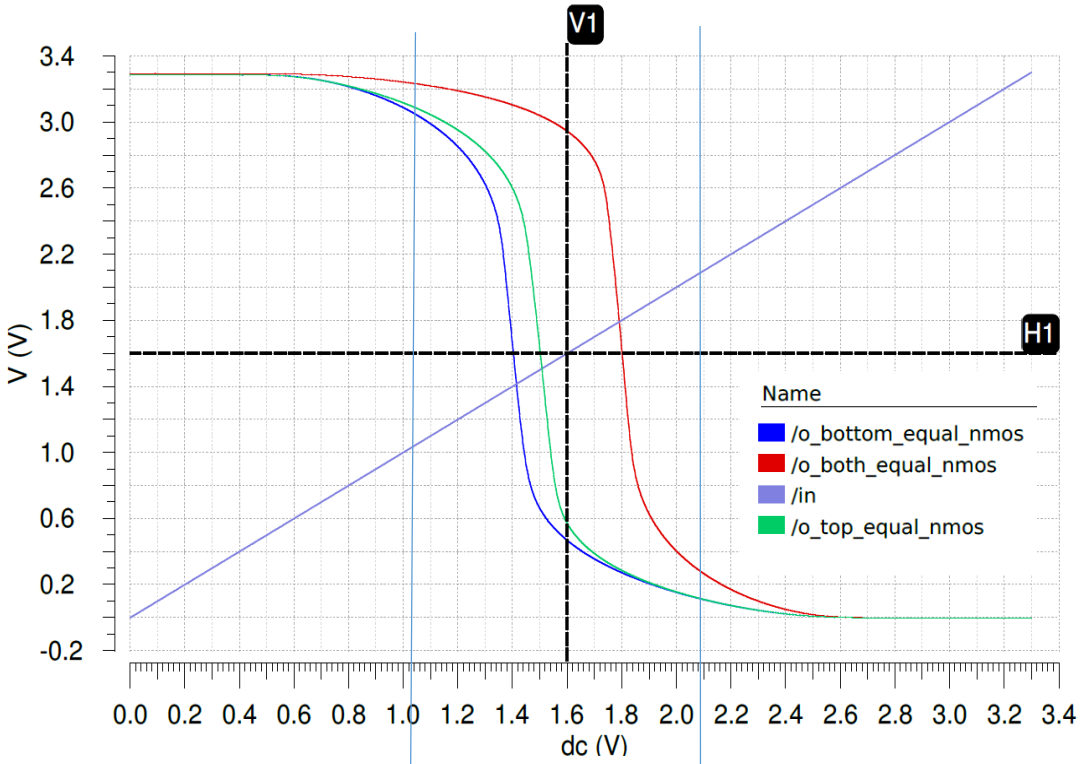




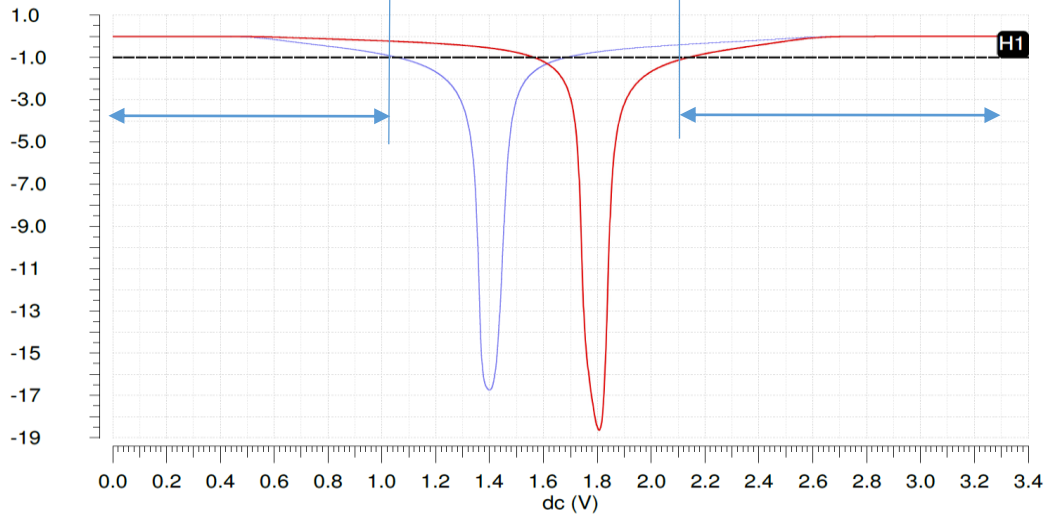
From Schematic



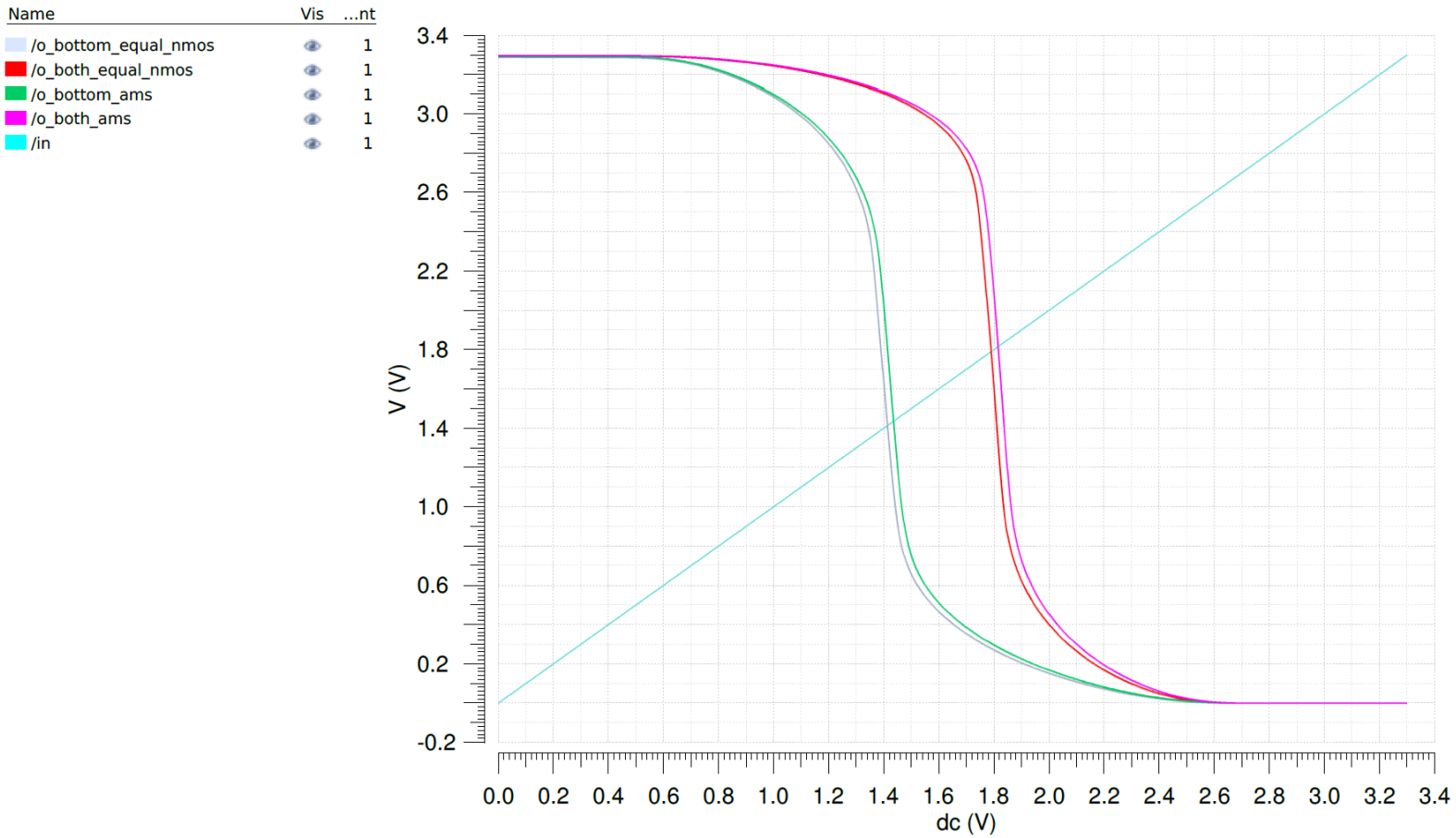
Transfer characteristics and noise margin for 2-Input-CMOS-NAND-Gate



$$\frac{dV_{out}}{dV_{in}}$$

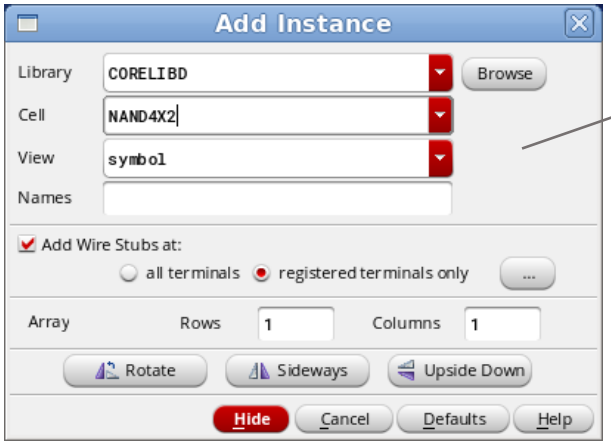


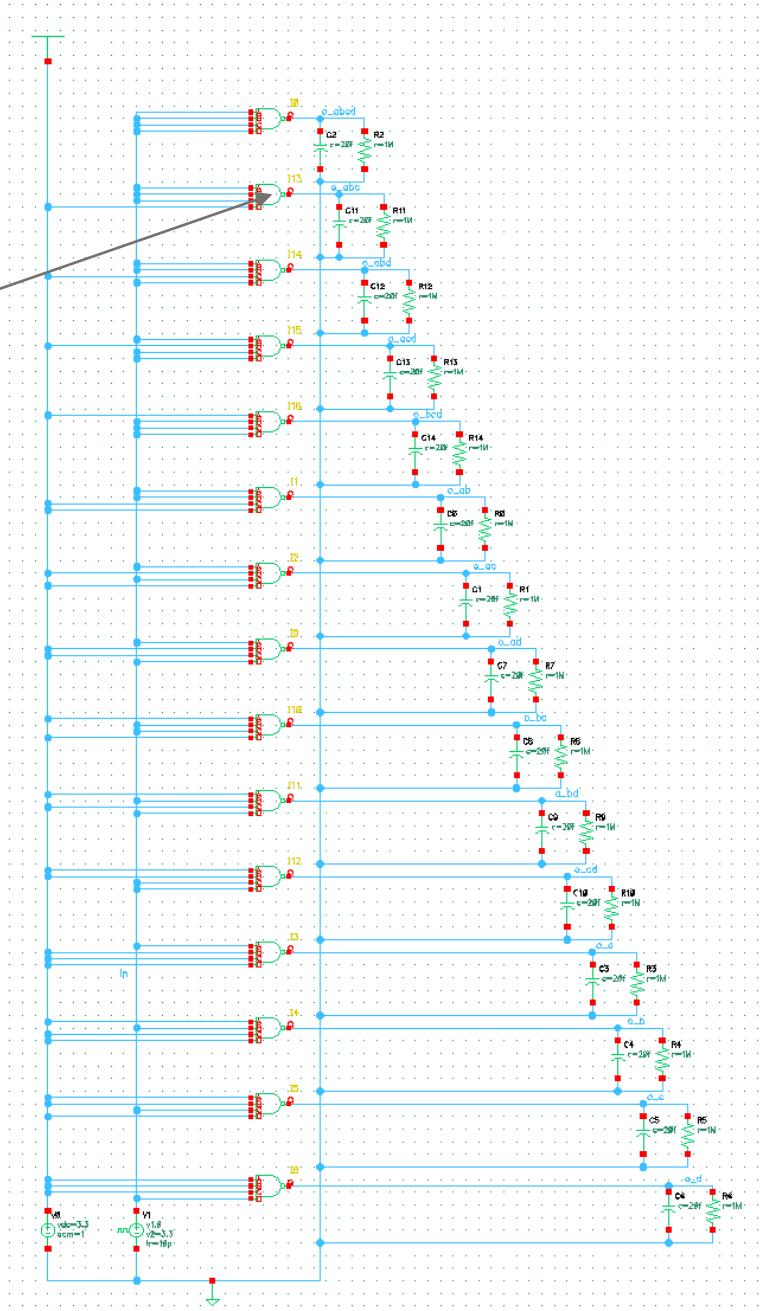
Transfer characteristic for 2-Input-CMOS-NAND-Gates



Transfer characteristics of 2-input-NAND-Gates
from AMS-0.35µ-library with $L_{NMOS,PMOS} = 0.35\mu, W_{NMOS} = 1.325\mu, W_{PMOS} = 2.1\mu$
and
self-made gate with $L_{NMOS,PMOS} = 0.35\mu, W_{NMOS} = 1.0\mu, W_{PMOS} = 1.6\mu$
(Characteristics for switching top N-transistor only not shown, always between bottom and both cases)

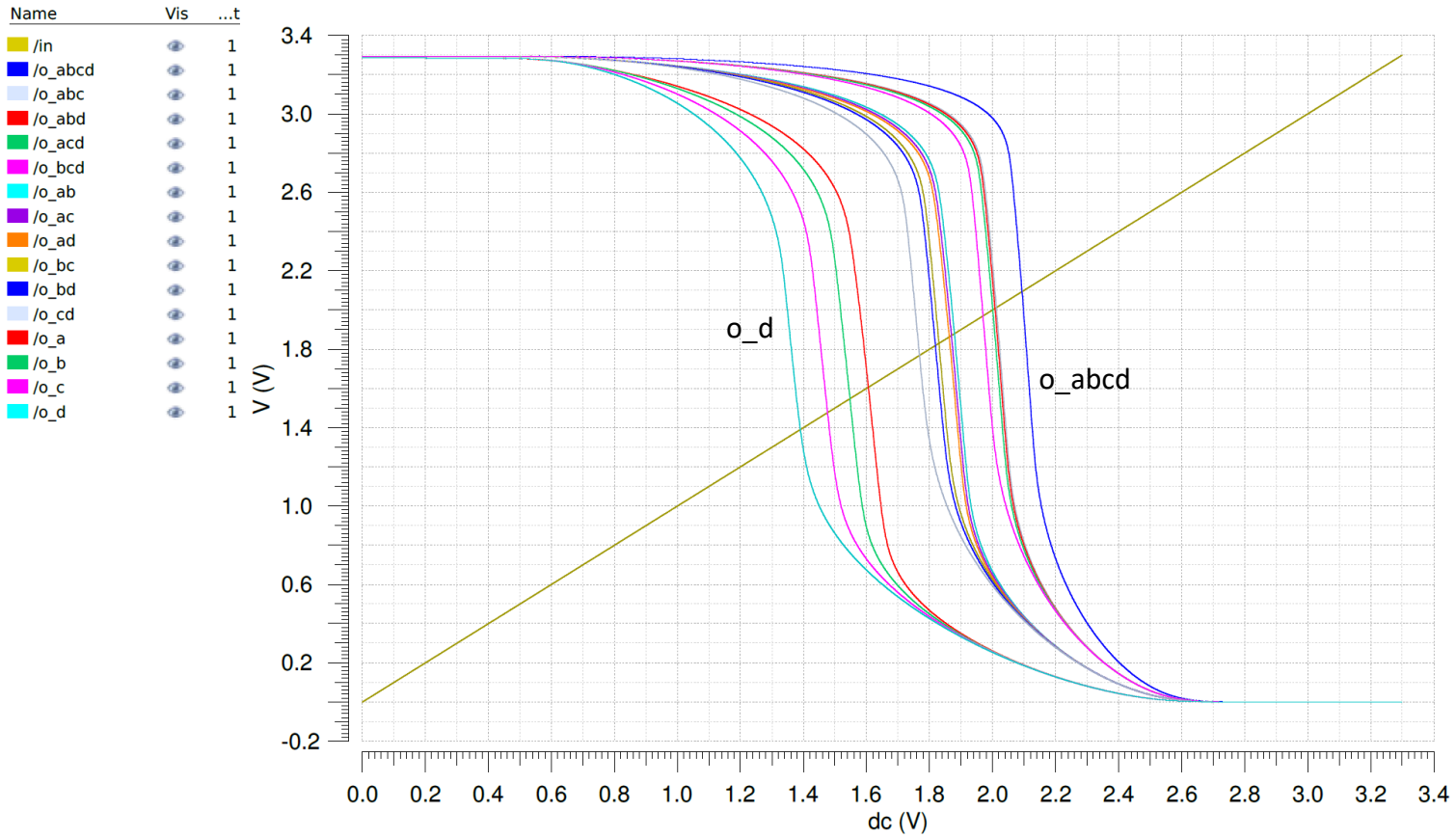
Simulation of 4-input-NAND from 0.35µm library





D-input uses NMOS-transistor nearest to GND, A-input is top NMOS-transistor.

4-Input-NAND-Gate from AMS-0.35µ-library

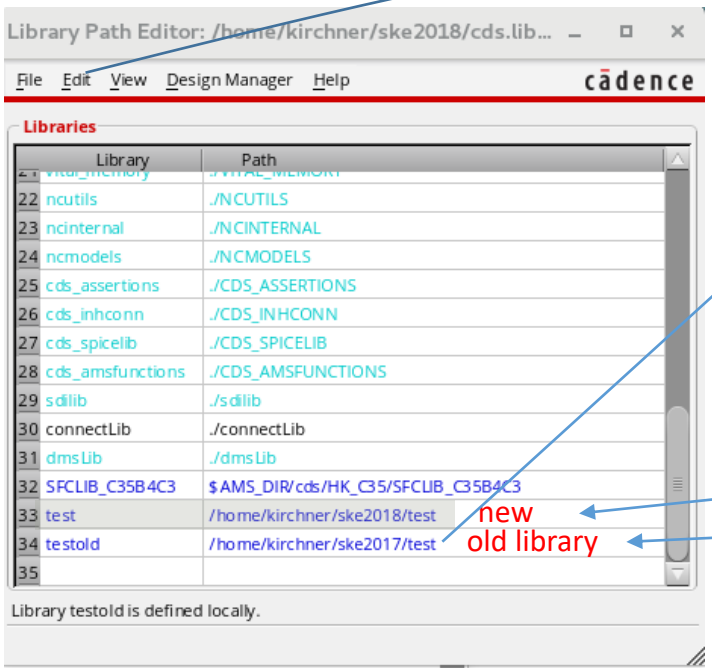


Transfer characteristic of 4-input-NAND-Gate from AMS-0.35µ-library
with $L_{NMOS,PMOS} = 0.35\mu\, W_{NMOS} = 1.05\mu, W_{PMOS} = 1.4\mu$
Leftmost line for switching lowest (nearest to ground)nmos-transistor only,
rightmost line for all 4 inputs switched simultaneously

Cadence Transfer Library Content to a new Library

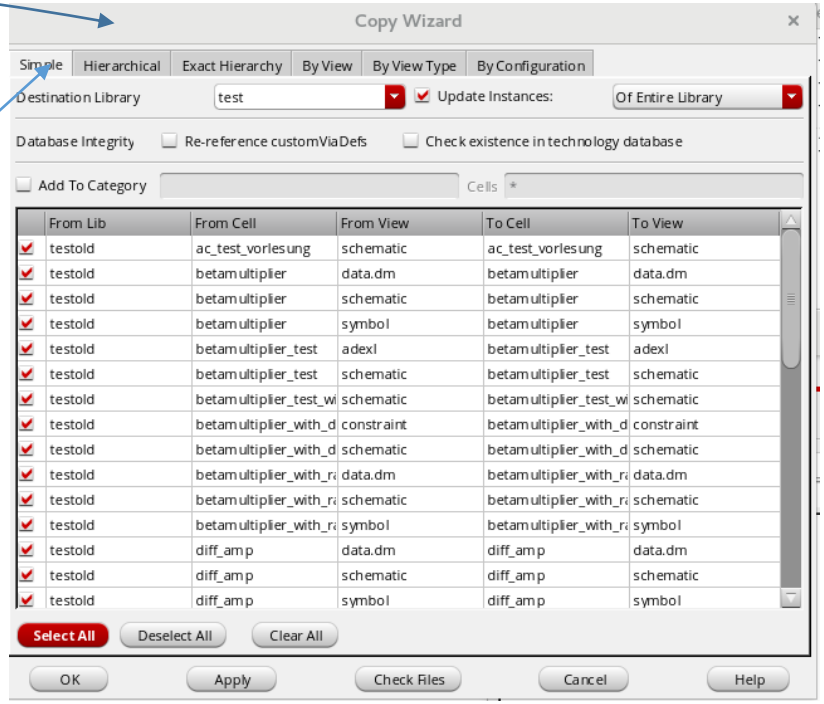
Use Cadence tools always! DO NOT copy in linux.

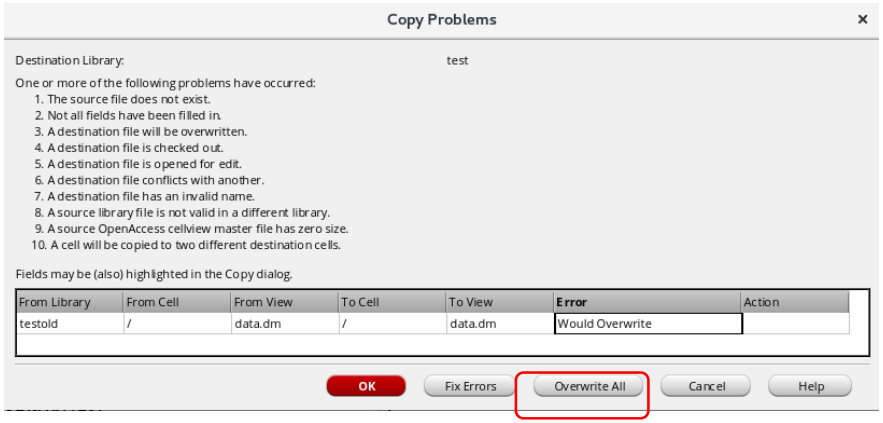
Edit -> Copy Wizard

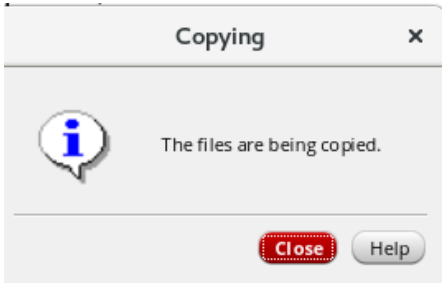


new
old library

Create before!
Enter path!







When we will have finished copying we can delete the old libraries entry.

We get a warning because we are coying the library completely.
Acknowledge with "Overwrite All" !