

## Lab 2 "Programmable Integrated Circuits"

### "School Grade Die" with Lattice ispMACH4256ZE (Verilog)

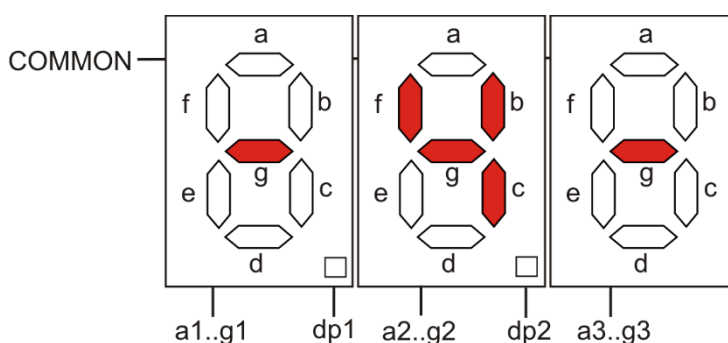
A "school grade die" shall be implemented in an ispMACH400ZE-CPLD with 256 logic cells. The frequency of occurrence observed for the grades 1 to 5 shall be adjustable in 1%-steps.

The "Story" is that a professor determines the results not by the time-consuming process of reading and evaluating the written exams. He simply uses his die. By adjusting the die he can pretend a "normal" result over the entirety of the students to hide his cheating. For example 9% get grade 1, 22% get grade 2 et cetera.

We use a board (ispMACH400ZE Pico Development Kit) with a 3-digit-LCD display and a button (low-output if pressed) that we can use as a RUN-button. The Board uses the **Lattice ispMACH4256ZE-5MN144C** in a BGA-package. The CPLD has an internal clock generator (about 50 MHz) dividable by 1:1, 1K:1, 1Meg:1.

When the RUN button is not pressed one digit of the 3-digit-LCD display shall show the grade N between 1 and 5. The two other digits shall show "-". When the Button is pressed the internal grade counter shall count using the 50 MHz clock. The LCD display must be driven by an alternating voltage. The frequency should be 60 .. 80 Hz.

There is one COMMON-input for all segments and separated inputs for the individual segments. To activate a segment (display a bar) there must be applied an alternating voltage between COMMON and SEGMENT inputs. An easy way to do so is to apply a clock CLK to COMMON and a signal CLK xor SEGMENT\_VALUE to the SEGMENT input. For inactive segments (no bar) CLK will be applied both to COMMON and SEGMENT inputs.



Common Pin PM2					
Left (1)		Middle (2)		Right(3)	
Segment	Pin	Segment	Pin	Segment	Pin
a1	PB1	a2	PE2	a3	PB6
b1	PC3	b2	PF2	b3	PA6
c1	PC2	c2	PM1	c3	PC6
d1	PC1	d2	PF1	d3	PB5
e1	PD1	e2	PF3	e3	PA5

f1	PD2	f2	PG1	f3	PA4
g1	PD3	g2	PE3	g3	PB4
dp1	PB2	dp2	PE1		

The synthesis program expects the Letter "P" in front of the pin name from the data sheet.

**The Button is located at pin PH11. For the button input the CPLDs internal pulldown resistor must become deactivated. It is activated by default!**

The pulldown in the CPLD pulls about 30µA. The external pullup at the button has a value of 100 kΩ. So there will never be a valid logic high level at the button output as long as the pulldown in the CPLD is active. Pulldown can be deactivated using the Constraint-Editor. When we generate the JEDEC-File we must select "Merge" for the constraint import.

The oscillator is included as a library module in the verilog description.

Declaration:

```
module osctimer(DYNOSCDIS, TIMERRES, OSCOUT, TIMEROUT);

parameter TIMER_DIV = "128";
input DYNOSCDIS;
input TIMERRES;
output OSCOUT;
output TIMEROUT;
endmodule
```

The oscillator is used with a divider of 1024.

Instantiation:

```
defparam I1.TIMER_DIV = "1024",

osctimer I1 (.DYNOSCDIS(1'b0), .TIMERRES(resettimer),
            .OSCOUT(CLK_5M), .TIMEROUT(CLK_5K));
```

"resettimer" is an H-active reset signal.

CLK\_5M und CLK\_5K should be replaced by the names used for the 5 MHz- and 5 KHz- clocks respectively. I1 is the user-defined instance name of the oscillator.

In the Lab we use ispLever Classic (Development) and ispVM(Configuration over USB) as software. Details will be discussed in the class.

Information sources:

Software: [http://www.latticesemi.com/dynamic/view\\_document.cfm?document\\_id=47330](http://www.latticesemi.com/dynamic/view_document.cfm?document_id=47330)

Demoboard:

<http://www.latticesemi.com/products/developmenthardware/developmentkits/ispmach4000zepico/devkit.cfm>

CPLD: [http://www.latticesemi.com/dynamic/view\\_document.cfm?document\\_id=29095](http://www.latticesemi.com/dynamic/view_document.cfm?document_id=29095)