Lab 1 "Programmable Integrated Circuits“

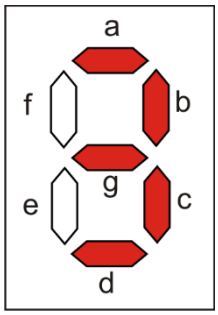
Dice with Lattice GAL16V8 and GAL22V10 (Verilog)

We want to use simple GAL-PLD to implement different versions of dice.

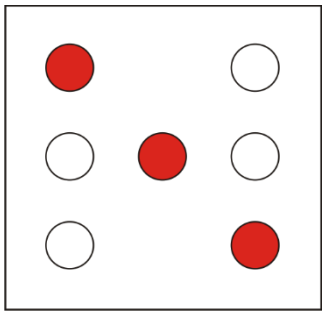
Pin 1 of the GAL is always connected to a clock. The clock can be "hand driven" using a push button for test purposes or can be connected to an external clock of up to 50 MHz in normal mode. (See appended schematics!)

Pin 2 is connected to a second push button. When pressed the die shall roll, when not pressed the result is shown. We get a random result because there is no correlation between the clock (or the count cycle of our die driven by the clock) and the moment of releasing the run button.

The outputs may be connected by two kinds of displays (See schematics for details!):



7-segment display



7-dot die surface

First (GAL16V8):

Die shall count as an ordinary die from 1 to 6. One may implement two versions with different output patterns to fit a 7-segment display or a 7-dot die surface.

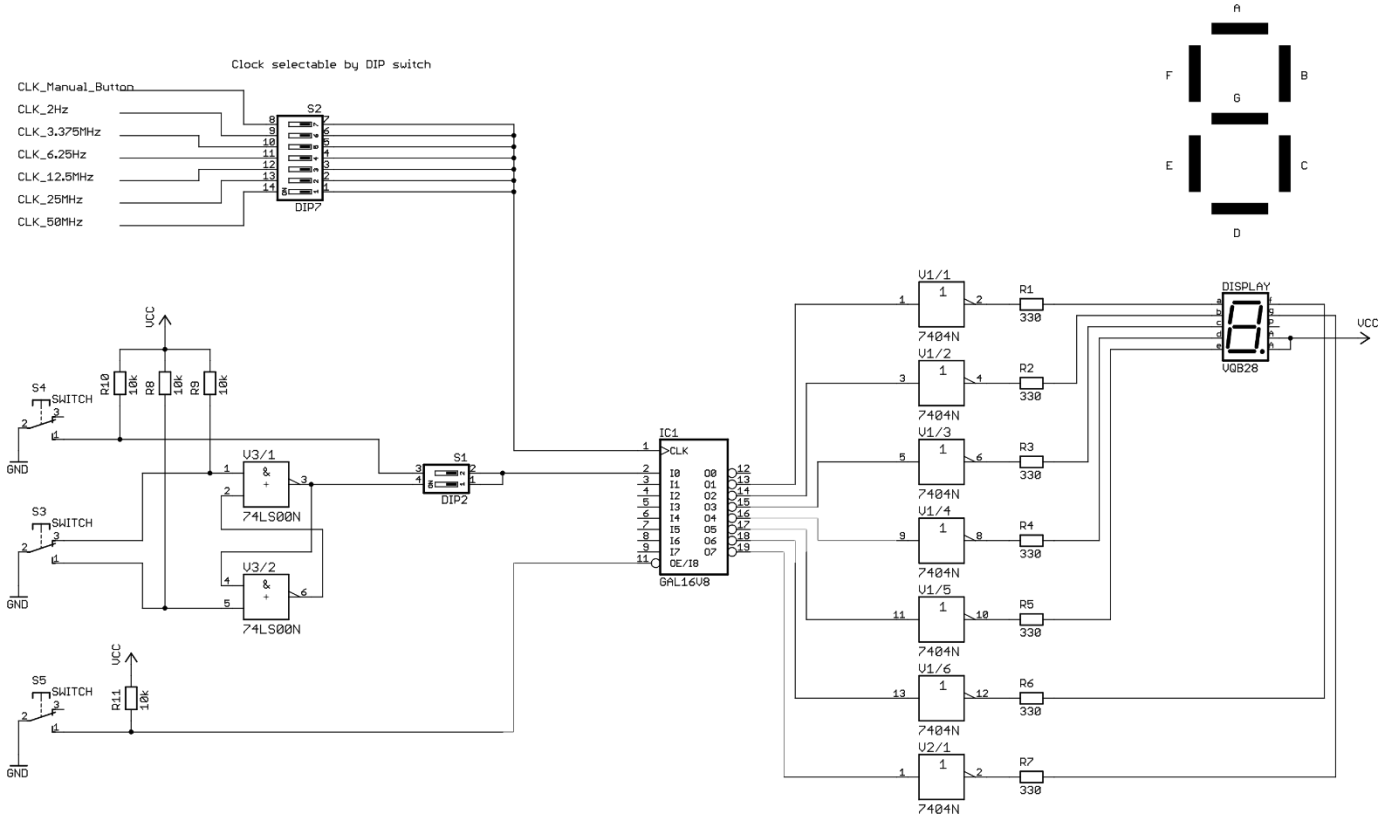
Second (GAL22V10):

We construct a die for school grades (marks). Student's results are valuated from 1 (best) to 5 (not sufficient). A professor wants to omit the time-consuming work of reading and evaluating written exams. He simply uses his die. But the overall result should be "normal": few student s with very good and not sufficient, most of the students with average results.
So he wants to have a die with average

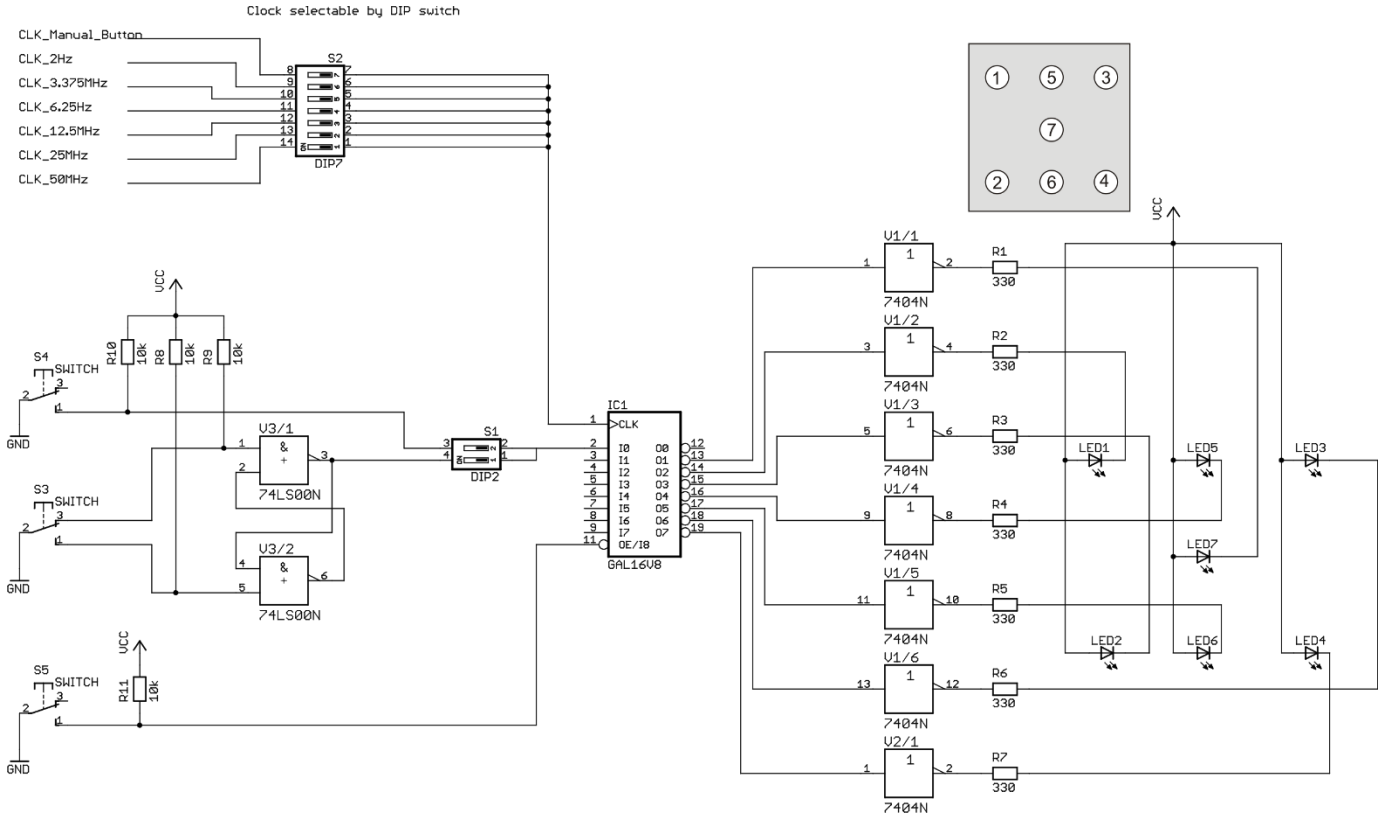
1 occurrence of grade 1
2 occurrences of grade 2
5 occurrences of grade 3
2 occurrences of grade 4
1 occurrence of grade 5

Use Verilog as a description language!

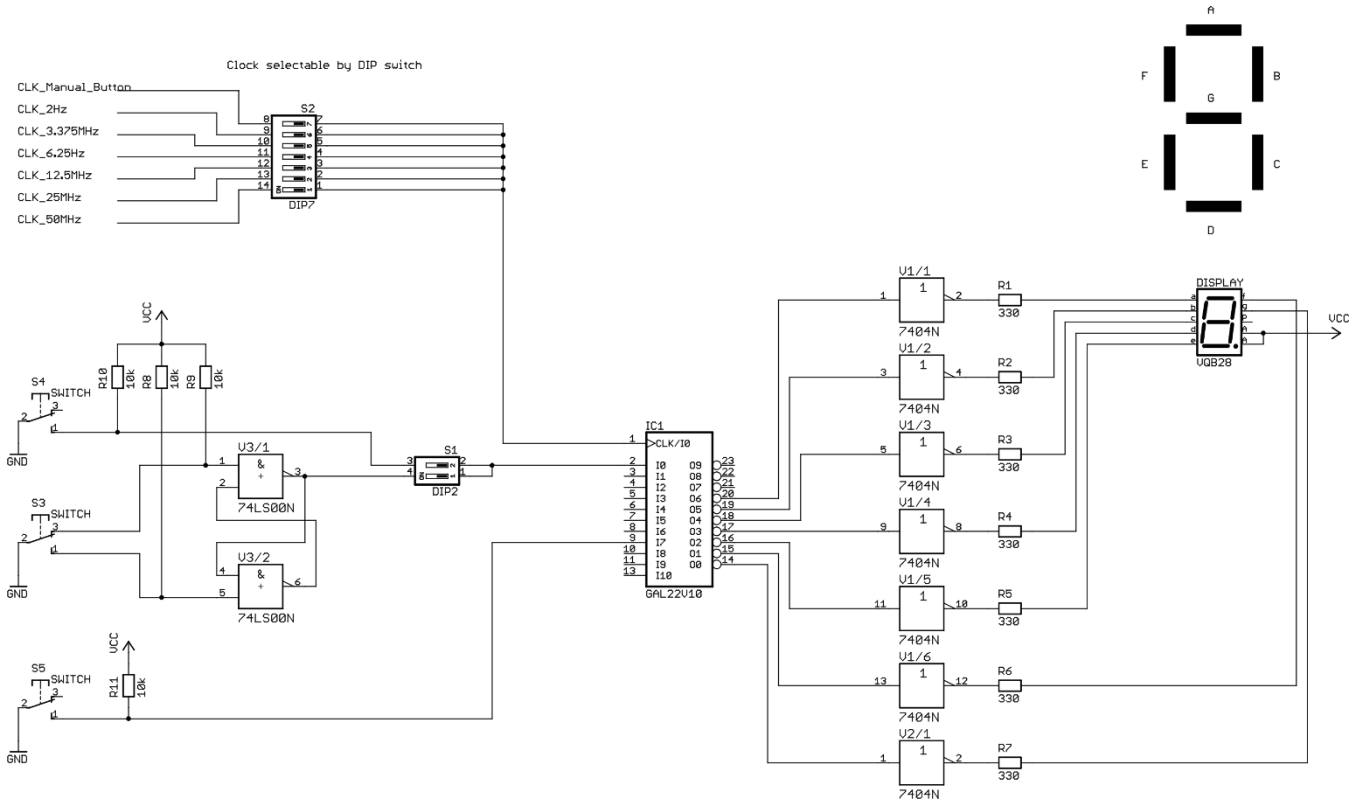
Next pages show the schematics of the experimental board for different output patterns and two GAL-types.



GAL16V8 Simple Die with 7-Segment Display



GAL16V8 Simple Die with 7-dot die surface



GAL22V10 with 7-Segment Display for "School Grade Die"